EPITAXIAL GALLIUM ARSENIDE WAFERS

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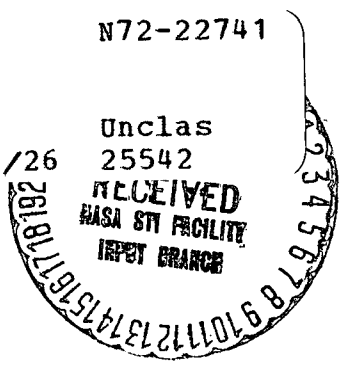

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16. Abstract

The preparation of GaAs epitaxial layers by a vapor transport process using $AsCl_3$, Ga and H_2 was pursued to provide epitaxial wafers suitable for the fabrication of transferred electron oscillators and amplifiers operating in the subcritical region. Both n-n+ structures, and n++-n-n+ sandwich structures were grown using n+ (Si-doped) GaAs substrates. Sixty-five epitaxial wafers were supplied to NASA-Goddard. Process variables such as the input $AsCl_3$ concentration, gallium temperature, and substrate temperature and temperature gradient and their effects on properties are presented and discussed. N-layers were grown with carrier concentrations in the range of 1×10^{14} to 1×10^{15} cm^{-3}, with room temperature mobilities of 6000 $cm^2/V \cdot sec$ and above and with thicknesses ranging from 6 to 40 micrometers. Most of these n-layers had mobilities of 50,000 $cm^2/V \cdot sec$ or above at 77°K and several had 77°K mobilities above 90,000 $cm^2/V \cdot sec$. The n^{++} layer in sandwich structures were normally grown to a thickness in the range 2 μm to 4 μm, with $n^{++} > 2 \times 10^{18}$ cm^{-3}.

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PREFACE

Objectives

The principal objectives of this contract were to develop fabrication methods for, and to fabricate, n-n+ and n+-n-n+ gallium arsenide epitaxial structures for use in producing transferred electron oscillators and amplifiers. Specific contract requirements called for the n+ substrate wafers to be silicon doped, approximately one inch in diameter, with a resistivity of approximately 10^{-3} ohm·cm, and a thickness of approximately 0.5 mm (0.02 inch). Epitaxial structures were to be fabricated according to the following schedules.

1. Twenty-five n-n+ wafers: The n-type epitaxial layer to have electrical properties and thickness such that the $n\ell$ product be suitable for devices to operate in the subcritical range.
2. Twenty-five n+-n-n+ wafers: This structure to consist of n-n+ structures as described in Schedule 1 with an additional n+ layer grown on the n-region to form a sandwich structure.
3. Fifteen epitaxial structures similar to Schedules 1 or 2, but with the thickness of the n-layer ranging from 12 μm to 40 μm in increments of 2 μm.

Scope of Work

The work program emphasized a careful, detailed, definition of each of the operating parameters of our vapor-phase epitaxial reactor, to determine which of them were of critical importance to the contract goals. In addition, the influence of wafer preparation techniques, and the effects of reactor system assembly, disassembly, and cleaning procedures were evaluated. Evaluation of grown layers was also emphasized. This provided the means for collecting sufficient sample data for correlation with the day-to-day and run-to-run changes in growth conditions so that we could unambiguously determine the influence of the several system and process variables on grown epitaxial layers. Later on, the rapid evaluation of the GaAs layers prepared in our reactor proved necessary to make controlled changes in growth parameters from run to run to keep the prepared material within contract specifications. The following highlights deserve specific mention.

- All of the n+ substrate wafers used had dislocation density below $1000/cm^2$.
- Charge carrier mobilities at 77°K were usually above 50,000 $cm^2/V \cdot sec$. Several layers had mobility above 90,000 $cm^2/V \cdot sec$ and one had 101,400 $cm^2/V \cdot sec$.

- It was not necessary to use sources of n-dopants such as sulfur, selenium, or tellurium in the epitaxial reactor to control the electron concentration in grown n-layers. With properly selected batches of $AsCl_3$, control of free electron concentration over the range $1 \times 10^{14}/cm^3$ to $1 \times 10^{15}/cm^3$ could be achieved by adjustment of several system parameters.

Conclusions

The vapor epitaxial growth method described in this report can produce GaAs epitaxial layers with thickness and electrical properties in the range desired for sub-critical Gunn devices. However care must be taken in processing the substrates before epitaxy, and in the selection of the highest purity chemicals to accomplish this. This investigation has demonstrated the feasibility of controlling the carrier concentration and resistivity of epitaxial layers by close regulation of gallium source temperature, substrate temperature and input $AsCl_3$ mole fraction.

Summary of Recommendations

It is important to conduct a careful correlation of device performance with material properties. This would be particularly meaningful in this case because of the detailed information that has been obtained for each wafer.

ABSTRACT

The preparation of GaAs epitaxial layers by a vapor transport process using $AsCl_3$, Ga and H_2 was pursued to provide epitaxial wafers suitable for the fabrication of transferred electron oscillators and amplifiers operating in the subcritical region. Both n-n+ structures, and n++-n-n+ sandwich structures were grown using n+ (Si-doped) GaAs substrates. Sixty-five epitaxial wafers were supplied to NASA-Goddard. Process variables such as the input $AsCl_3$ concentration, gallium temperature, and substrate temperature and temperature gradient and their effects on properties are presented and discussed. N-layers were grown with carrier concentrations in the range of 1×10^{14} to 1×10^{15} cm^{-3}, with room temperature mobilities of 6000 $cm^2/V \cdot sec$ and above and with thicknesses ranging from 6 to 40 micrometers. Most of these n-layers had mobilities of 50,000 $cm^2/V \cdot sec$ or above at 77°K and several had 77°K mobilities above 90,000 $cm^2/V \cdot sec$. The n++ layer in sandwich structures were normally grown to a thickness in the range 2 μm to 4 μm, with $n^{++} > 2 \times 10^{18}$ cm^{-3}.

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1. EXPERIMENTAL APPARATUS AND PROCEDURES

1.1 Cleaning Procedures and Substrate Preparation

The successful preparation of n-n+ gallium arsenide wafers for microwave devices depends on the purity of the starting chemicals, the substrate surface treatment, and the reactor cleaning procedure.[1] To prepare n-layers containing a low free-carrier concentration with the requisite high mobility, special semiconductor grade chemicals and ultra-high-purity water (> 12 megohm· cm) must be used along with rigorous cleaning procedures.

1.1.1 Chemicals

Reagent chemicals were selected that are particularly low in Cu, Fe and other heavy metals as follows:

Inorganic Acids - H_2SO_4, HNO_3, HCL (37%) and HF (49%) - TransistAR*
Mallinckrodt Chemical Works

Organic Solvents - Methyl Alcohol (anhydrous), Trichloroethylene - TransistAR*
Mallinckrodt Chemical Works

Hydrogen Peroxide - 30% solution - TransistAR*
Mallinckrodt Chemical Works

Genesolv-D (Trifluoro-trichloroethane) - Electronic Grade
Allied Chemical

Deionized Water - 12 to 18 megohm· cm resistivity from a Barnstead distilled, deionized water system.

Before assembling the reactor, all quartz and pyrex parts were soaked in aqua regia for several hours, etched in a 10 percent solution of HF rinsed in high-purity deionized H_2O and air dried at 110 to 120°C.

1.1.2 Substrate Processing

Single crystal Si-doped GaAs with resistivities of approximately 10^{-3} ohm· cm and dislocation densities of less than 1000/cm^2 were used for n+ substrates. Ingots oriented 2 degrees from a {100} plane towards a [111] were cut into wafers with a diamond-tipped saw on a precision wafering machine. Slices were usually 0.63 mm thick before they were lapped for parallelism and elimination of gross saw damage.

Substrate processing for epitaxial growth consisted of three phases:

- Chemo-mechanical polish with a Lustrox 1550 solution on a rotating Supreme-K cloth to provide an optically flat and polished surface.

- Chemical polish to remove residual polish scratches (revealed by x-ray diffraction topography).
- A final in situ vapor etch to provide a clean surface for epitaxy.

The procedure used in the chemical polish is briefly outlined as follows:

- Deionized high purity H_2O (10-18 megohm·cm) rinse to remove dust and lint followed by an anhydrous methanol rinse.
- Ultrasonically clean in warm trichloroethylene to remove traces of oil or wax from the ingot mounting and slicing step.
- Rinse in successive portions of anhydrous methanol and then in running high purity H_2O.
- Place in hot $HCl:H_2O$ (1:1) to remove any chemo-mechanical polishing compound.
- Rinse thoroughly in running high purity H_2O.
- Chemically polish at 70°C in $5H_2SO_4:1H_2O_2:1H_2O$ for 1 minute.
- Dilute in ~ 200 cm^3 high-purity H_2O without exposing substrates to atmosphere.
- Rinse in running high-purity H_2O, 15 minutes.
- Multiple rinses in anhydrous CH_3OH.
- Samples placed in electronic grade Freon. Trade name Genesolve-D (Allied Chemical).

Substrates were kept under Freon with no further treatment and then loaded directly onto the substrate holder for vapor etching. Loading of the substrates was done under a strong helium flow (4 liters/min) and Pd-purified hydrogen (400 cm^3/min). Vapor etching conditions were as follows:

Etching temperature: 800°C

Gas flow conditions: f_A - H_2 flow through $AsCl_3$ - 200 cm^3/min

f_H - H_2 flow for dilution - 200 cm^3/min

Duration: 5 minutes.

This treatment removed GaAs at a rate of ~ 0.48 mg/cm^2·min. Prior to loading the substrates, the reactor was given a thorough vapor cleaning at 850°C by diverting the H_2-$AsCl_3$ stream around the gallium melt to the doping tube. Thirty minutes was sufficient time to completely clean the deposition region of contaminants.

1.2 Epitaxial Growth and Evaluation of n-n+ Wafers

Epitaxial growth of GaAs was accomplished in an "open tube" system using $AsCl_3$ and Ga as reactant sources and H_2 as a carrier gas. This method first reported by Effer,[2] is suitable for producing high quality material for device applications. In this process, the arsenic trichloride provides both the chlorine for the gallium transport and the arsenic vapor for synthesizing gallium arsenide. The predominant vapor species and chemical reactions that are generally recognized as occurring in the high temperature gallium saturation region of the system are as follows:

$$AsCl_3(v) + 3/2H_2\,(v) \rightarrow 3HCl\,(v) + 1/4As_4(v) \qquad (1)$$

$$Ga\,(\ell) + HCl\,(v) \rightarrow GaCl\,(v) + 1/2H_2(v) \qquad (2)$$

and

$$3GaCl\,(v) \rightleftarrows GaCl_3\,(v) + 2Ga(\ell)\,. \qquad (3)$$

The deposition of GaAs downstream does not occur until the Ga(ℓ)-GaAs (s) equilibrium within the gallium melt is attained. This state corresponds to the absorption of arsenic vapors by the gallium melt until it is saturated with GaAs. Gallium arsenide will now deposit on the substrates and on the reaction tube, as the arsenic and gallium chloride vapors flow from the saturation zone along the reaction tube to a region of lower temperature.

The apparatus used for preparing epitaxial GaAs layers is shown in its own special laboratory in the photograph of Fig. 1. The reactor consists of a two-zone, 84-cm-long Kanthal wound furnace with external taps on the windings for altering the temperature profile. Temperature control in each zone is maintained by temperature controllers having a control sensitivity of ± 0.5°C. A simplified diagram of the reactor and flow system is shown in Fig. 2. At the gas exit end of the reactor the H_2 is kept ignited by a small wire heater. Details of the reaction tube are shown in Fig. 3.

The reaction tube is made of natural quartz tubing of 40-mm OD. The 50/50 standard taper joints on the ends are provided with matching Teflon sleeves. Inside the reaction tube, a quartz liner 33-mm OD is placed to collect the excess deposition products. This liner can be removed, cleaned and replaced after each deposition, or it can be kept in place with vapor cleaning for several depositions. If the liner is used repeatedly, the substrates must be protected by a quartz plate supported above to avoid surface damage caused by particles dropping from that portion of the liner extending outside the furnace

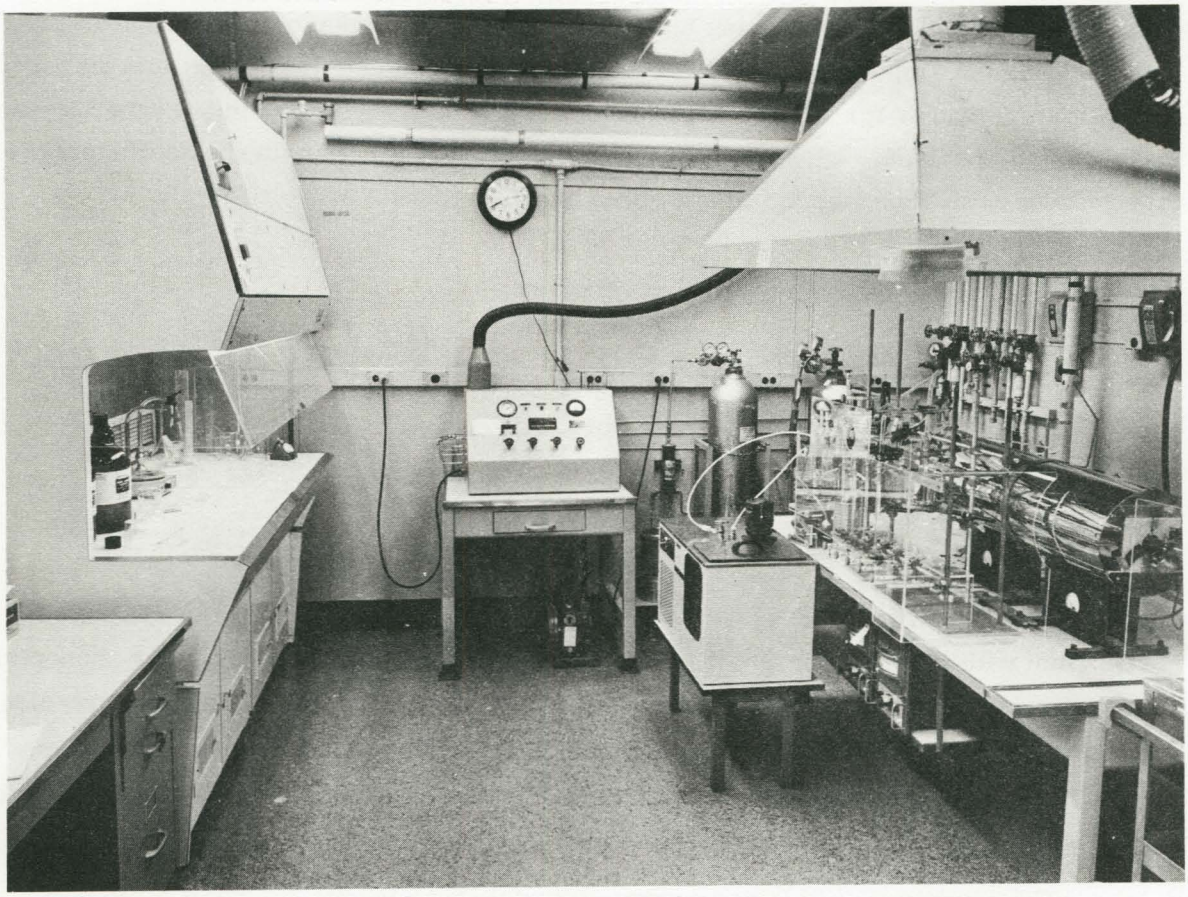


Fig. 1. General view of laboratory and epitaxial reactor facility for preparation of high-purity GaAs for Gunn devices.

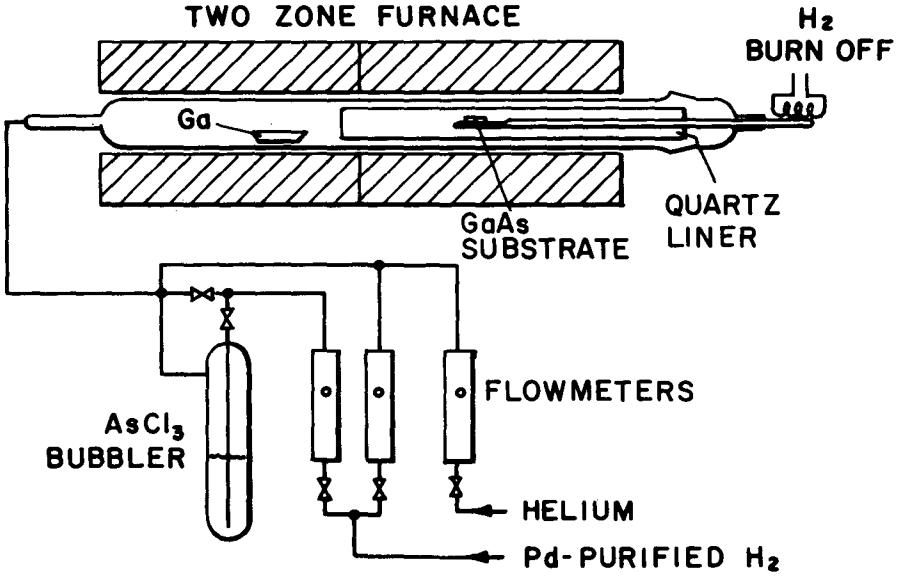


Fig. 2. Simplified diagram of epitaxial reactor and gas flow system.

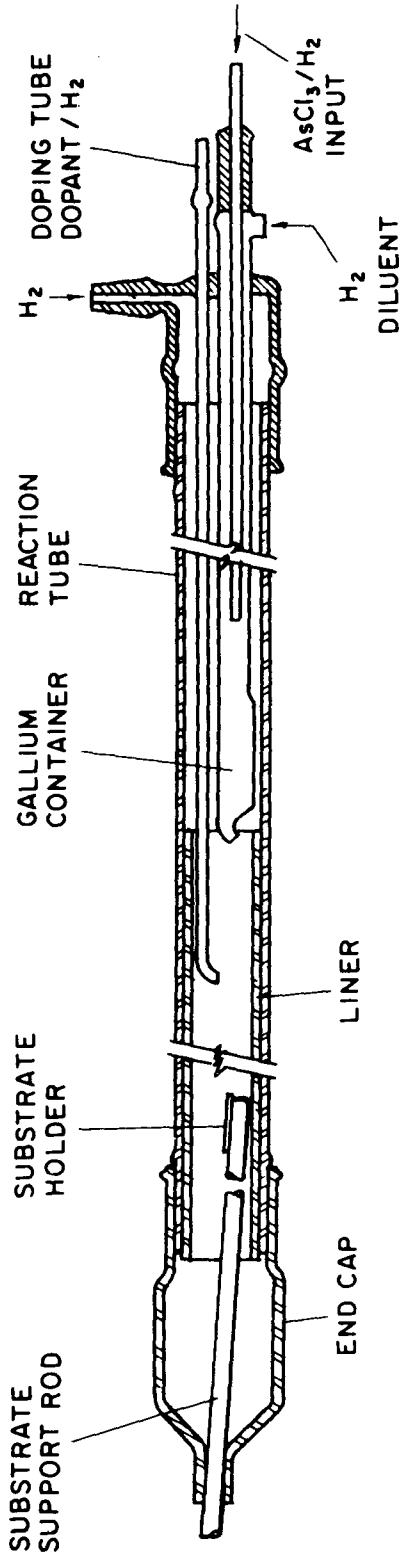


Fig. 3. Epitaxial GaAs reaction chamber.

during the loading and unloading of the wafers. The gallium receptacle is made of Spectrosil quartz and can accommodate 50 grams of gallium. The substrate support rod contains a thermocouple well which permits the temperature of each wafer to be monitored during vapor etching and growth.

Gas lines connecting the reaction chamber to several precision bore flow rate tubes are constructed of Pyrex tubing with a minimum number of Teflon O-ring compression fittings for ease of assembly.

The arsenic trichloride source is contained in a 150-gram capacity Pyrex bubbler with two teflon stopcocks appropriately placed on the bubbler so that they are not in direct line with the $AsCl_3$-saturated hydrogen gas stream and arranged so that the $AsCl_3$ may be partially or fully bypassed. The total hydrogen flow to the gallium source was fixed at 250 cm^3/min and the input arsenic-to-hydrogen ratio was varied by controlling the temperature of an ethylene glycol-water bath surrounding the $AsCl_3$ bubbler.

The gases used, gas line arrangement and purification section are shown in Fig. 4. The gas line arrangement is designed to be used in two operating modes which are: (1) a continuous flow of hydrogen is passed through the system at approximately 450 cm^3/min when the system is not in use. During this time a partial pressure of arsenic was constantly maintained over the arsenided gallium source at temperature. This was accomplished by opening only the valve connecting the downstream end of the $AsCl_3$ bubbler to the H_2 bypass lines. Although no H_2 was passed through the bubbler, enough $AsCl_3$ vapor diffused along the connecting tube to provide an adequate supply of $AsCl_3$ to the reactor; (2) A hydrogen tank source is used to insure a constant line pressure and gas flow rate to the reaction chamber during the epitaxial growth phase. Stainless-steel gas lines and valves are used between the flowmeters and both hydrogen and helium purifiers. Palladium-diffused hydrogen from the Model HPD20-150D purifier (Engelhard Industries) is continuously supplied to the system. Helium is used in certain stages of operation such as loading and unloading samples. The helium is purified by means of Deoxo purifier Model D (Engelhard Industries), a stainless-steel liquid nitrogen cold trap, and a helium purifier Model P31 (J. P. Mickel Associates).

The occurrence of an electrical power failure results in a cessation of the H_2 flow from the Pd-H_2 diffuser purifier as the Pd alloy heater cools down. To prevent the possibility of serious damage to the reactor and to preclude time consuming disassembly, clean up, reassembly run in etc. operations, a fail-safe mechanism starts a flow of pure He into the system whenever there is even a brief interruption of electrical power.

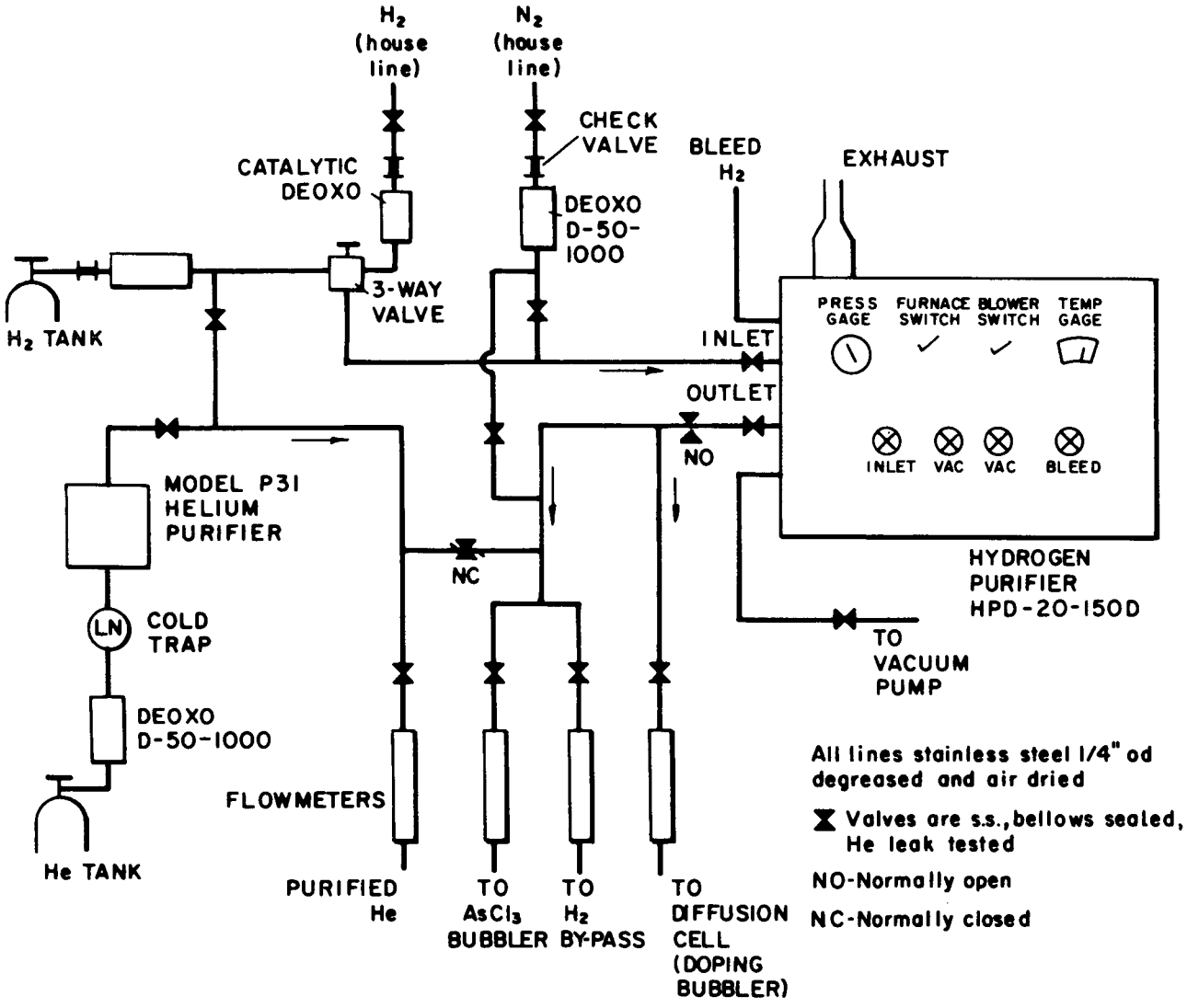


Fig. 4. Diagram of gas flow and purification system for GaAs reactor.

1.2.1 Gallium Saturation

With the furnace at room temperature, a high-purity gallium ingot is loaded into the Spectrosil quartz container under a flow of helium (5 liters/min) and H_2 (200 cm^3/min). A cleaned liner is carefully put in place in the reaction tube and the helium gas is turned off. The furnace controllers are set for the normal temperature profile and gallium saturation is started when the furnaces have reached the desired temperature. Normally, f_A is 200 cm^3/min and f_H is 200 cm^3/min. The $AsCl_3$ temperature is 27°C and the gallium temperature is 800°C. Saturation of 25 grams of gallium under these conditions takes approximately 2 hours.

After saturation, the liner is removed under a flow of helium (5 liters/min) and H_2 (450 cm^3/min), and the initial GaAs deposition point in the liner is noted. This determines the position in the reactor for the best growth on GaAs substrates, i.e., smooth surface and reproducibility in thickness. The best results to date have been obtained when the substrates are positioned in the region 2.5-cm upstream of the initial GaAs deposition point on the liner, as shown in Fig. 5. This is a region where the GaAs deposition is kinetically controlled by surface catalysis. In Fig. 6, the smoothness of the layer obtained on a substrate placed in this region is contrasted with that of a substrate positioned in an area downstream of the initial deposition point. The growth hillocks or pyramids seen in Fig. 6a are a common type of growth defect.

1.2.2 $AsCl_3$ Characterization

The quality of the $AsCl_3$ source is found to be a most important factor in determining the purity of the GaAs. When the purity of $AsCl_3$ is such as to make it possible to deposit n-type GaAs with low carrier concentration, the available analytical techniques are not able to resolve differences in various $AsCl_3$ lots. Therefore, in the selection of $AsCl_3$ lots to generate low $10^{14}/cm^3$ GaAs, the most reliable test of the quality of a given lot of $AsCl_3$ is afforded by evaluation of the GaAs made from the lot. After saturating a gallium melt with a particular $AsCl_3$ lot, the carrier concentration of the epitaxial layers in successive runs usually drops off rapidly and then levels out to some relatively constant value for a specific $AsCl_3$ temperature. This is shown in Fig. 7 for a particular $AsCl_3$ lot at 20°C. The electrical properties of epitaxial layers are strongly dependent on the temperature of the $AsCl_3$, which in turn regulates the input $AsCl_3/H_2$ mole ratio in the vapor. Therefore, when the layers are produced with a constant carrier concentration the temperature versus carrier concentration of the $AsCl_3$ is determined. In Fig. 8 data points are shown that correspond to temperatures of 0°C, 15°C, 20°C and 25°C for three different lots of $AsCl_3$. All of the GaAs epitaxial layers discussed in the following section were prepared using the three $AsCl_3$ lots shown in Fig. 8.

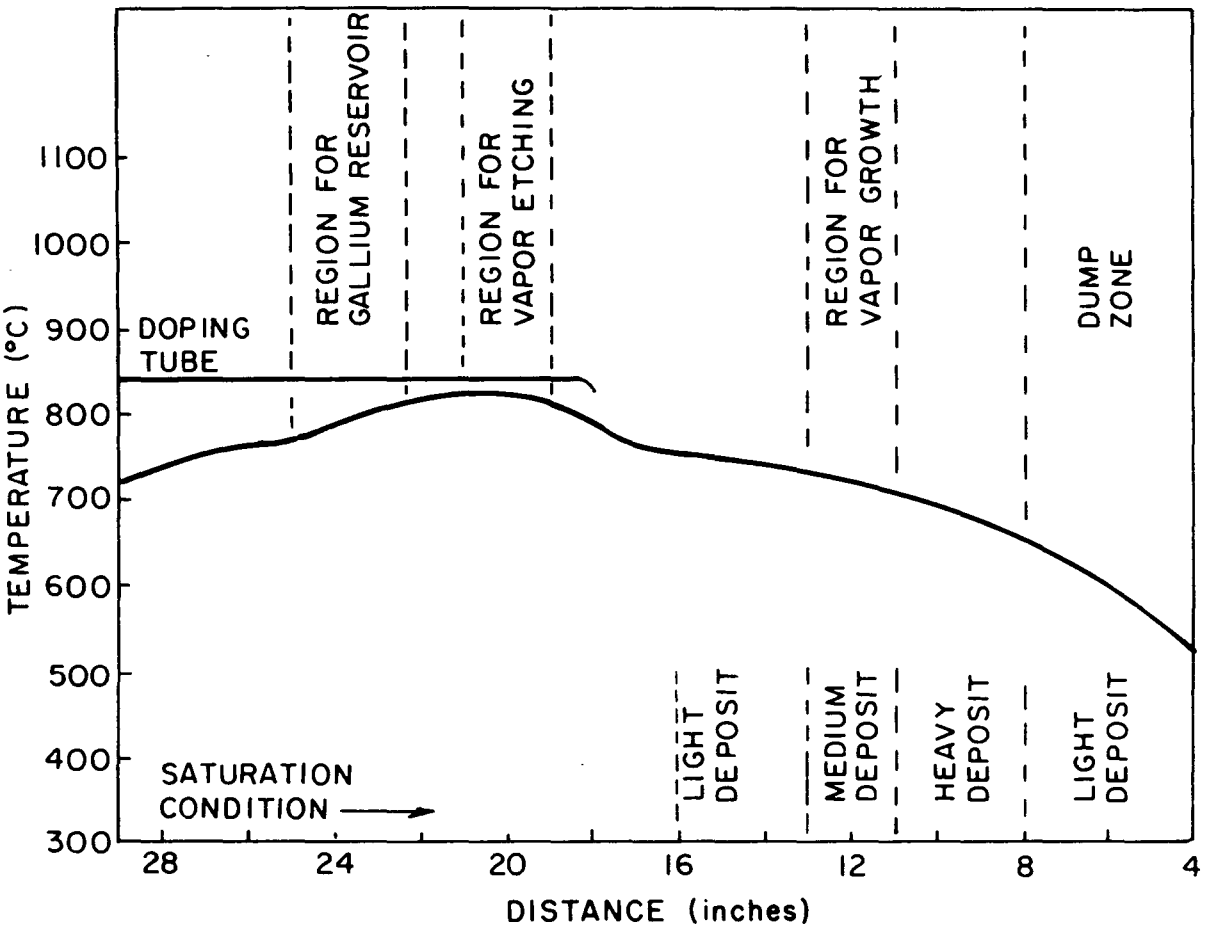
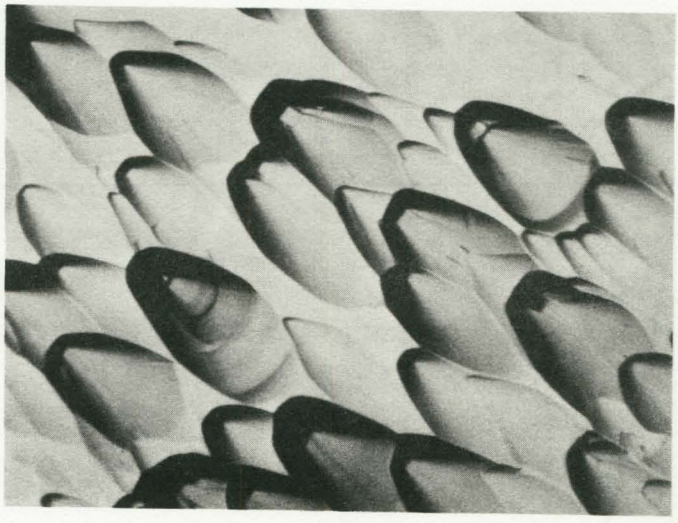
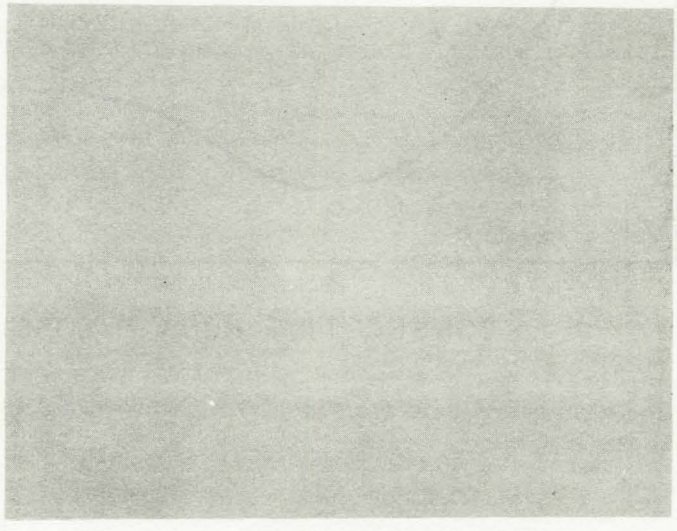


Fig. 5. Temperature profile and location of various zones during gallium saturation phase and epitaxial growth phases of operation.



(a)



(b)

Fig. 6. Two epitaxial layer surfaces prepared using the same vapor etching and growth conditions: (a) Run No. 2258 - n+ substrate GF76A (s15) in a growth area downstream of the initial deposition point (see Fig. 5); (b) Run No. 2259 - n+ substrate GF76A (s16) upstream of the initial deposition point (see Fig. 5).

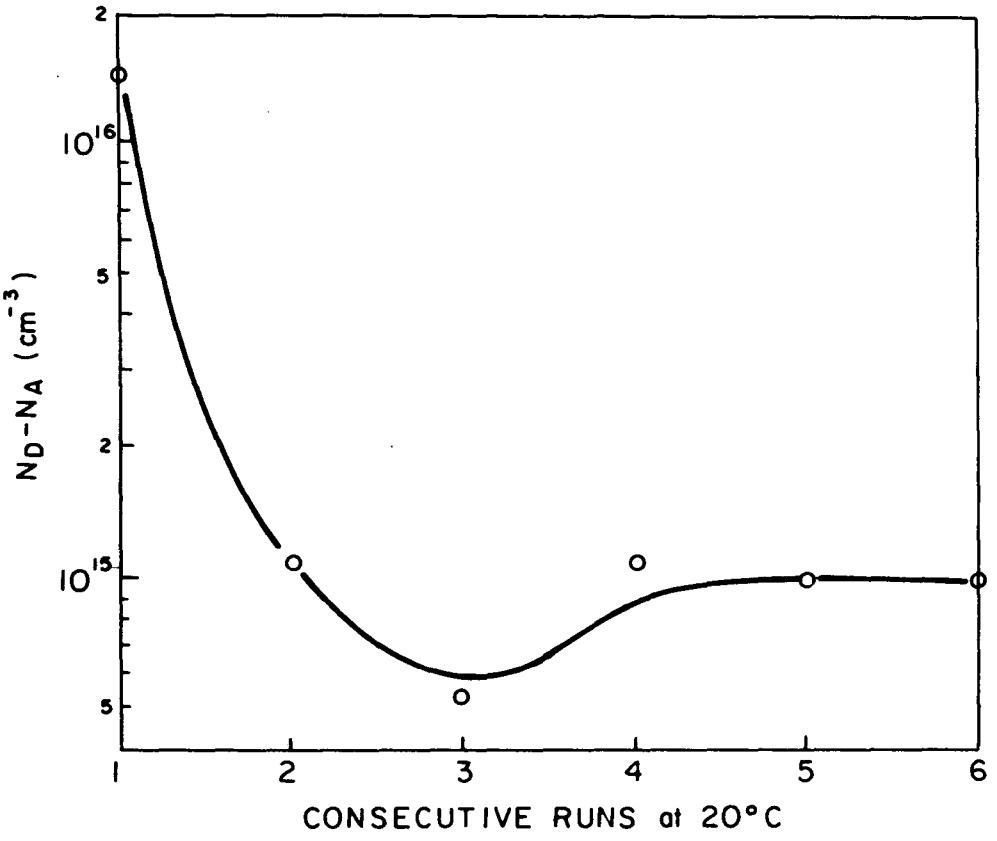


Fig. 7. Variation of carrier concentration during successive runs after initial loading with Ga and $AsCl_3$.

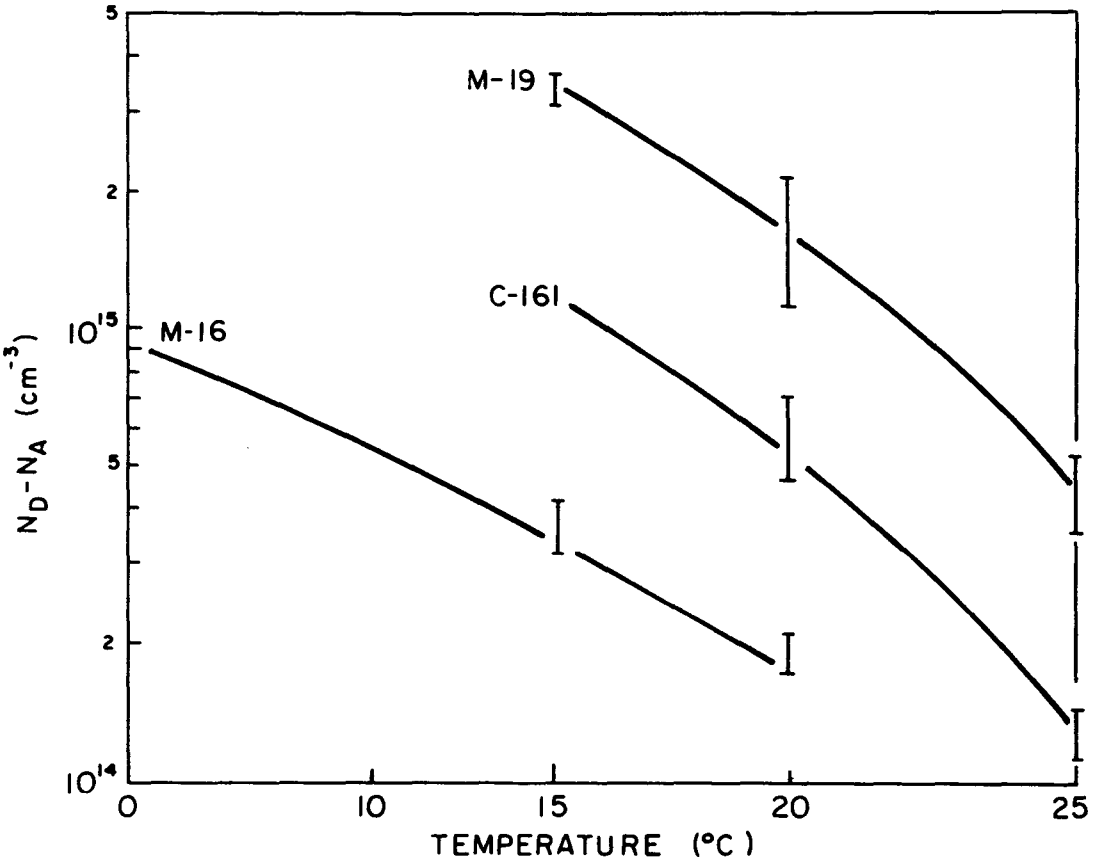


Fig. 8. Variation of free carrier concentration (N_D-N_A) as a function of $AsCl_3$ temperature for three different lots of $AsCl_3$.

1.2.3 Method of Epitaxial Layer Preparation

The substrates were loaded into the reactor and vapor etched as described in Section 2.1. This vapor etch was followed by a 10 minute purge of the reaction tube. The first five minutes was in hydrogen gas flowing at 450 cm^3/min, followed by 5 minutes in a flow of 450 cm^3/min hydrogen plus 2 liters/min of helium. The substrates were then pulled into Zone 2 of the furnace at the predetermined growth position. The helium was shut off and 10-minutes was allowed for the substrates to come to the equilibrium temperature at this position (730°C) and for the helium in the reaction chamber to be replaced with hydrogen. Epitaxial growth was then begun using the growth conditions outlined below for a (100)-oriented substrated in a 40-mm OD reaction tube.

H_2 flow through $AsCl_3$	250 cm^3/min
H_2 dilution flow	200 cm^3/min
$AsCl_3$ temperature	Determined by N_D-N_A required (see Fig. 8)
Gallium temperature	800°C
Substrate temperature	730°C to 750°C
Temperature gradient across substrates	6°C/cm to 4°C/cm

The deposition rate was usually ~ 0.2 μm/min for these conditions. When the desired growth time had elapsed, the arsenic trichloride flow was stopped by diverting the hydrogen stream to bypass the bubbler. The total hydrogen flow was still, however, maintained at 450 cm^3/min. Hydrogen was allowed to sweep the system for 10 minutes before the substrates were drawn slowly into the reaction tube cap and cooled to room temperature (15 to 20 minutes). The helium valve was opened, and the flow rate was steadily increased to 5 liters/min. The substrates were removed immediately. If the liner and support rod were not removed after each deposition, then the temperature in Zone 2 of the reactor was raised to 850°C and these parts were vapor cleaned with arsenic trichloride.

No matter how stringent or extended the chemical cleaning procedures, whenever new quartz was installed in the high temperature parts of the reactor system, an extended period of in-situ operation was usually required before the epitaxial reactor yielded high-quality GaAs.

Whenever the quality or the quantity of the $AsCl_3$ and/or the gallium had reached the point where useful material could no longer be prepared, all of the $AsCl_3$ and gallium were expended by running the reactor continuously for several days with the gallium at 850°C.

The reloading of the system was normally done in two stages. First, the furnace was allowed to cool down to room temperature in hydrogen and flushed with helium. The gas exit part of the reaction tube was closed off so that the helium flowing in the system was forced to exit through the gallium loading section, thus preventing dust and air from entering while loading. The $AsCl_3$ could be loaded at any time provided the $AsCl_3/H_2$ input tube to the gallium container was bypassed. However, the $AsCl_3$ was usually added at working temperature after the gallium had been baked out in hydrogen for at least 24 hours in situ. Before the gallium was arsenided, the $AsCl_3$ was purged with hydrogen and passed through the doping tube of the reactor for 30 minutes.

1.2.4 Evaluation

1.2.4.1 Surface Quality

By careful visual inspection of a wafer using a low power microscope when necessary, it is often possible to determine the causes of growth defects and correct them in subsequent runs. The causes of most epitaxial imperfections can usually be attributed to improper cleaning and handling of the substrates and to foreign matter introduced from the atmosphere or from the liner. Surface damage in GaAs is readily introduced after etching by handling with teflon tweezers; consequently, handling should be kept to a minimum and limited to only one corner of the substrate. The most common imperfection observed on epitaxial layers are growth hillocks or pyramids, as shown in Fig. 6a. Their presence in layers has been the subject of much discussion and may be due to several causes such as improper growth and etching conditions, substrate defects and surface damage. Using the proper conditions, a wafer is free of hillocks and exhibits a bright mirror-smooth surface (see Fig. 6b).

1.2.4.2 Junction Delineation

Metallographic techniques were used for layer thickness determinations, junction delineation and for observing extraneous layers within the epitaxial growth. The latter can be the result of impurity diffusion from the substrate or changes in gas composition during growth. For thickness determinations, a section of the wafer was cleaved along the (110) plane perpendicular to the junction. Cleavage was accomplished by placing the epitaxial layer face down on a flat surface and passing the point of a diamond scribe on the very edge of the wafer. The sample was mounted with the cleaved face along the edge of a pyrophyllite block (19 mm x 19 mm x 13 mm high) epitaxial-surface down. This was done by heating the block and applying a thin layer of wax (No. 70C cement - Hugh Courtright & Co.). The sample was pressed down and leveled so that the cleavage plane was exactly at right angles to the optical axis of the microscope.

The junction was delineated by etching with a Murakami stain. This etch consists of 10 grams of potassium ferricyanide, 10 grams of potassium hydroxide and 100 cm^3 of distilled water. The etching time was approximately 10 seconds, depending on the dopant and doping concentration in the substrate. This etch was preferred to the strong oxidizing solutions normally used, because the GaAs was not severely attacked when it was left in contact with the etch for long periods of time. The junction between the substrate and deposit was revealed as a very distinct line. With very few exceptions, the interface was extremely flat along the section taken for measurement. Figure 9 is an example of a 10 μm-thick n-type layer on an n+ Si-doped GaAs substrate. The stain can also be used on n-i samples to measure the layer thickness needed for calculating the Hall effect. The epitaxial layer thickness was measured directly with a Zeiss metallurgical microscope equipped with a calibrated eyepiece. Layer thickness could be determined to within 1 μm using this method.

Nondestructive determination of thickness and thickness uniformity of epitaxy layers was accomplished by recording the infrared reflectivity spectrum between 2.5 and 20 μm.[3] Infrared measurements were made using a Beckman IR 10 grating infrared spectrophotometer.

1.2.4.3 Electrical Evaluation

Layers grown on semi-insulating substrates were evaluated using the Van de Pauw method. For this measurement, a portion of the sample was cleaved into a symmetric piece approximately 6 mm square.

The contacts to n-type GaAs were made by alloying tin dots (0.75 mm in diameter) to the surface in a hydrogen atmosphere. A cleaned sample was placed on a quartz plate with the epitaxial layer up and a tiny drop of reagent grade 37 percent HCl solution added to the surface at the four corners. The tin dots were placed directly onto the HCl drops, which served to clean the dots and promote wetting when heated. The quartz plate was pushed carefully into position in the tube and the system was purged by flowing nitrogen for one-half hour. Pure hydrogen was introduced and after 10 minutes the furnace was turned on. The temperature was raised rapidly (20°C/min) to 400°C and the sample left at this temperature for one minute. The power input to the furnace was manually reduced, and the system was cooled slowly to 100°C in approximately 30 minutes. Nitrogen gas replaced the hydrogen in the system before the removal of the sample. Deep penetration of the tin into the (100) oriented sample was not observed under these conditions and strong metallurgical bonds with good ohmic properties were obtained. Copper wires 0.05 mm in diameter were carefully attached to the tin dots with a hot soldering iron and the other ends

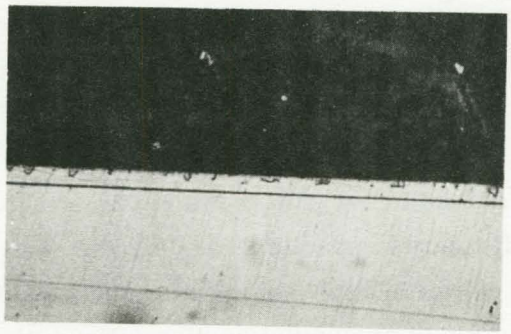


Fig. 9. Sample No. 2440 - GaAs n-n+ structure cross-sectioned and etched with Murakami stain. (250X)

of the wires soldered to heavy leads mounted on a special sample holder to secure the samples in place for electrical measurements.

The Van der Pauw technique that was used in making dc Hall effect and resistivity measurements is well described in the literature.[4] The measurements were carried out with the Hall probe mounted in a dewar. Routinely, Hall coefficient (R_H) and resistivity (ρ) measurements were made at room temperature and at liquid nitrogen temperature (77°K). The current (I) through the sample was kept as small as possible ($\sim$ 1 mA) to avoid resistive heating.

The Hall effect measurement gives the average mobility and carrier concentration in the n-layer grown on a semi-insulating GaAs substrate. However, it is known that the behavior of semiconductor devices and particularly of Gunn devices is related more closely to the doping profile of the semiconductor material used in the devices realization. Measurements of the junction capacitance of a Schottky barrier provide a means of determining the doping profile within a epi-layer as well as the doping variations over the surface of a n-n+ wafer through the "differential capacitance technique" first derived by Hillibrand and Gold.[5] In the differential capacitance measurement, the capacitance of a Schottky barrier diode is measured as a function of an applied dc bias. From these data and the diode area. the carrier concentration as a function of depth below the epi-surface is calculated from

$$N_{(X)} = \frac{C^3}{K\epsilon_o qA^2} \frac{dV}{dC}$$

and

$$X = \frac{K\epsilon_o A}{C}$$

where

$N_{(X)}$ is the carrier concentrations in carriers/cm^3 at a point X micrometers from the Schottky contact

C is the diode capacitance in $\mu\mu F$

A is the junction area in cm^2

K is the dielectric constant of the semiconductor

ϵ_o is the dielectric permittivity of vacuum

q is the electronic charge, and

V is the applied bias in volts.

An IBM 360 computer with a Cal Comp 703 plotter was used for the calculations and for automatic plotting of dopant profiles. The program in this case computes the derivative, dV/dC, by fitting three consecutive points to a parabola and finding the tangent at the middle point. This technique produces a profile point for each C-V data point.

Figure 10 is an oscillogram of the current-voltage characteristics of a Schottky diode deposited on wafer 2419;t = 4.9 μm, $n = 1.3 \times 10^{15}/cm^3$. A sharp breakdown voltage of about 82 volts was obtained which agrees with the expected theoretical breakdown voltage for an abrupt junction in a 5 micrometer thick epitaxial layer in GaAs of $n = 1.3 \times 10^{15}/cm^3$. The forward characteristics is exponential and may be described by the familiar equation

$$I_f = I_s \left(e^{\frac{qV}{\eta kT}} - 1 \right) .$$

The numerical value of η indicates the degree to which the current-voltage characteristic approached that of an ideal diode, i.e., at voltages less than the built-in junction potential the current flow is by cross-diffusion of electrons and holes and $\eta = 1$. A value of η close to unity indicates that the contribution to the capacitance from semiconductor surface states is small.[6] Figure 11 shows the forward log-current-voltage plot for sample 2419 from which an η value of 1.02 was obtained.

1.3 Epitaxial Growth and Evaluation of n++-n-n+ Wafers

Epitaxial n++-n-n+ structures were prepared by growing n++ layers onto previously prepared n-n+ wafers. For this purpose a separate vapor phase epitaxy system similar to that used for growth of n-layers was employed. A bubbler which was connected to the main $AsCl_3/H_2$ line downstream of the $AsCl_3$ bubbler was charged with S_2Cl_2 as a source of sulfur. Sulfur is a highly soluble donor impurity in GaAs. The liquid S_2Cl_2 was maintained at room temperature. In operation it was not necessary for the doping gas stream to be bubbled through the liquid to achieve the desired result. Instead, diffusion of S_2Cl_2 vapor along the tubing connecting the bubbler to the $AsCl_3/H_2$ line was sufficient to produce heavily doped layers.

The procedures for start up, gallium saturation, sample handling, etc. were the same as those followed for n-layer growth except for the following details.

1. Neither chemical nor vapor phase etch cycles were employed during wafer preparation, or during predeposition procedures. The n-n+ wafers were cleaned just prior to growth by a rinse in dilute HCl, followed by successive rinses in H_2O, CH_3OH and freon.

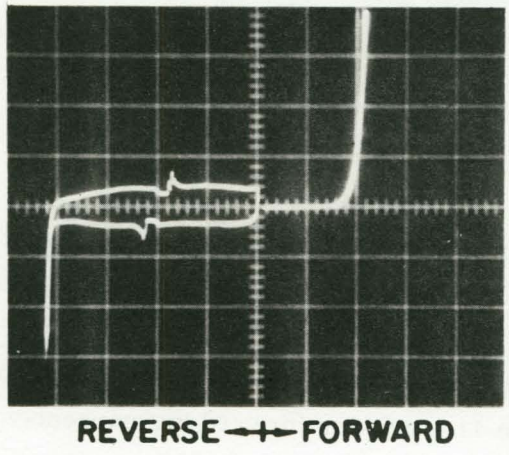


Fig. 10. Oscillograms of current voltage characteristics of Schottky barrier diode for Sample No. 2419 ($n = 1.3 \times 10^{15}/cm^3$). Forward bias; vertical 0.01 ma/div., horizontal 0.2 V/div: reverse bias; vertical 0.01 ma/div., horizontal 20 V/div. Reverse breakdown at 82 volts.

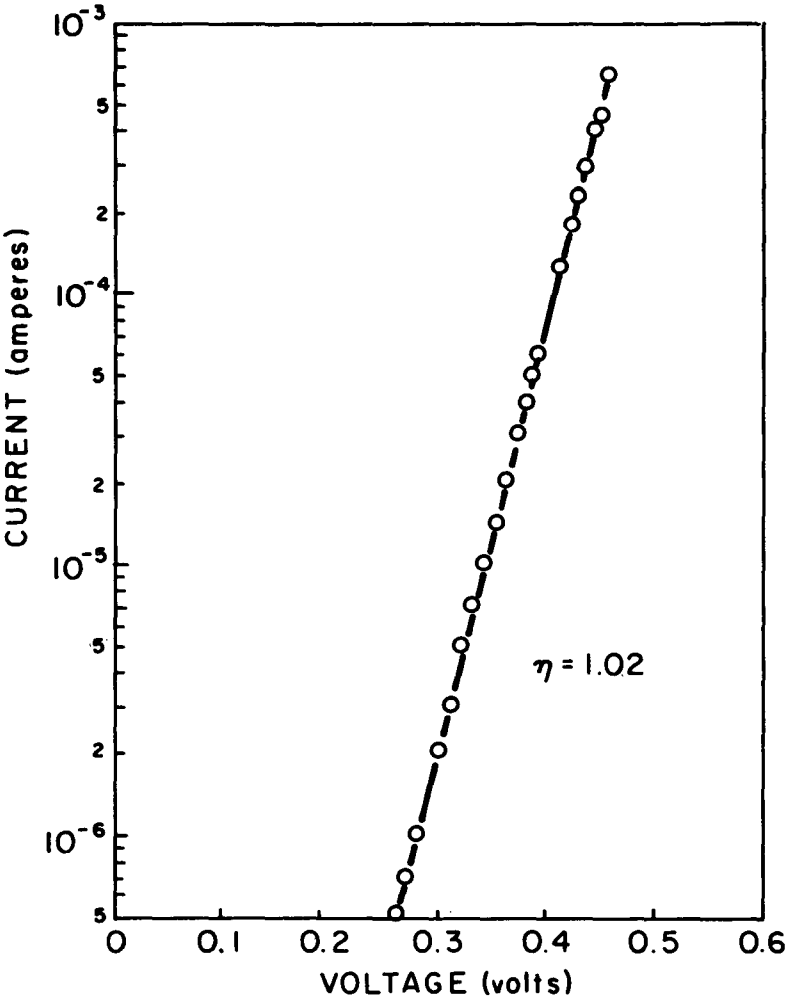


Fig. 11. Forward current-voltage characteristic of a Schottky barrier diode.

2. To initiate growth, the $AsCl_3$ and S_2Cl_2 valves were opened. The gas flow through the doping line was kept at 50 cm^3/min, the gas flow through the $AsCl_3$ bubbler was 200 cm^3/min and the total system flow was 500 cm^3/min. A period of 15 minutes was required to produce n++ layers several micrometers thick.

Evaluation of n++-n-n+ wafers for surface quality, and the use of cleave and stain procedures, etc. was as described previously.

The free carrier concentration in the n++ layer was deduced by measurement of the position of the plasma-resonance minimum in the infrared reflectivity spectrum.[7] As a check on the accuracy of this method of measuring the doping level a number of runs were made with Cr-doped (insulating) wafers in the system. The comparison of free carrier concentration determined from Hall effect measurements made on n++-i wafers and the free carrier concentration deduced from the position of the infrared plasma resonance is shown in Table I.

2. EXPERIMENTAL RESULTS AND DISCUSSION

During the vapor phase epitaxy of GaAs several critical effects of process parameters on electrical properties, growth rate and surface quality were studied in detail. These are summarized below.

At substrate temperatures in the range 700°C to 750°C the free-carrier concentration in an epitaxial layer can be varied approximately one order of magnitude by a 0°C to 25°C change in the $AsCl_3$ temperature. High $AsCl_3$ input concentrations (high $AsCl_3$ temperatures) yielded high resistivity material. The growth rate is not strongly affected by an $AsCl_3$ temperature change and surface smoothness improves as the $AsCl_3$ temperature is reduced.

As the gallium temperature is raised from 800°C to 900°C at constant input $AsCl_3$ concentration, the free carrier concentration increases and the Hall mobilities at room temperature and 77°K tend to be high. The growth rate and epitaxial surface imperfections increase as the gallium temperature is raised.

With increasing temperature above 700°C the free carrier concentration in the n-layers decrease and Hall mobilities at room temperature and 77°K increase. At a particular substrate temperature, however, depending on the gallium temperature and $AsCl_3$ concentration, the mobilities begin to decrease as n decreases and the resistivity rises rapidly. At 750°C and above, changes in $AsCl_3$ temperature have little or no effect on electrical properties. Normally, at substrate temperature above 750°C the GaAs is high

TABLE I

The Free Electron Concentration in n++ Layers Measured by the Infrared Reflectivity Technique and the Hall Effect Technique

	Carrier Concentration, cm^{-3}	
Sample No.	by IR Reflectivity	by Hall Measurement
3118	5.2×10^{18}	6.2×10^{18}
3119	5.2×10^{18}	5.9×10^{18}
3120	5.7×10^{18}	6.8×10^{18}
3122	4.5×10^{18}	6.1×10^{18}

resistance or p-type. The growth rate increases with substrate temperature in the 700°C to 750°C range. The epitaxial layer surface becomes progressively better as the substrate temperature increases.

The gas flow rate of $AsCl_3$ saturated hydrogen is determined by the geometry of the gallium container and reaction tube. If the flow is too rapid the Ga-GaAs equilibrium in the melt is not attained and no epitaxial growth occurs. Unreacted HCl at high $AsCl_3$ concentration and high gas flow will in fact etch the substrates away. High flow rates also cause poor thickness uniformity.

Based on these effects appropriate adjustments were made in the various growth parameters to obtain a high yield of device quality GaAs.

For epitaxial layers prepared during the contract period the reactor temperature profile and positions of source and substrate shown in Fig. 5 were used. Also shown is the relative deposit buildup on the liner after the gallium was arsenided. All of the epitaxial wafers grown can be divided into three groups according to the $AsCl_3$ batches that were used to produce them.

The first group of wafers was produced using $AsCl_3$ from batch M-19 ($AsCl_3$ charges A, B and C in Table II). Eleven of these wafers were acceptable and their properties are listed (Samples 2369-2402). This group was notable for the somewhat low mobility values measured at 77°K. Only one sample possessed a charge carrier mobility above 50,000 $cm^2/V \cdot sec$ at liquid nitrogen temperature. Free carrier profiles determined from capacitance-voltage measurements of samples from runs 2369 and 2384 are shown in Figs. 12a and 12b. Representative wafers were selected from each series of runs for detailed evaluation by capacitance-voltage measurements. The rather high $AsCl_3$ temperatures that were necessary to obtain low free carrier concentration from this batch of $AsCl_3$ made precise control of layer properties difficult. All of the $AsCl_3$ and gallium remaining after run No. 2402 were expended by running the reactor continuously for several days.

A new charge of 50 grams of gallium was placed into the system and a new charge of $AsCl_3$ from batch M-16 was introduced into the bubbler. The $AsCl_3$ characterization curve for this lot is shown in Fig. 8. From this curve, it appeared that better control of carrier concentration in the epitaxial layers would be possible because of the low temperature range available. In addition, it was expected that surface smoothness should improve at the lower input $AsCl_3$ concentrations. The thirteen wafers with $n\ell$ products in the range of 3.2×10^{11} to 9.9×10^{11} cm^{-2} that were delivered to NASA-Goddard in the

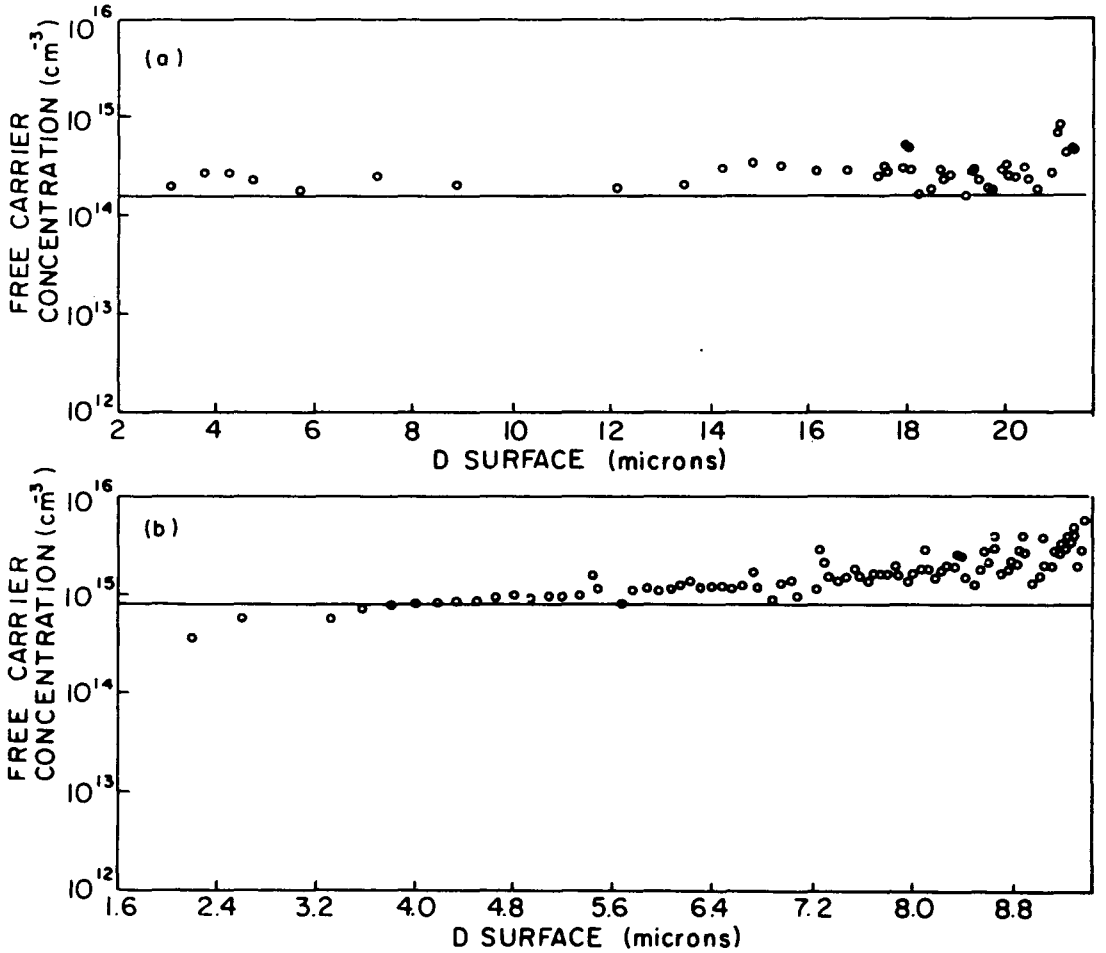


Fig. 12. Profile of the free carrier concentration in wafers prepared from $AsCl_3$ lot M-19: (a) 20 μm thick; (b) 10 μm thick layer. The solid horizontal line in this and in the following profiles represents the average free carrier concentration calculated from Hall effect measurements on companion n-i wafers.

M-16 series are listed in Table II ($AsCl_3$ charge D). Wafers Nos. 2409 through 2412 were grown to satisfy a part of Schedule 3 in the Objective. The 2-μm increments in thickness corresponded to increments in growth time of 15 minutes, and the 18-μm layer represented a total growth time of one hour and 45 minutes. As the $AsCl_3$ and gallium sources became depleted, adjustments in the growth conditions were made from run to run. In general, a decrease in the carrier concentration of the grown layer was compensated by a decrease in the $AsCl_3$ temperature and/or by a decrease in the substrate temperature.

As can be seen in Table II, only two of these samples had 77°K mobility significantly below 50,000 $cm^2/V \cdot sec$ in contrast to the results from the M-19 $AsCl_3$ series. The impurity profile for one of these samples is shown in Fig. 13. Of primary concern in these measurements was the presence or absence of gross irregularities in the profile that would cause problems in the device performance. Since the $AsCl_3$ was used for in situ vapor etching of the substrates and cleaning the liner in the area of vapor growth after each run, the 50 gram (23 cm^3) $AsCl_3$ source was rapidly depleted. The last two wafers prepared (2425 and 2426) from M-16 had epitaxial layers that were over 12 μm thick but electrically they were high resistance. Again, the remaining $AsCl_3$ and gallium were expended by prolonged operation of the system.

The reactor was recharged with 100 grams of $AsCl_3$, lot No. C-161 and 50 grams of gallium. The characterization curve for this $AsCl_3$ lot indicated that it was of intermediate quality. The samples listed in Table II $AsCl_3$ charges E and F were obtained from this lot of $AsCl_3$. To produce material in the low $10^{14}/cm^3$ range, it was necessary to operate with an $AsCl_3$ temperature of 20°C except after gallium was added or when the liner was replaced after cleaning. In this case, the temperature was raised to 25°C for the first run. It was observed in making this series of runs that when the amount of gallium source was low, the $AsCl_3$ temperature had to be steadily reduced from 20°C to 0°C to remain in the $10^{14}/cm^3$ range (runs 2453-2463). High resistivity material resulted when the conditions of growth were such that the quantity of $AsCl_3$ in the bubbler was so low that there was incomplete saturation of hydrogen with $AsCl_3$ vapors and the $AsCl_3$ temperature was less than 10°C.

Samples 2453 to 2468 were prepared without removing the liner or substrate support rod for solution cleaning. Only in-situ vapor cleaning of these parts was performed. This procedure resulted in several layers with mobilities at 77°K greater than 90,000 $cm^2/V \cdot sec$. Sample 2457 was one of the wafers in this series of runs that was selected for C-V profiling. A cleaved cross section of the n-n+ wafer indicated the epitaxial layer

TABLE II

Data on the Preparation and Properties of the n-n+ Wafers Delivered to NASA-Goddard

Sample No.	Temp. of $AsCl_3$ °C	Temp. of[a] Substrate °C	$AsCl_3$ Charge	Gallium Charge	Liner No.	Thickness μm	n, $10^{14}cm^{-3}$	μ, $cm^2/V \cdot sec$ 300°K	μ, $cm^2/V \cdot sec$ 77°K
2369	20	755	A	A	1	20	1.7	7200	68,000
2383	25	730	B	B	2	6	3.5	8300	32,000
2384	25	730	B	B	2	10	8.0	6300	40,000
2385	25	730	B	B	2	12	5.2	6300	32,000
2393	25	730	C	C	3	9	12.2	6500	23,000
2394	25	730	C	C	3	10	16.8	6500	42,000
2395	25	750	C	C	3	8	5.5	6400	40,000
2396	25	750	C	C	3	7	4.4	6100	36,000
2400	20	730	C	C	4	6	3.7	7000	47,000
2401	15	730	C	C	4	6	8.6	6400	36,000
2402	20	730	C	C	4	8	11.5	6000	39,000
2406	25	750	D	D	5	6	4.3	6300	50,000
2408	20	750	D	D	5	11	8.7	7200	62,000
2409	20	750	D	D	5	12	4.0	6300	50,000
2410	20	750	D	D	5	14	2.0	6500	67,000
2411	15	750	D	D	5	16	6.0	6400	68,000
2412	15	750	D	D	5	18	1.7	7000	90,000
2414	10	750	D	D	5	11	2.6	6300	46,000
2416	0	730	D	D	5	17	9.3	6200	56,000
2417	0	730	D	D	6	11	9.2	6200	46,000
2418	10	730	D	D	6	11	8.6	6100	50,000
2421	20	750	D	D	6	16	2.0	7400	93,000
2423	15	750	D	D	6	14	3.4	7100	73,000
2424	15	750	D	D	6	13	3.3	6000	52,000
2428	25	750	E	E	7	13	4.0	6100	65,000
2429	20	750	E	E	7	7	8.5	6000	60,000
2433	25	750	E	E	8	11	2.7	6000	67,000
2434	20	750	E	E	8	11	6.4	6000	57,000
2439	20	750	E	E	9	9	7.0	6500	48,000
2440	20	750	E	E	9	10	9.8	6400	57,000
2441	20	750	E	E	9	16	4.9	6400	60,000
2442	20	750	E	E	9	13	9.7	6000	46,000
2443	25	750	E	E	9	11	1.1	7500	75,000
2444	20	750	E	E	9	12	7.6	6300	49,000
2446	20	750	E	E	9	12	7.6	6300	49,000
2447	20	750	E	E	9	10	7.0	6500	48,000

TABLE II (Continued)

Sample No.	Temp. of $AsCl_3$ °C	Temp. of[a] Substrate °C	$AsCl_3$ Charge	Gallium Charge	Liner No.	Thickness μm	n, $10^{14}cm^{-3}$	μ, $cm^2/V \cdot sec$ 300°K	77°K
2448	20	750	E	E	9	12	4.9	6300	60,000
2449	20	750	E	E	9	10	9.6	6100	47,000
2453	20	750	E	E	10	12	1.0	7200	56,000
2454	15	750	E	E	10	16	3.2	6000	72,000
2455	20	750	E	E	10	10	1.1	7100	56,000
2456	15	750	E	E	10	12	3.2	6100	72,000
2458	15	750	E	E	10	15	2.3	6000	67,000
2459	15	750	E	E	10	16	2.7	6000	54,000
2460	10	750	E	E	10	20	1.9	6700	91,000
2461	5	750	E	E	10	20	1.4	6300	91,000
2462	0	740	E	E	10	17	1.8	7000	72,000
2463	0	730	E	E	10	8	3.4	6900	70,000
2464	15	750	E	E	10	18	2.3	6100	67,000
2465	15	750	E	E	10	14	2.8	6000	54,000
2466	10	750	E	E	10	14	2.0	6500	90,000
2467	5	750	E	E	10	10	1.7	6400	91,000
2468	0	740	E	E	10	11	2.0	6900	73,000
2470	20	750	E	F	11	40	7.9	6900	69,000
2471	20	750	E	F	11	32	1.5	6300	101,000
2472	10	750	E	F	11	36	1.9	7200	95,000
2474	10	750	E	F	12	38	2.2	6200	82,000
2478	20	750	E	F	13	22	5.0	7100	57,000
2481	25	750	F	F	13	20	5.3	6500	54,000
2482	25	750	F	F	13	24	4.6	7000	62,000
2484	25	750	F	F	13	26	1.8	7600	79,000
2489	20	750	F	G	14	28	3.3	6700	72,000
2490	15	750	F	G	14	34	4.9	6000	79,000
2491	10	750	F	G	14	30	3.5	6600	87,000

(a) Temperature gradient at 750°C = 4°C/cm; 740°C = 5°C/cm; 730°C = 6°C/cm

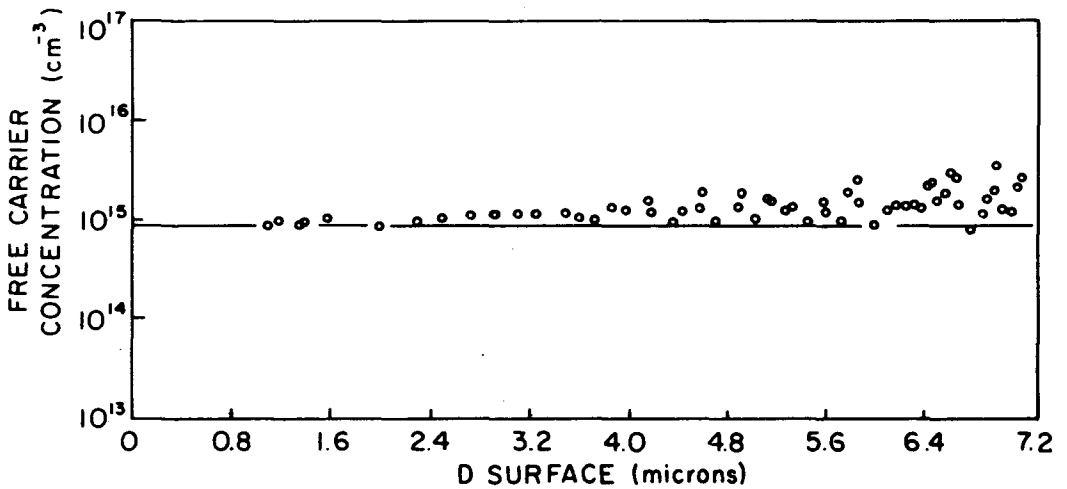


Fig. 13. Profile of the free carrier concentration in wafer typical of lot M-16. The n-layer thickness is 11 μm.

thickness was 12 μm. Hall measurements on the n-i sample gave an n value of 1.23 x 10^{15}, and mobilities of 6600 and 48,000 at room temperature and 77°K respectively. The impurity profile of a part of the n-n+ sample on which was fabricated Schottky barrier diodes is shown in Fig. 14. It can be seen that the profile is reasonably flat and uniform with no major impurity variations throughout the layer. There is also good agreement of depletion depth with the thickness measurement and of the average free carrier concentration calculated from the Hall data on the n-i sample with the C-V profile.

Epitaxial layer thickness was determined on four areas of a sample as shown in Fig. 15. In Table III, it can be seen that the thickness uniformity in these epitaxial layers increased as the temperature gradient across the substrate decreased (Samples 1, 2 and 3). Also, the growth rate increased as the substrate temperature was raised. The arsenic trichloride temperature does not appear to significantly affect the growth rate. However, the thickness gradient across the layer does increase as the $AsCl_3$ temperature decreases (Samples 3, 4 and 5). Each of these samples was approximately 8.6 cm^2 in area. With the present reactor design the temperature gradient across the substrate could not be varied independently of the substrate temperature, without causing undesirable large changes in the wafer location, or in the gallium temperature. Thus it is noted that the lower the temperature gradient, the higher is the substrate temperature.

Twenty-five of the wafers prepared in the M-16 and C-161 series were n++-n-n+ sandwich structures. The highly doped n++ GaAs layer in these wafers was normally in the range of 2 μm to 4 μm thick as measured on a cleaved and stained cross section. The doping level of the n++ layers ranged from a high of 6.89 x 10^{18}/ cm^3 to a low of 2.15 x $10^{18}/cm^3$ as determined from the infrared reflectivity plasma minima. Table IV is a list of wafers that have the n++-n-n+ structure with the doping level and thickness of the n++ layer.

3. SUMMARY AND CONCLUSIONS, AND RECOMMENDATIONS FOR FUTURE WORK

A careful detailed series of epitaxial growth runs, using an "open tube" vapor-phase system with $AsCl_3$, Ga and H_2 have been carried out to prepare GaAs wafers suitable for Gunn effect devices. Extensive data have been gathered showing that there are several system variables that are of critical importance in effecting control over electrical properties, thickness and surface quality. The $AsCl_3$ temperature, the gallium temperature, and the substrate temperature all have an effect on electrical properties as well as on epitaxial surface quality. Extreme care is required in processing substrates just prior

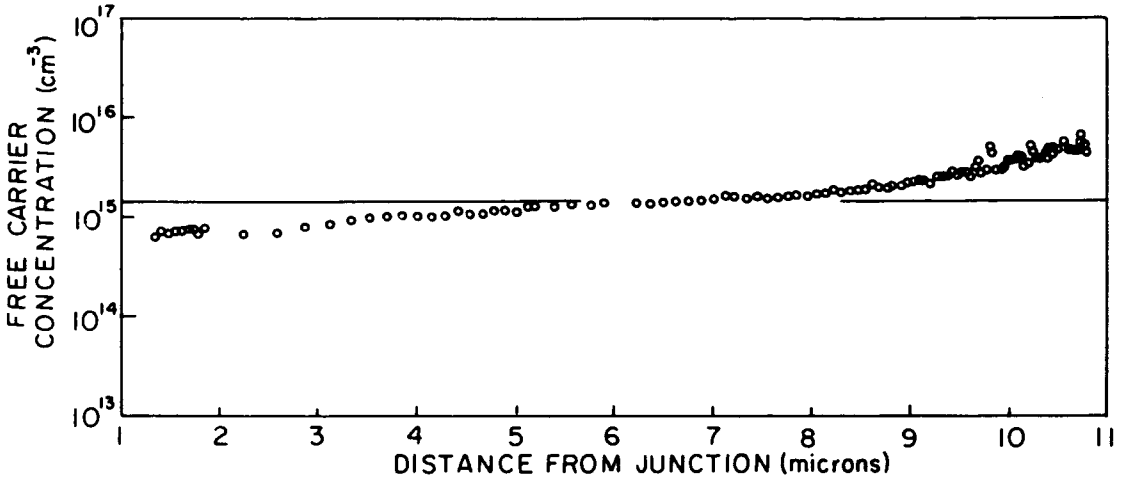


Fig. 14. Profile of the free carrier concentration in a wafer typical of those prepared from $AsCl_3$ lot C-161. The n-layer thickness is 12 μm.

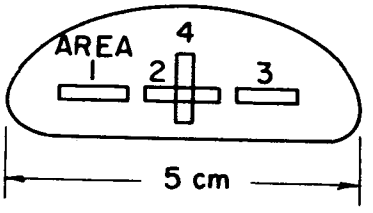


Fig. 15. Location and size of areas sampled by infrared measurements for nondestructive determination of n-layer thickness uniformity in n-n+ wafers.

TABLE III

Data on the Preparation and Properties of n-n+ Wafers Grown to Determine Thickness Uniformity

Sample No.	$AsCl_3$ Temp., °C	Substrate Temp. °C	Temp. Gradient Across Substrate °C/cm	Epi-Layer Thickness Gradient μm/cm	Sample Area	Thickness μm	Average Thickness μm
1	0	730	6	0.93	1	12.1	9.7
					2	9.6	
					3	7.5	
					4	9.4	
2	0	740	5	0.698	1	12.9	11.0
					2	11.3	
					3	9.4	
					4	10.2	
3	5	750	4	0.6	1	17.5	15.8
					2	15.6	
					3	14.6	
					4	15.5	
4	10	750	4	0.52	1	19.5	17.7
					2	17.7	
					3	16.9	
					4	16.8	
5	15	750	4	0.43	1	17.4	16.3
					2	16.0	
					3	15.2	
					4	16.4	
6	15	750	4	0.44	1	15.2	14.1
					2	13.8	
					3	13.0	
					4	14.2	
7	20	755	2		1	23.6	23.0
					2	22.9	
					3	22.6	

TABLE IV

Samples with n++-n-n+ Structures

Sample No.	n++, 10^{18} cm^{-3}	Thickness (μm)
2414	5.0	2
2416	4.8	3
2417	6.9	6
2424	4.4	4
2441	5.0	5
2442	4.9	10
2443	6.2	2
2444	6.9	3
2446	6.9	4
2448	5.0	2
2449	4.9	3
2453	4.7	2
2454	5.0	3
2455	4.7	2
2456	5.0	2
2458	4.9	4
2459	4.4	2
2460	3.2	2
2461	2.1	3
2462	5.2	2
2464	4.9	3
2465	4.4	4
2466	3.2	3
2467	2.1	3
2468	5.2	2

to epitaxial growth to assure the exclusion of surface contaminants and to produce layers with highly smooth surfaces. Only the highest purity chemicals may be used for pre-deposition processing and the water used must be highly pure (preferably 12 megohm·cm to 18 megohm·cm).

By proper qualification and selection of $AsCl_3$ batches it was shown to be possible to control the free carrier concentration from about the mid $10^{13}/cm^3$ range to about the middle of the $10^{15}/cm^3$ range. Capacitance-voltage measurements were used to construct profiles of the free carrier concentration through the thickness of epitaxial layers. These profiles consistently showed the absence of undesirable "dips" in the distribution of free charge carriers through the n-layers.

In the final analysis, a materials preparation program of this kind cannot be fully judged until measurements of operating devices are shown to be consistent with measurements of the materials properties. Thus it is recommended that a careful correlation of device performance and materials properties be conducted. This is particularly important in the present case because of the detailed information that is available for each wafer.

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