ELECTRONICS IMPLEMENTATION OF THE SOLAR NEUTRON EXPERIMENT DECEMBER 1970

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1. Introduction

This report describes the functioning of the electronics used in the neutron counter experiment. The overall system block diagram (Fig. 1) shows the electronics assembled on various boards. On the pages that follow the boards will be discussed individually.

Functional block diagrams have been omitted from this report as they appear in Section 1.1 Experiment 1 of the Themis Renewal Proposal, December 14, 1970. That proposal gives an overall functional electronics description of the experiment while the operating details are given here.

2. S_1, S_2 Adder Boards

The S_1 and S_2 Adder Boards that are connected to the S_1 and S_2 photomultiplier tube outputs (16 total), perform three main functions: (1) linear, passive addition of the photomultiplier tube outputs, (2) singles rate monitoring and (3) scintillation cell identification. A brief description of each follows. See Figs. 2 to 5.

A. Adders. Passive adders were selected to satisfy the requirements of a large linear dynamic range of 100:1, isolation greater than 100:1 and fast pulse rise time. Signals are added two at a time, with hybrid transmission line transformers. They are constructed from very high permeability (μ= 5000) ferrite cores on which are wound the parallel wire transmission lines twisted in bifilar

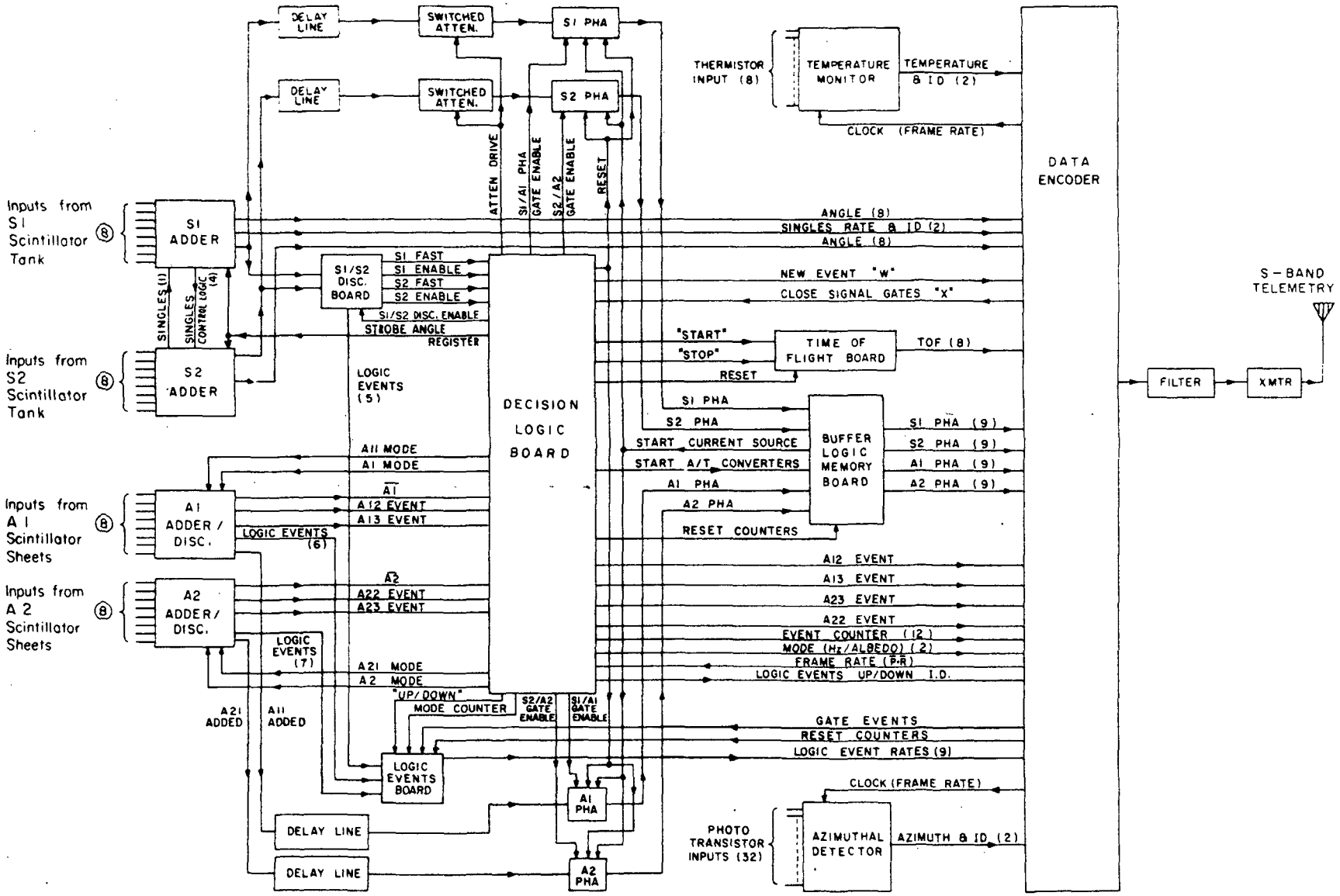
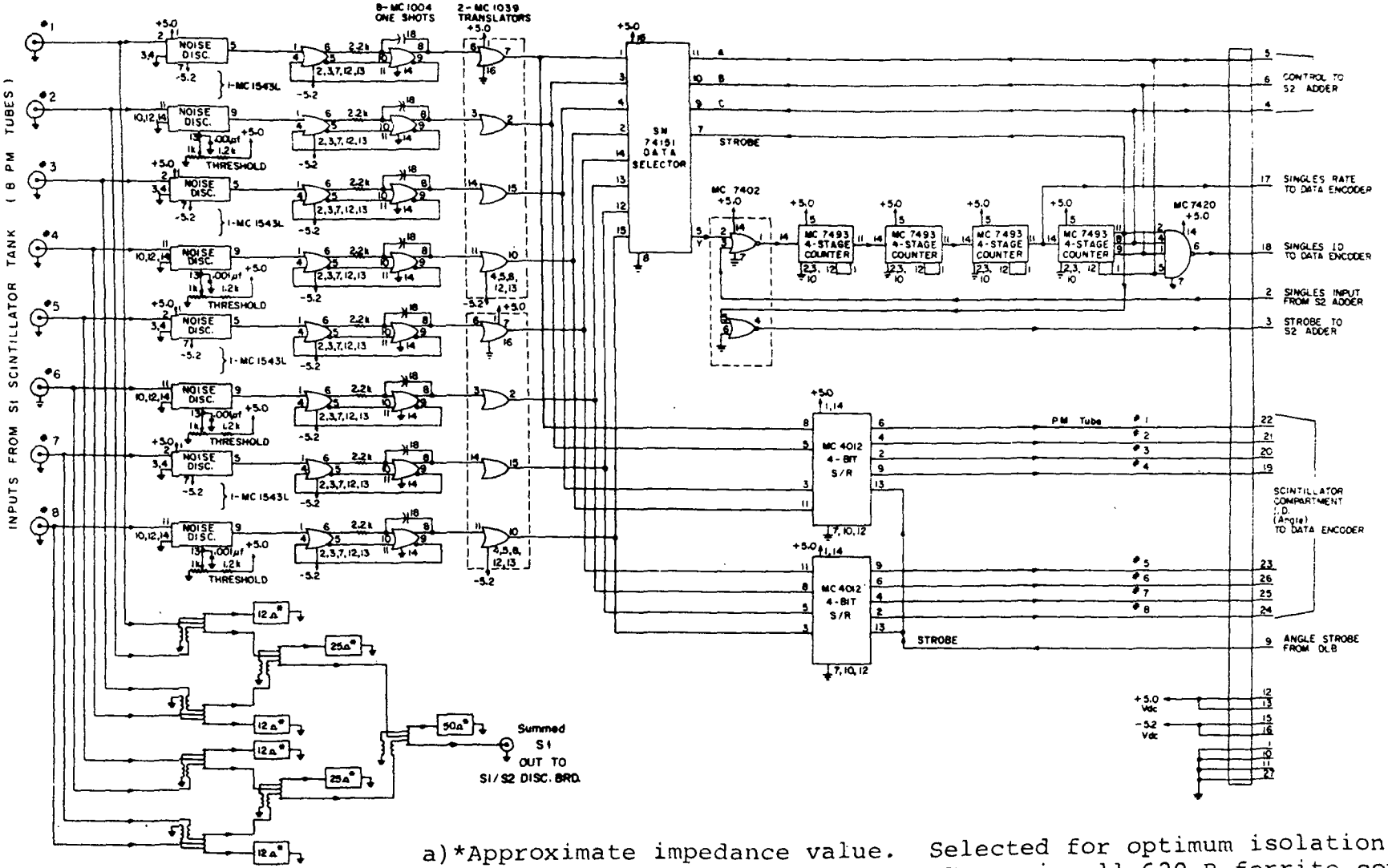


Fig. 1. Overall System Block Diagram



a)*Approximate impedance value. Selected for optimum isolation.
b)All adder transformers wound on Ferronics 11-620-B ferrite cores.

Fig. 2. S_1 Adder Board Schematic

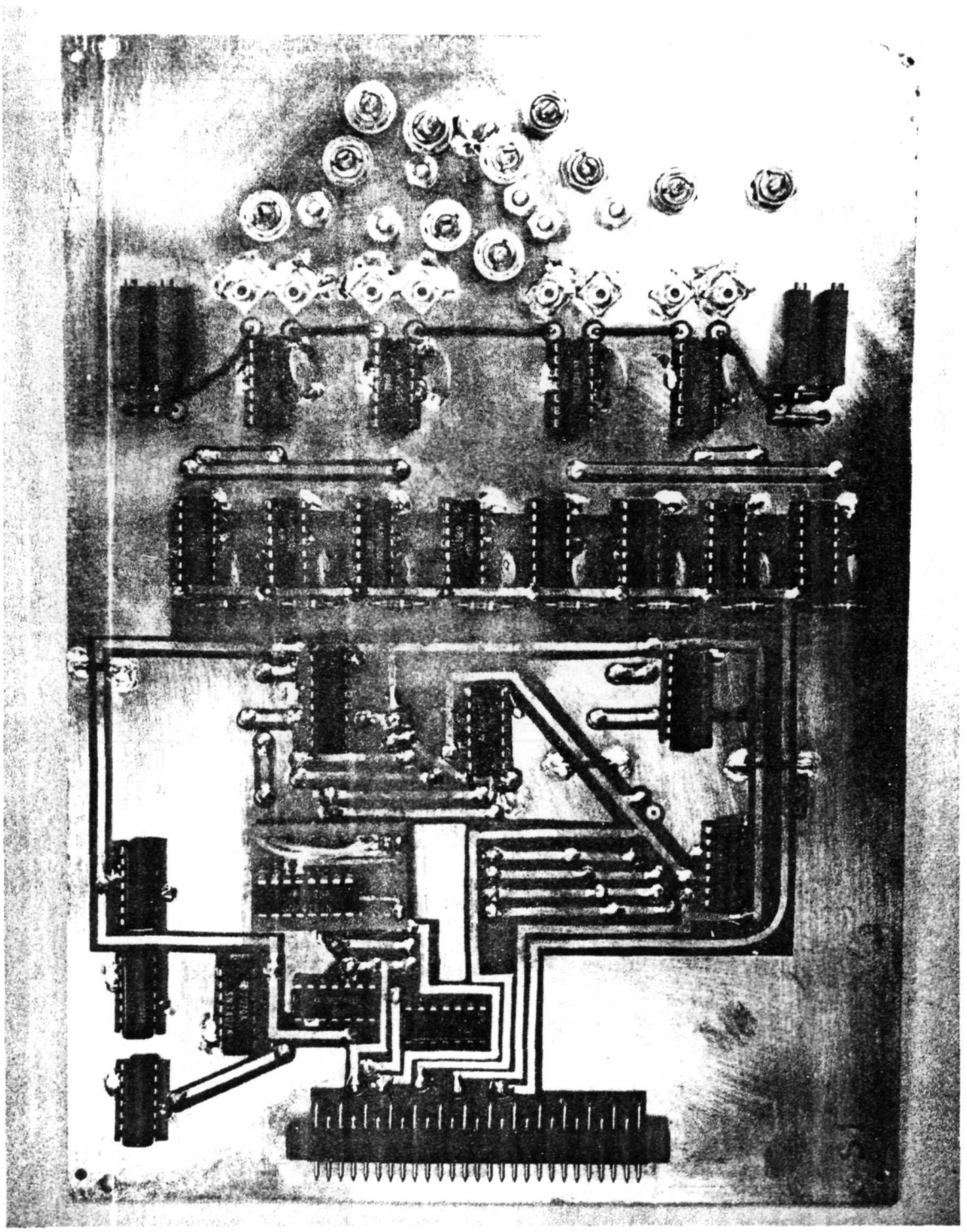
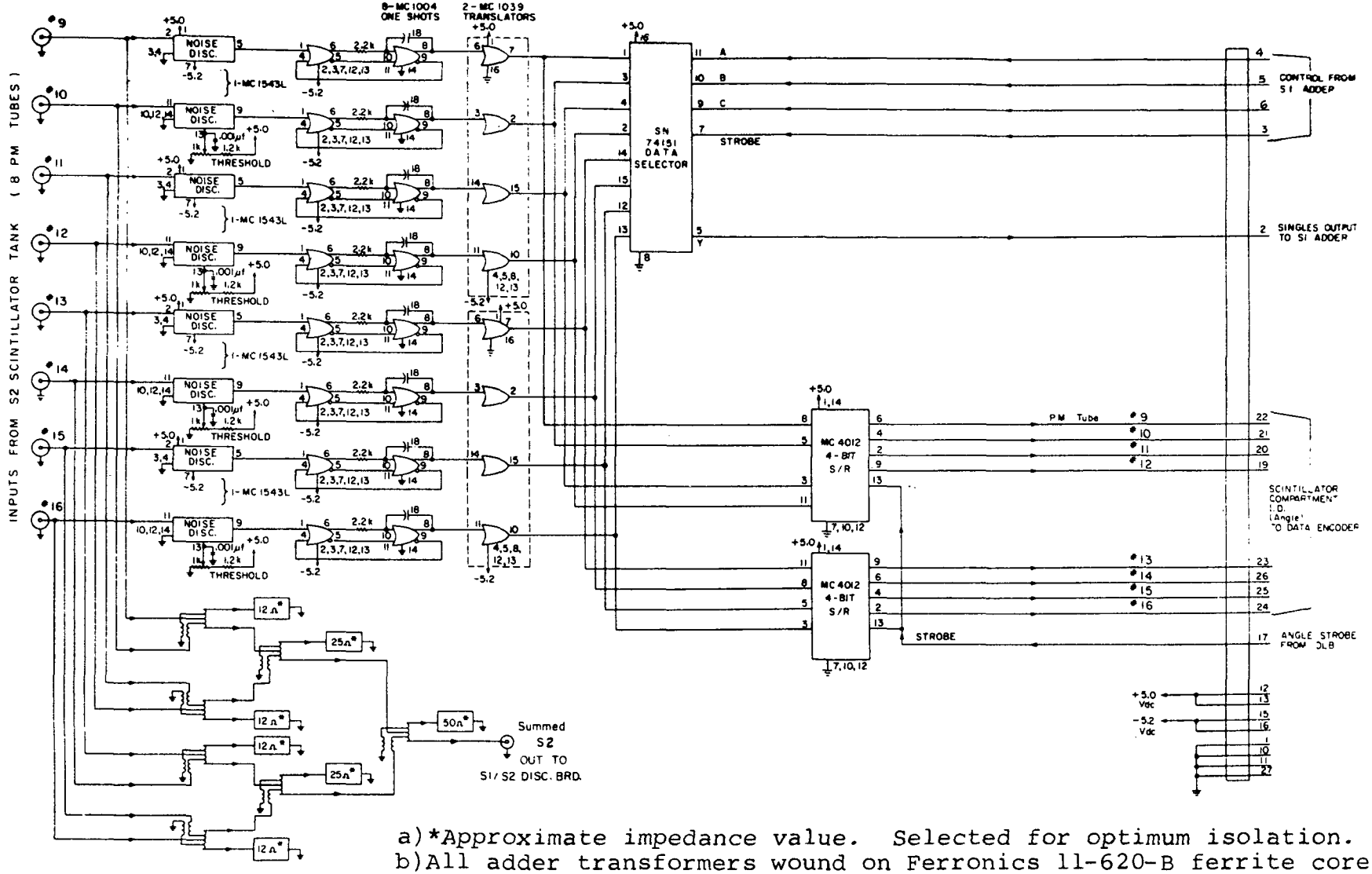


Fig. 3. S_1 Adder Board



a)*Approximate impedance value. Selected for optimum isolation.
b)All adder transformers wound on Ferronics 11-620-B ferrite cores.

Fig. 4. S_2 Adder Board Schematic

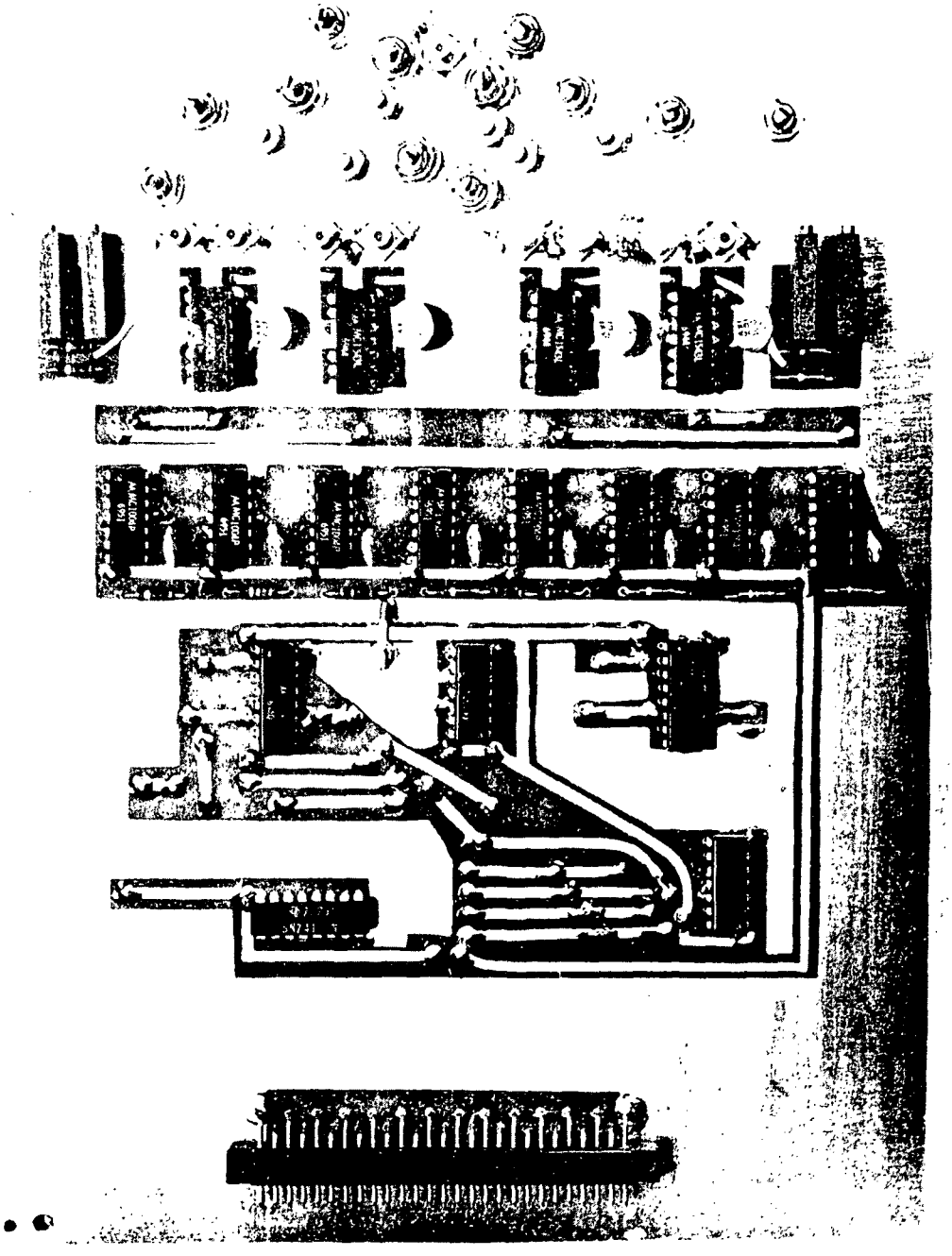


Fig. 5. S_2 Adder Board

arrangements. Each adder section consists of an unbalanced to balanced transformer, an adder transformer and a matching or balancing load impedance to achieve the required isolation. Once balanced, isolation between inputs exceeds 40 dB when driving the adder with simulated PM tube pulses (2-3 nanosecond rise time, 10-20 nanosecond fall time).

B. Singles Rate Experiment. Each PM tube input is connected to a threshold circuit discriminator to prevent unwanted noise from triggering the following electronics. High speed core-memory sense amplifiers with adjustable thresholds and strobe inputs in integrated form (MC 1543L) are used. After discrimination, the pulses are all normalized to a fixed amplitude (Emitter Coupled Logic) and then normalized to a fixed width in one-shot circuits composed of interconnecting two OR/NOR gates. The signals are translated to Transister Transister Logic, and applied to a data selector that acts as a single pole, eight position switch whose position is determined by binary logic.

With the data selector in some arbitrary position, scintillator pulses corresponding to that position are fed into a 12 stage, 4096 count, register. When the register is full, the data selector is stepped to the next position by using a four stage counter to produce the control logic.

The photomultiplier singles rate is determined by the length of time required for the register to fill and its identification by noting when the control counter is full.

The S_1 and S_2 adder boards each has its own data selector, but the common counter and control logic counter is located on the S_1 adder board.

C. Scintillation Cell Identification (Angle Information). Much of the electronics used for the singles rate is also used for the cell scintillator identification (discriminator, one-shot and translator). After the translator, each signal is applied to a shift register (MC4012). The state of the shift register's input is stored by applying a strobe pulse to the shift register. This strobe pulse is generated by the output of the signal gates on the decision logic board, and thus is present for neutron events. The strobe pulse for the S_1 and S_2 PM tubes is derived from the S_1 and S_2 signal gates, respectively. The outputs of the shift registers are fed to the data encoder.

3. S_1/S_2 Discriminator Board

After the photomultiplier tube outputs of S_1 and S_2 have each been added on their respective adder boards, the added output lines are routed to the S_1/S_2 Discrimination Board. The summed output signals: (1) are fed to a pulse height analysis board, (2) generate pulse signals with the proper width and delay for use in the logic events or particle events circuit and (3) precise timing signals for use in measuring the time of flight of neutrons and in gating the signal or anticoincidence gates. Fig. 6 is schematic of the board.

A. Pulse Height Analysis. The added incoming signals are simply fed out again to a coaxial delay line to provide sufficient delay (approximately 50 nanoseconds) so that a gating signal can be generated to record the signal pulse.

B. Logic Events Pulses. Each summed input is applied to a threshold or noise discriminator (MC1543L) and then the proper delay and width are obtained by using cascaded one-shot multivibrators using interconnected OR/NOR gates for the one-shot. The outputs are fed to the logic events board using twisted wire pairs.

C. Timing Signal Generation. To obtain accurate time-of-flight results, timing pulses must be generated which have fast response times (one nanosecond rise and fall times) and are input amplitude insensitive, i.e. the time delay through the timing generator must not be sensitive to the summed analog input signal. This requirement can also be stated as a need for "zero-walk" performance. The zero-walk circuit operates on the summed signals as follows. (See schematic, Fig. 7 and photo Fig. 8).

The heart of the zero-walk circuit is the charge storage or step recovery diode. It has the property that when driven from forward conducting to reversed biased the diode continues to conduct in the reverse direction until the charge stored in the diode during its forward biased period is removed. Then, within a hundred picoseconds or so the diode "snaps" off to a nonconduction state. Therefore by removing charge

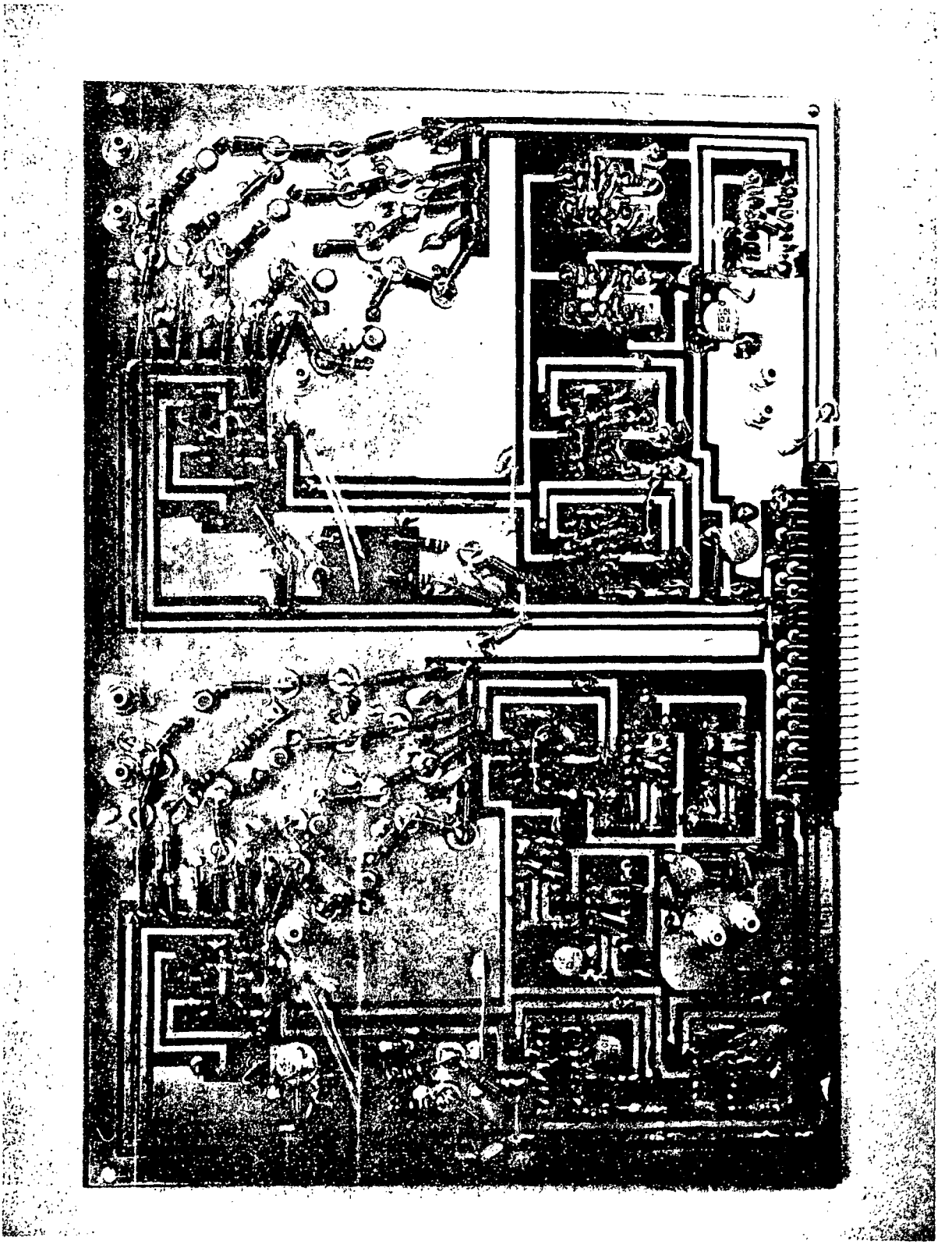


Fig. 8. S_1/S_2 Discriminator Board

proportional to the rate of adding charge, both of which are dependent on the input signal amplitude, this step recovery always occurs at the same time with respect to an amplitude varying input.

In order to cover the large dynamic range of the input signals (25 mV to 6 volts), amplification of the low level signals is needed to operate the timing generators. Four fast amplifier stages are used which amplify and shape the pulses, with limiting occuring to reduce the dynamic range of signals applied to the step recovery diode. The diode first receives a negative signal and starts conducting. Then through inverting transformer T1, the signal is delayed and inverted, and removes charge from the diode until it "snaps" back to a non-conduction state.

Overall, in spite of some slight timing errors introduced by the amplifier circuits, the timing accuracy is within 0.5 nanosecond for the dynamic range of 25 mV to 6 volts (a 240 to 1 range).

The output of the zero walk circuit is applied to a threshold discriminator which is used as a controlled gate and logic translator. A fast, short, one-shot (MC1660) of ten nanoseconds follows and is used as the "fast" input to the signal gate.

Since the zero walk does not provide noise discrimination, a parallel discriminator circuit, using an MC1543L along with a MC1660 OR/NOR one-shot, generates an "enable" signal for use with the signal gates.

4. A_1, A_2 Discriminator Boards

The A_1 and A_2 Discriminator Boards receive photomultiplier tube outputs from the anticoincidence scintillator sheets around S_1 and S_2. A schematic of both is seen in Figs. 9 and 11 and photos in Figs. 10 and 12.

The two PM tube outputs from the upper most sheet of both scintillators are added together and the resulting signal is used four ways. It is fed directly through a coax connector to a coaxial delay line and then is pulse height analyzed. It is used to generate logic event signals (by being level discriminated, delayed and stretched). Also high-Z discrimination takes place using a 40:1 resistive attenuator ahead of a discriminator. This high-Z channel signal is used for logic event signals and to enable the signal or anti-coincidence gates. Finally, the input signal is also added with the side and bottom scintillator PM tube outputs. This addition is accomplished using the passive adders described in the S_1 and S_2 adder section.

The PM tube outputs from the side and bottom sheets likewise are added to each other and used to generate logic event pulses. The four event pulses, A_{12}, A_{13}, A_{22} and A_{23} are used with the high-Z experiment and are routed to the decision logic board where their state is observed by the outputs of the signal gates.

The added signal from all the anticoincidence sheets of either A_1 or A_2 is discriminated and used for logic events and for an anticoincidence pulse to the signal gates.

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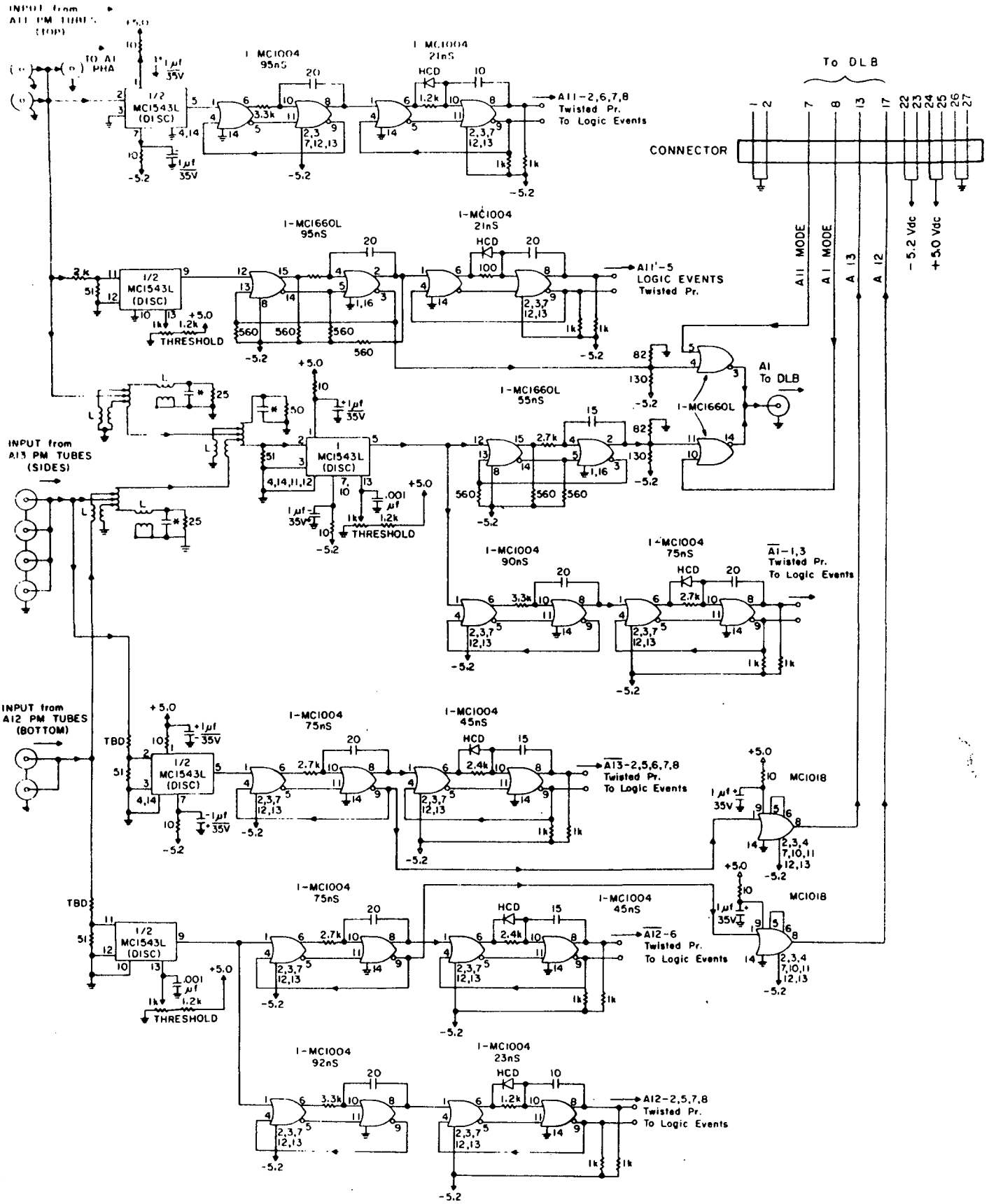


Fig. 9. A_1 Discriminator Board Schematic

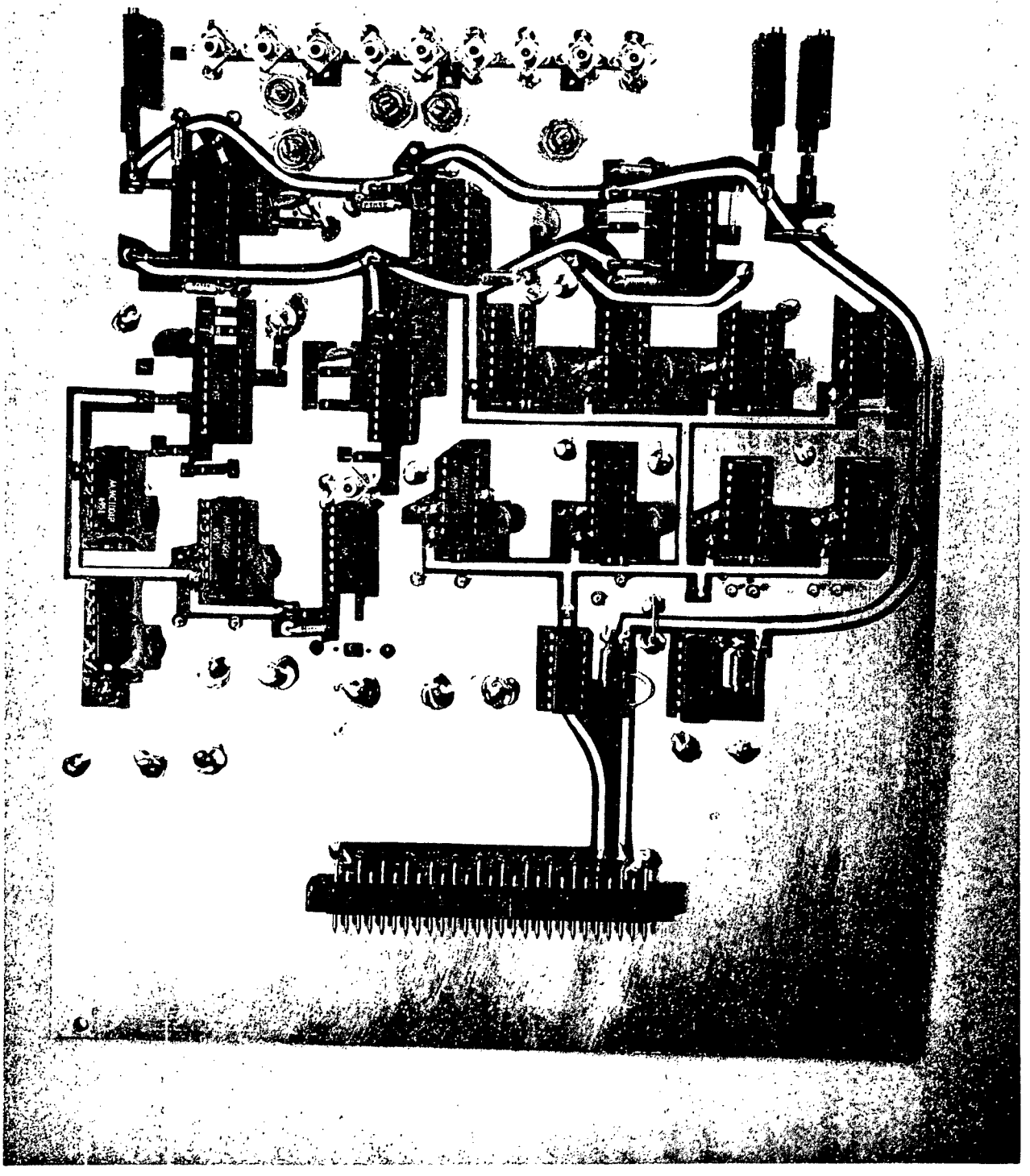


Fig. 10. A_1 Discriminator Board

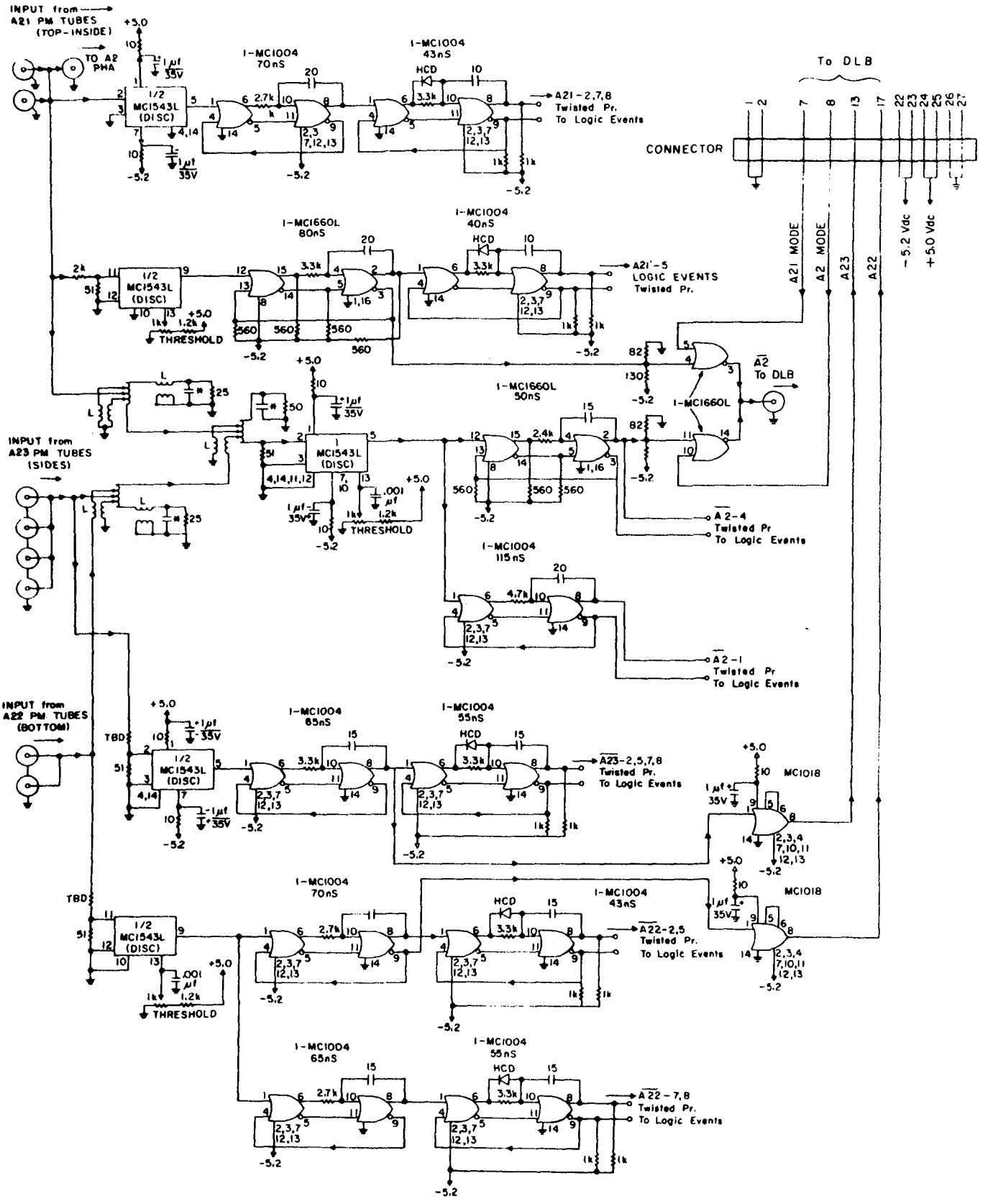


Fig. 11. A_2 Discriminator Board Schematic

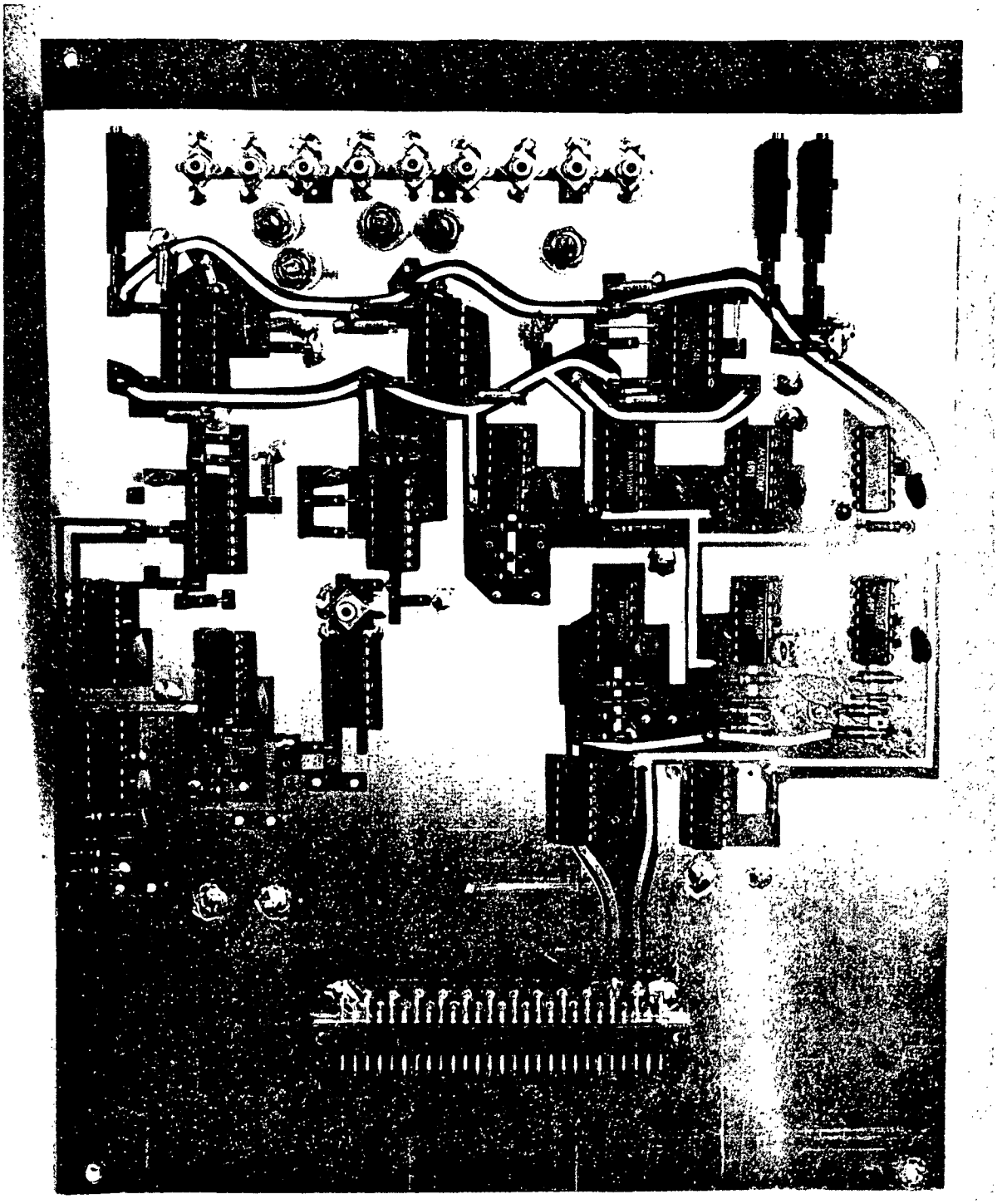


Fig. 12. A_2 Discriminator Board

5. Decision Logic Board

The Decision Logic Board serves many purposes. It contains the:

a. signal or anticoincidence gates

b. event counter

c. A_{12}, A_{13}, A_{22} and A_{24} event registers

It also generates:

d. "Start" and "stop" signals for the Time-of-Flight Board

e. mode (solar, albedo, high-Z) and calibrate logic

f. PHA gate enable pulses

g. strobe signals for the scintillator cell identification

i. control logic for the logic events data selector

j. the 40:1 PHA attenuator drive signal

k. reset signals for the PHA and time of flight registers

l. reset signals for the FET switches in the PHA's

m. a 300 microsecond "processing event" signal for the data encoder (W line).

The signal lines (Fig. 13,14) from the S_1/S_2 discriminator board and the A_1 and A_2 discriminator board are applied to the fast signal gates of IC2. These are 1 nanosecond MECL III, the fastest presently available logic. The outputs of the signal gates go to the 140 nanosecond pulse stretchers (IC3, 4, used as one shots) and also to mode control gates (IC5, 6). These gates route the signals coming from the

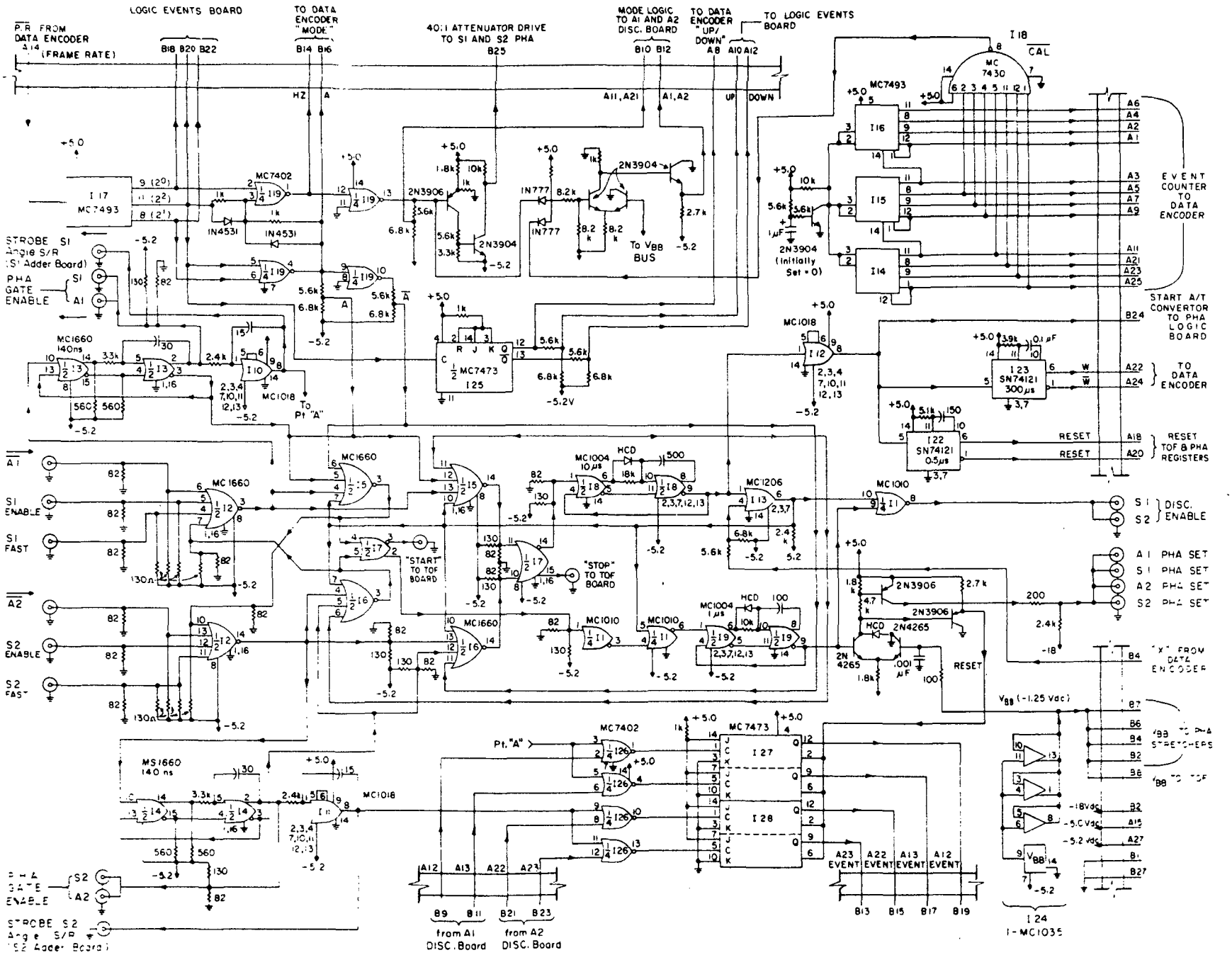


Fig. 13. Decision Logic Board Schematic

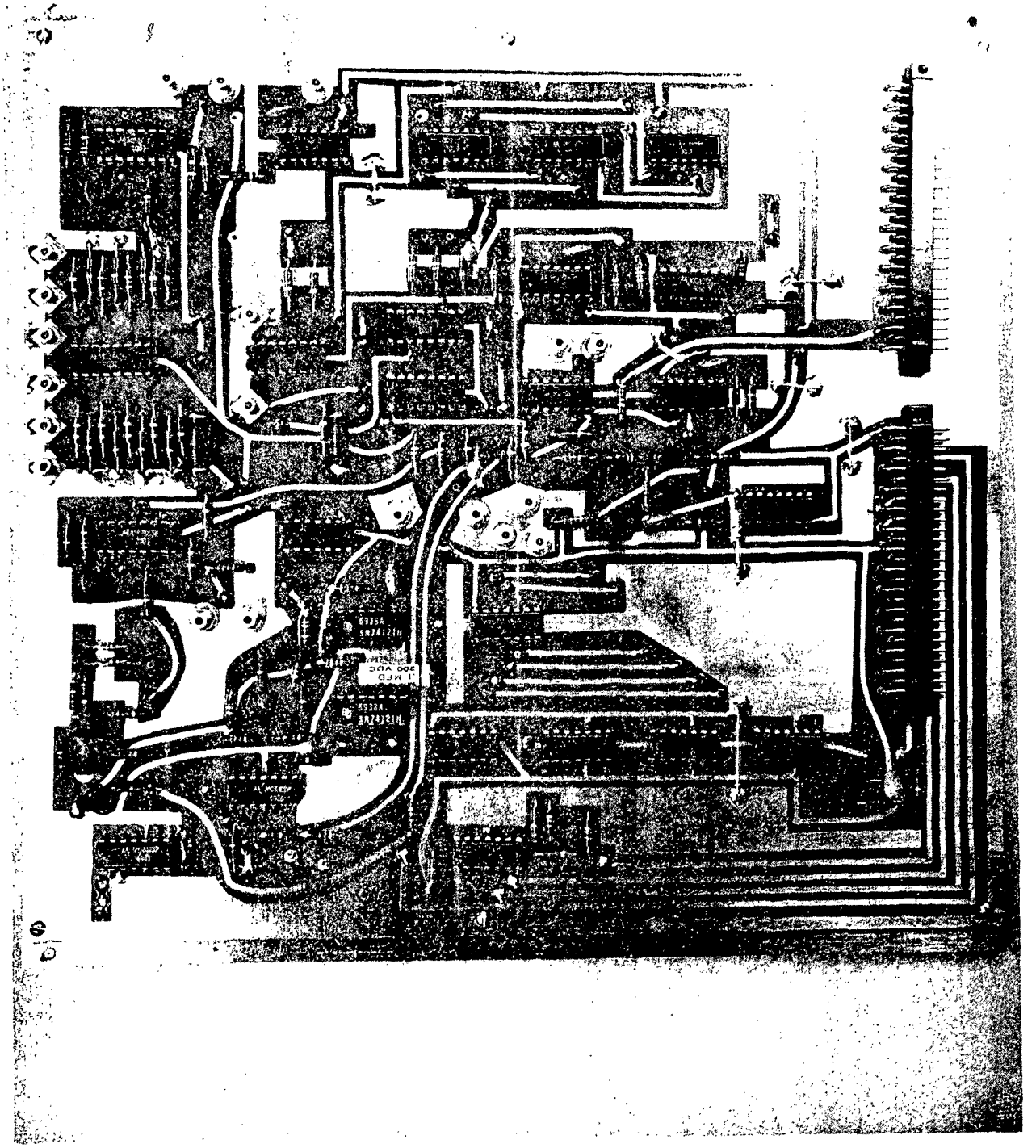


Fig. 14. Decision Logic Board

signal gates using logic generated in I17, 19 to gates I7, which produce the "start" and "stop" pulses for the time-of-flight circuitry.

If a stop signal is generated this indicates that a valid event has occurred and a 10 microsecond one-shot (I8) triggers and operates the event counter (I14, 15, 16), a 0.5 microsecond one-shot (I22) for quickly reseting the PHA and time-of-flight registers, the 300 microsecond "processing event" one-shot (I23), starts the PHA circuitry operating and disenables the signal discriminators on the S_1/S_2 discriminator board thru I13 and I1. The signal discriminators continue to be held off past the initial 10 microseconds by the "X" line from the data encoder. This line logically says that a signal is being processed or has been processed but not transferred yet to the shift registers of the data encoder.

The PHA holding capacitors are reset to zero both after an invalid event has occurred and after the buffer registers have been read out following a valid event via the "X" line. This is accomplished by gate I1, the 1 microsecond one-shot I9, and some transistor level shifting circuits. The A_{12}, A_{13}, A_{22}, and A_{23} flip flops are simultaneously reset.

If the system is in the "solar" mode, the S_1 signal gate will be enabled to receive a pulse but the S_2 signal gate is blocked by feedback from I5. Only after the S_1 signal gate receives a valid signal is the S_2 signal gate allowed to operate, and then only for a period of 140 nanoseconds. If

the particle does not interact in scintillator S_2, no "stop" pulse is generated and the system is reset as noted above.

The mode logic discussed earlier is also connected to a two transistor drive circuit for the 40:1 attenuator. A calibration logic signal is generated for every 128 events, so the first 7 lines from the event counter are connected to NAND gate (I18). This calibrate signal along with the mode logic operates some ECL to produce control logic for the A_1 and A_2 discriminator boards.

Strobing signals for the scintillation cell identification (angle) registers are obtained by delaying and translating the outputs of the 140 nanosecond one-shots connected to the signal gates. It is the negative going strobe signal which reads the cell identification information into the registers on the S_1 and S_2 adder boards.

6. Pulse Height Analysis Boards

The purpose of the pulse height analyzer is to convert amplitude of the PM tube pulses to pulses whose time duration is proportional to input pulse amplitude. This output pulse is connected to a clock which sends pulses at a fixed rate into a counter. Thus the larger the PM tube pulse, the longer the pulse duration from the analyzer board and the longer the time the clock sends pulses to the counter. The overall result is an A/D converter whose counter output is a binary code representation of the input pulse amplitude. (The clock and counter are located on the Buffer Memory Logic board).

The circuitry (Fig. 15, 16) consists of a fast current amplifier (Q7, Q11) that stores a charge on the 9 pF capacitor following diode D8 proportional to the input amplitude. Constant current sources (Q4-Q6, Q8-Q10 and Q16-Q20) place the current amplifiers in an initial conducting state and establish the maximum current swing possible.

A fast shunt attenuator, used as a signal gate, is composed of differential amplifiers Q14, 15 and Q12, 13 which switch shunt diode D4 on or off. The gate input drive originates on the decision logic board, and is derived from the output of the appropriate anticoincidence gate.

An FET input buffer (Q22-27) follows the holding capacitor and drives the amplitude to time converter. This A/T converter consists of a high gain differential amplifier (Q29-32) with a diode (D14) in the feedback loop. The circuit is used in a sample and hold arrangement by placing a 2700 pF capacitor at the output of the amplifier, after diode D14. Thus the loop has a closed loop gain of unity and for negative signals the capacitor voltage follows the input. When the input goes positive, the diode reverse biases opening the loop and holding the peak voltage on the capacitor.

Shunt FET switches across the capacitor and the 9 pF unit in the stretcher section are used to reset the capacitor voltages to zero following an invalid event (a neutron going through S_1 but not S_2, for example).

A constant current source (Q34) is switched on 10 micro-seconds after the input signals by a signal applied to the

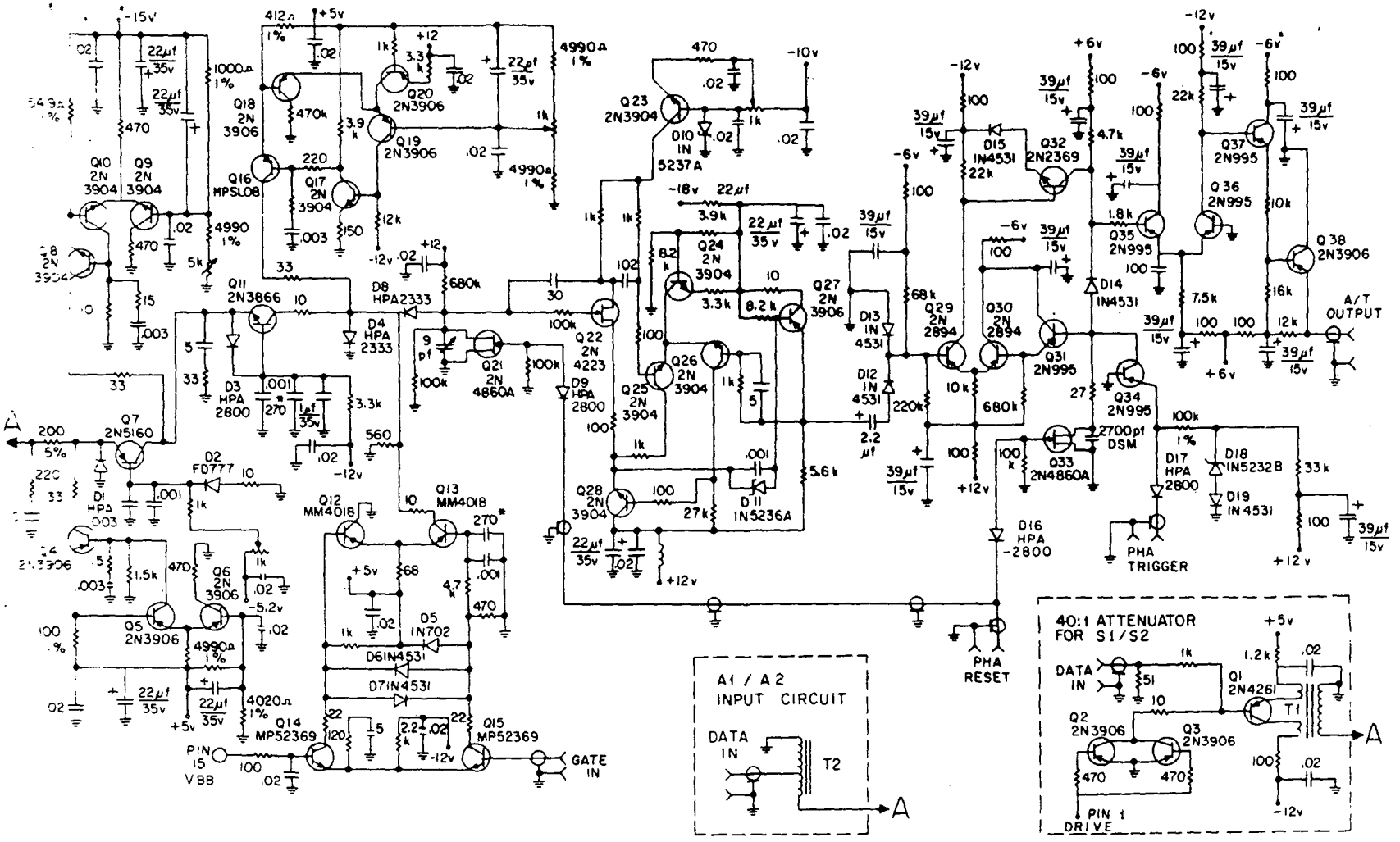


Fig. 15. Pulse Height Analysis Board Schematic

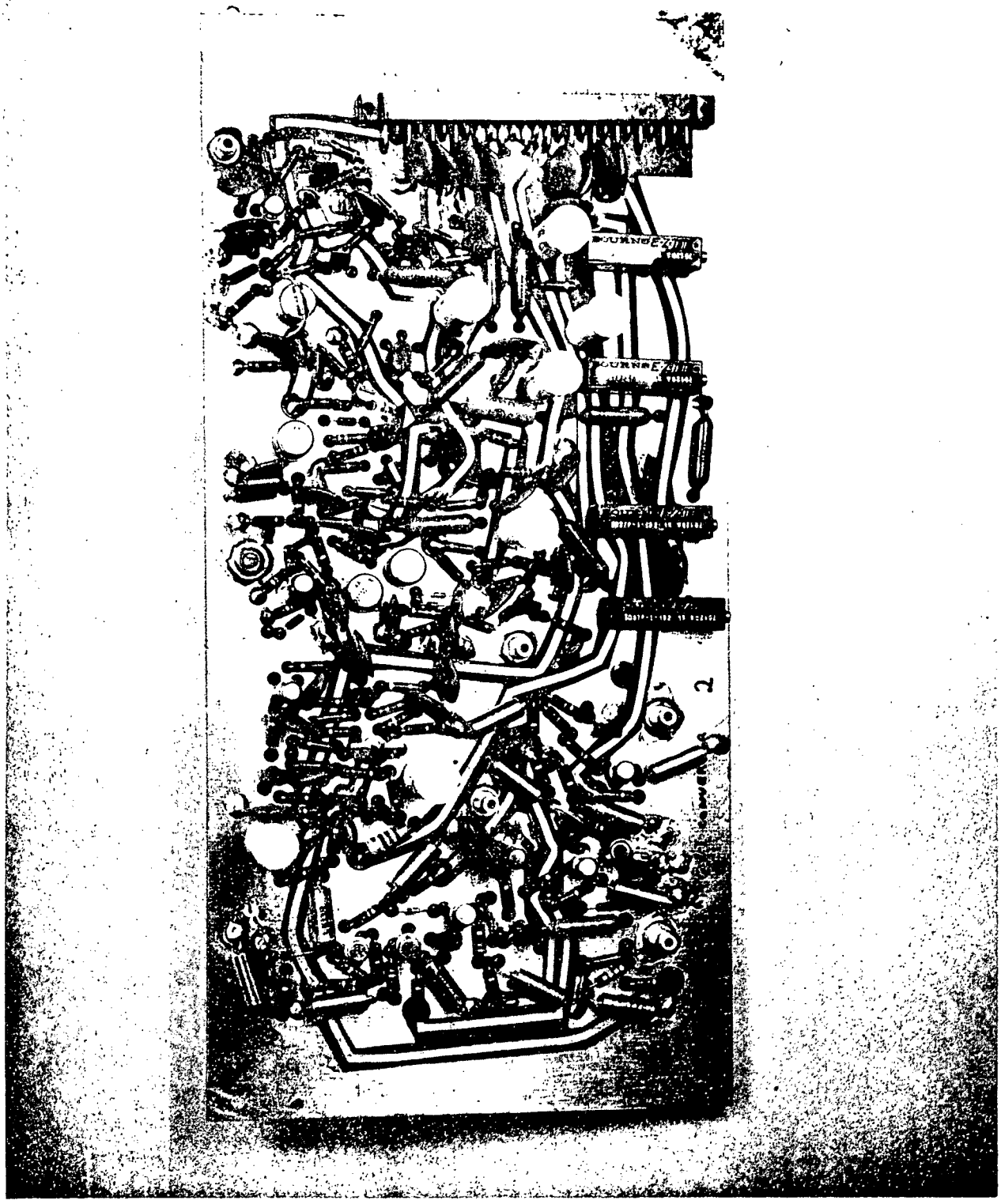


Fig. 16. Pulse Height Analysis Board

PHA trigger input. This signal is a pulse 300 microseconds wide and is derived on the Buffer Memory Logic Board. The current flow to the capacitor develops a linear (fixed slope) voltage ramp bringing the capacitor voltage back to zero. When close to zero, diode D14 begins conducting again and the loop once more closes.

Shaping amplifier (Q35-38) monitors the time that the amplifier loop is open and presents a gating signal output with a width directly proportional to the input PM tube pulse amplitude.

The S_1 and S_2 PHA are used both in the neutron mode and the high-Z mode. Therefore an attenuator must be employed prior to the PHA when in the high-Z mode to stay in the linear operating range of the PHA. This attenuator consists of a resistive attenuator switched in by transistors Q2, 3. Transistor Q1 lightly loads the attenuator and is used as a buffer amplifier.

7. Buffer Memory Logic Board

The buffer memory logic board (see Fig. 17, 18) receives a gating signal from each PHA board whose width is directly proportional to the input PM tube amplitude. This gating signal applied to a gate enables JK F/F MC7473, allows 2MHz clock pulses from oscillator IC6 and translator IC5 to be fed into an 8-bit memory (MC7493). The 9-bit memory, that includes the output state of the F/F, stores the pulse amplitude in a binary form to be fed to the Data Encoder.

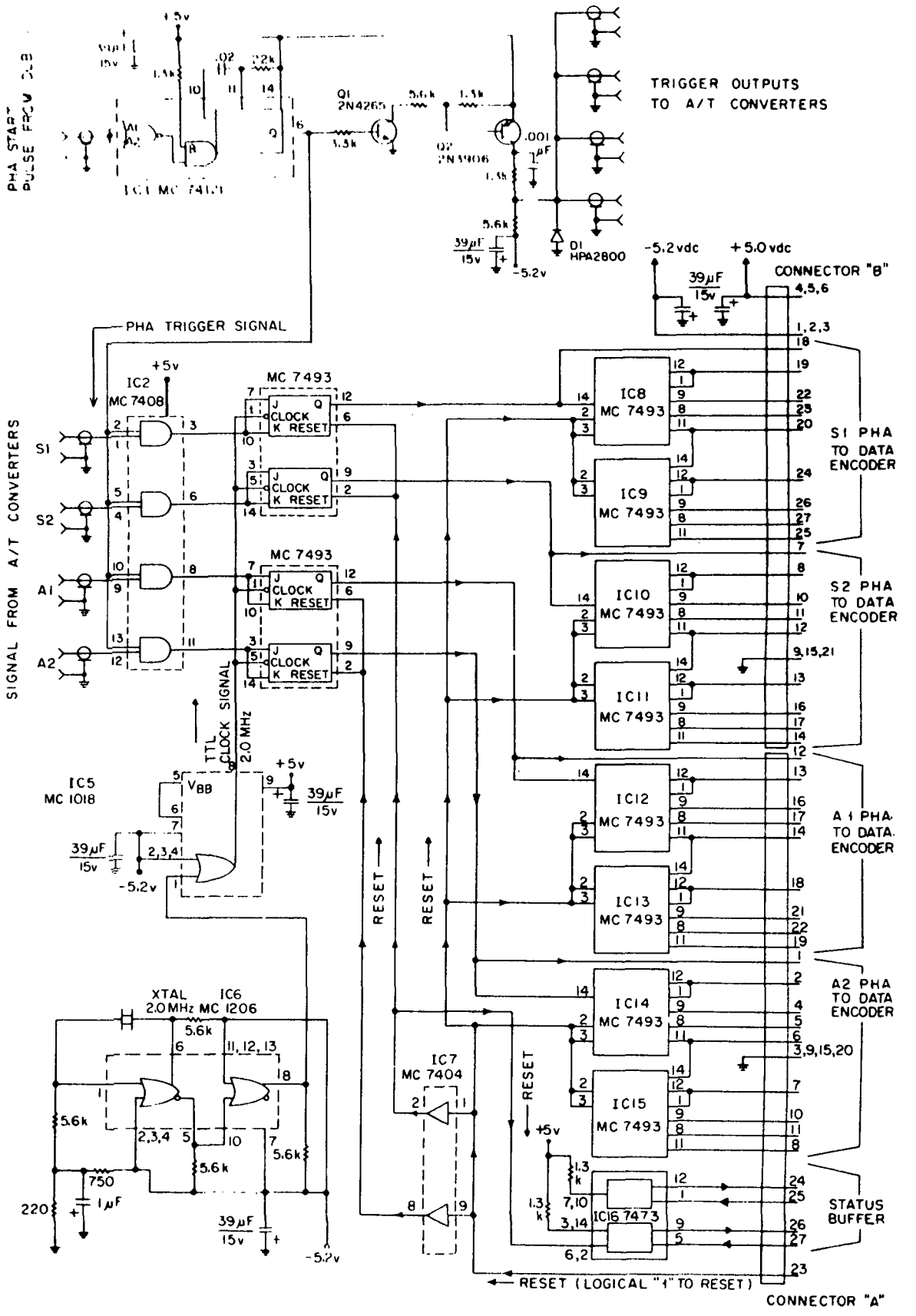


Fig. 17. Buffer Memory Logic Board Schematic

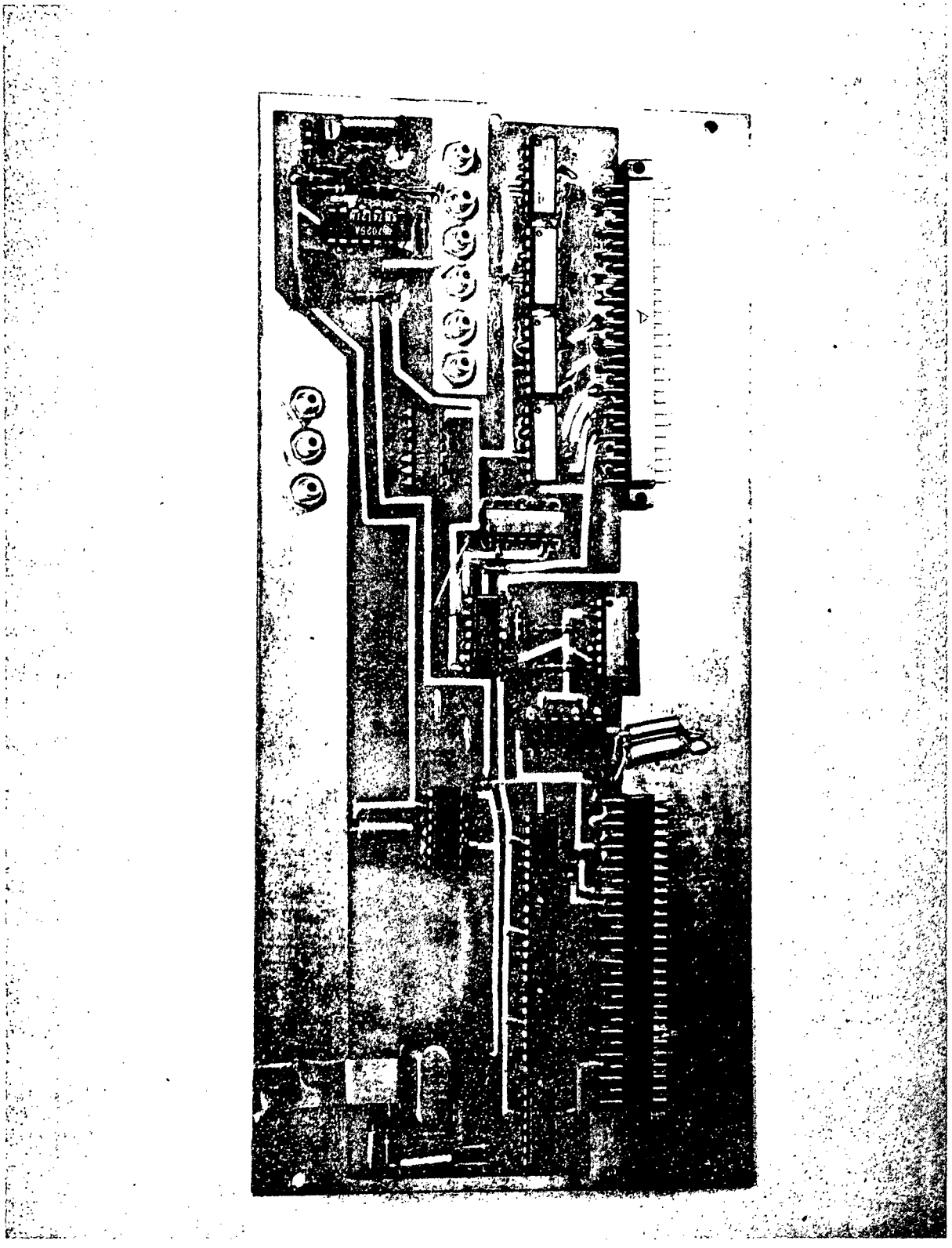


Fig. 18. Buffer Memory Logic Board

This board also includes the 300 microsecond one-shot for operating the current sources (through Q1,2) on the PHA boards and the input gates of IC2.

8. Time of Flight Board

The measurement of the time of flight of particles between the top and bottom scintillator tanks is performed on the time of flight board, Fig. 19,20. The technique is a time to voltage to digital code conversion. In this case a voltage proportional to the time of flight is generated, held and converted to a digital output using an accurate double ramp conversion technique.

Prior to an event occurrence, a constant current of 10 milliamperes, generated by the IC1, Q5, Q6 circuit, flows to the junction of D2 and D3 (D1 is reverse biased) where it splits equally with 5 milliamperes flowing through D4 (D5 is reversed biased) to another precise constant current source of 5 milliamperes formed by the IC2 and Q8 circuits. Since the currents through D2 and D3 are equal, the initial voltage across the sampling capacitors C1, C2 is zero.

Diode D1 is switched into a conducting state when a "start" pulse (generated in the decision logic board) appears at the input. The 10 milliampere constant current is then diverted through D1 and Q1, causing D2 to become reverse biased. Since the 5 milliampere current is still being demanded, it is supplied through the sampling capacitors, which thus begin charging at a constant rate of IT/C volts per second, set at about six millivolts per nanosecond.

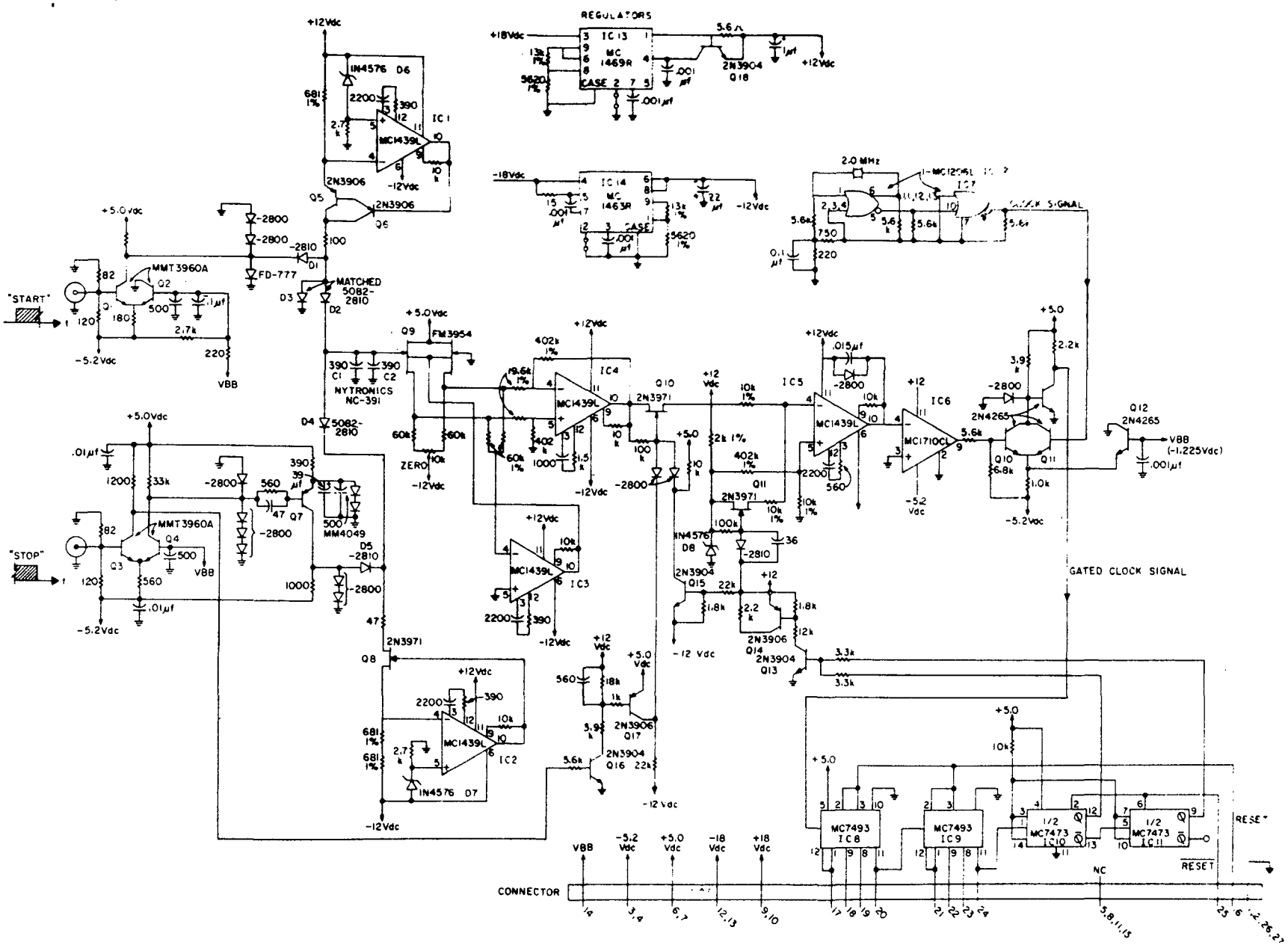


Fig. 19. Time-of-Flight Board Schematic

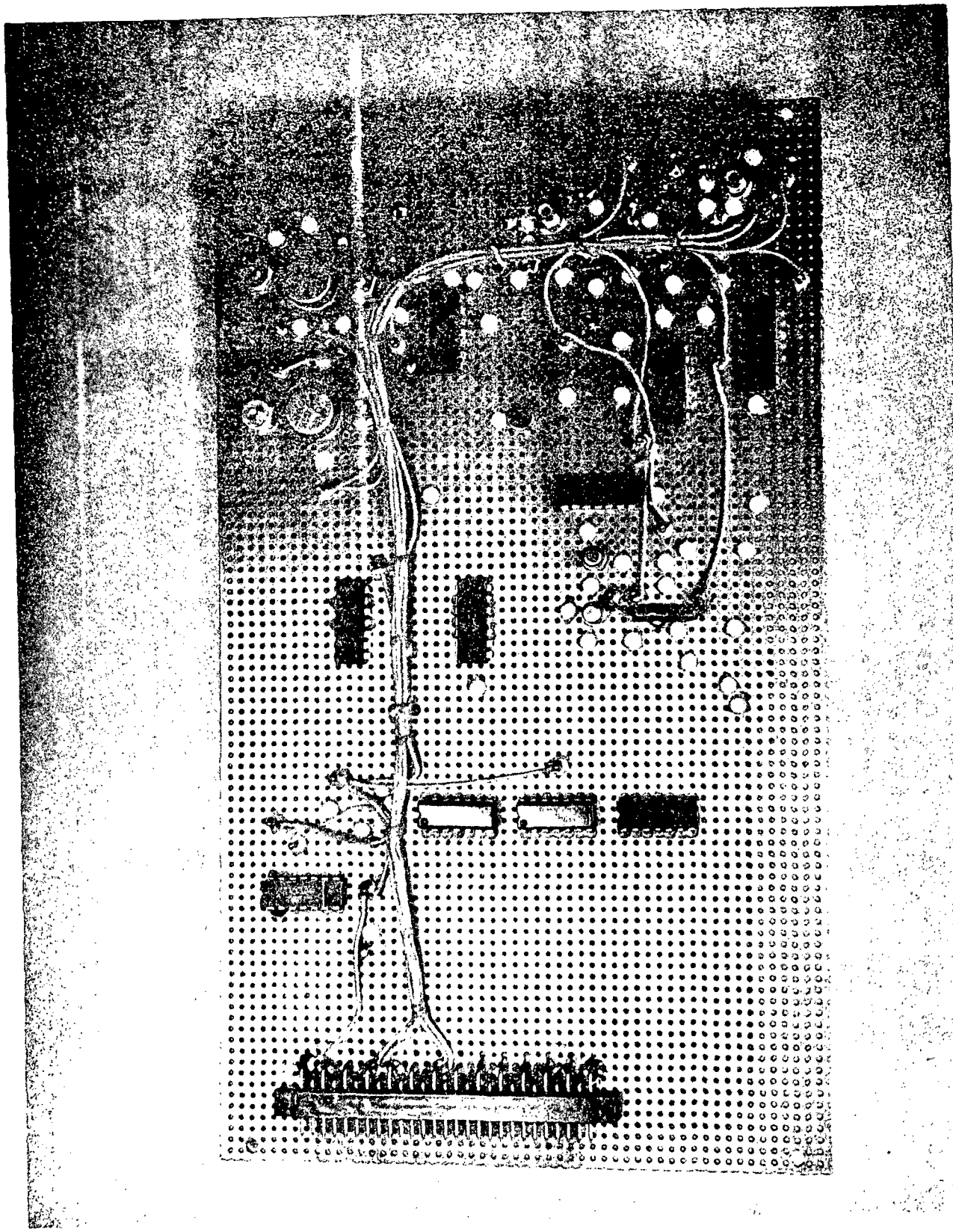


Fig. 20. Time of Flight Board

The voltage ramp across the sampling capacitors is stopped when the "stop" pulse arrives and causes D5 to be switched into conduction, so that diode D4 is reverse biased and the 5 milliampere current is now supplied through Q7 and D5.

The stored capacitor voltage is sensed by a unity gain buffer amplifier consisting of Q9, a matched monolithic dual-FET, and IC-3, used to bootstrap the source on the FET, keeping the input current to less than ten picoamperes. This buffered voltage is then amplified by IC-4, connected as a gain of twenty balanced differential amplifier.

It is this amplified version of the capacitor voltage which is now converted to binary form by the dual ramp A/D converter circuit. It is carried out by comparing the capacitor voltage with a stable reference voltage, developed across reference diode D8. The comparison is performed by two FET switches, Q10 and Q11 that connect first the amplified capacitor voltage and then the reference voltage to integrator IC-5 at the correct time. The output of the integrator is initially below ground, so the application of the capacitor voltage (negative) causes the integrator output to be a positive going ramp with a slope of V_{tof}/RC. Upon crossing zero, the output causes comparator IC-6 to change state, enabling gate Q10, 11 to pass clock pulses into the 8 bit (256 count) register IC8, IC9.

With clock pulses coming at the fixed rate of 2 megabits

per second, and a register capacity of 256, the register is filled after 128 microseconds. It then toggles flip flop IC10 that drives the transistor circuit Q13, Q14, Q15 to switch the integrator from the time of flight voltage over to the reference voltage.

The reference voltage is of the opposite polarity (positive) with respect to the time of flight voltage, so the integrator output is now a ramp going negative with a fixed slope of V_{ref}/RC. Concurrent with the time the switching changes, the register also clears itself to zero and continues counting. The counting continues until the integrator output again crosses zero, at which time the register is inhibited. The stored count is now directly proportional to the value of the integrator output at the time when the switchover takes place and hence to the time-of-flight.

Operation of the circuit has been very good and initial tests have indicated a time resolution on the order of a quarter of a nanosecond. Faster clock speeds could imporve on this if system requirements demanded better resolution.

9. Data Encoder

The Data Encoder consists of a clock generator, a synchronization pattern generator, a control section and a 96 bit memory in the form of shift registers. See Figs. 21, 22, 23.

The clock section (Fig. 21) begins with a 100 kHz transistor oscillator which is divided by four in a dual

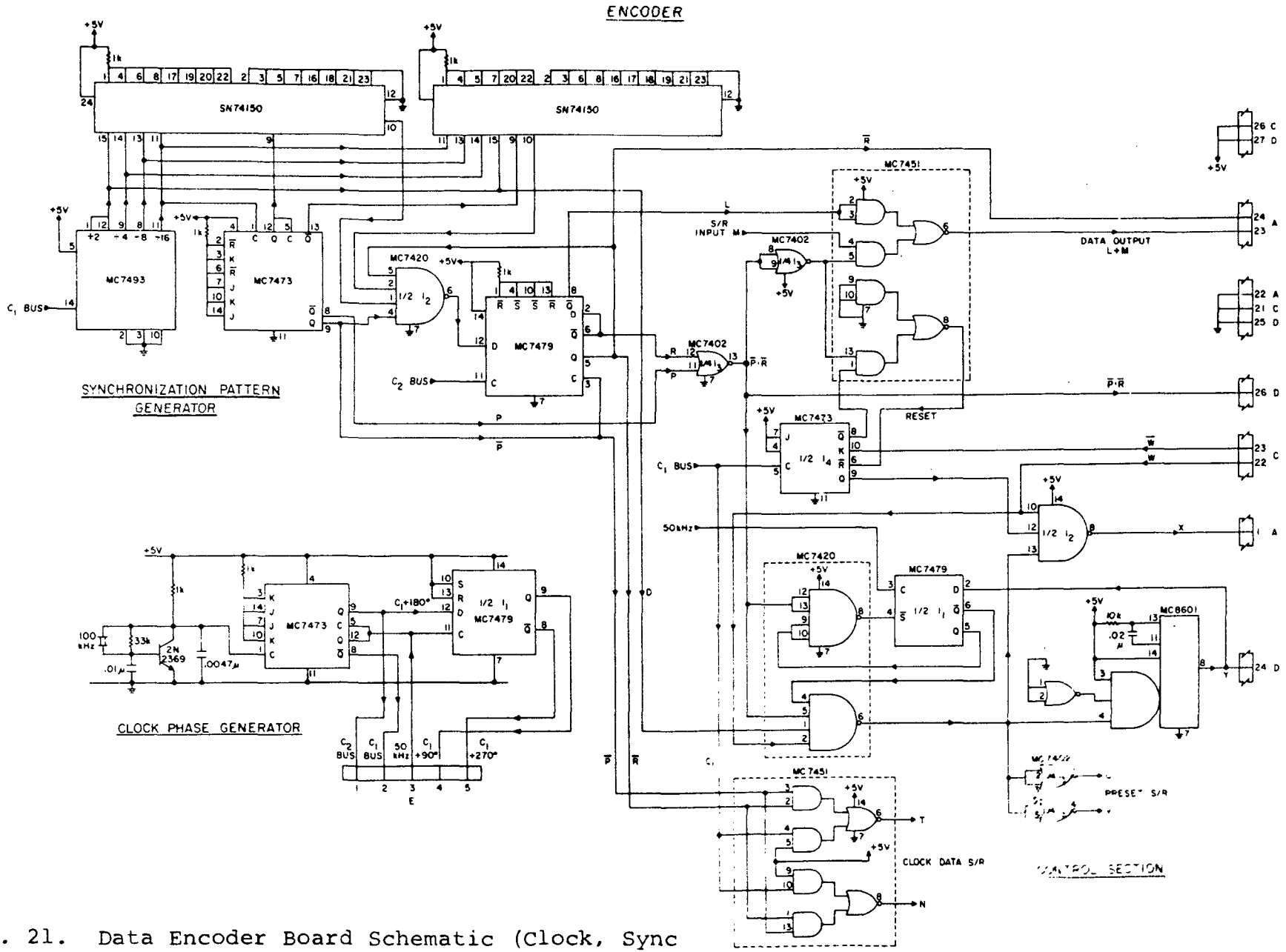


Fig. 21. Data Encoder Board Schematic (Clock, Sync Pattern Generator, Control)

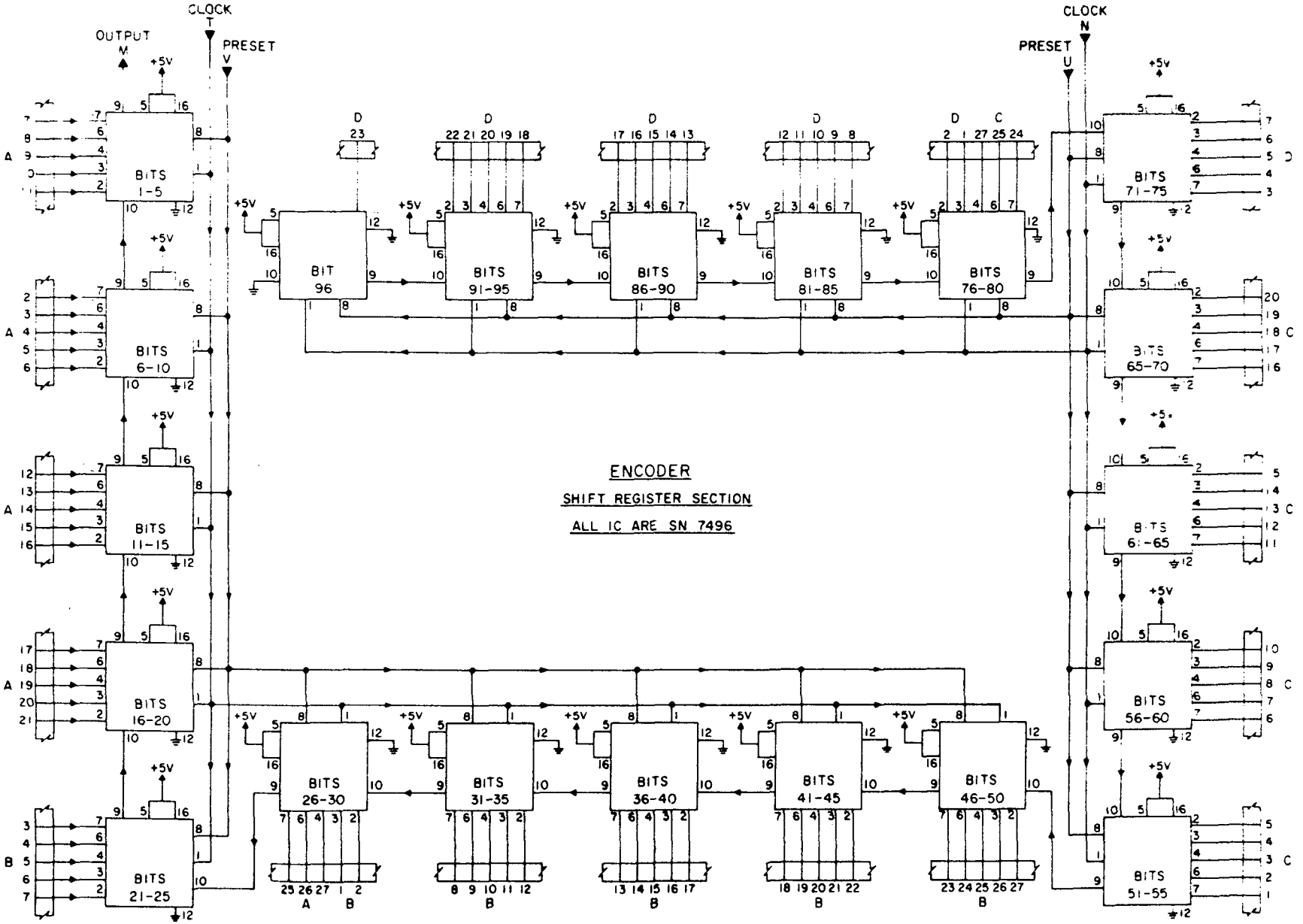


Fig. 22. Data Encoder Board Schematic (Shift Register Section)

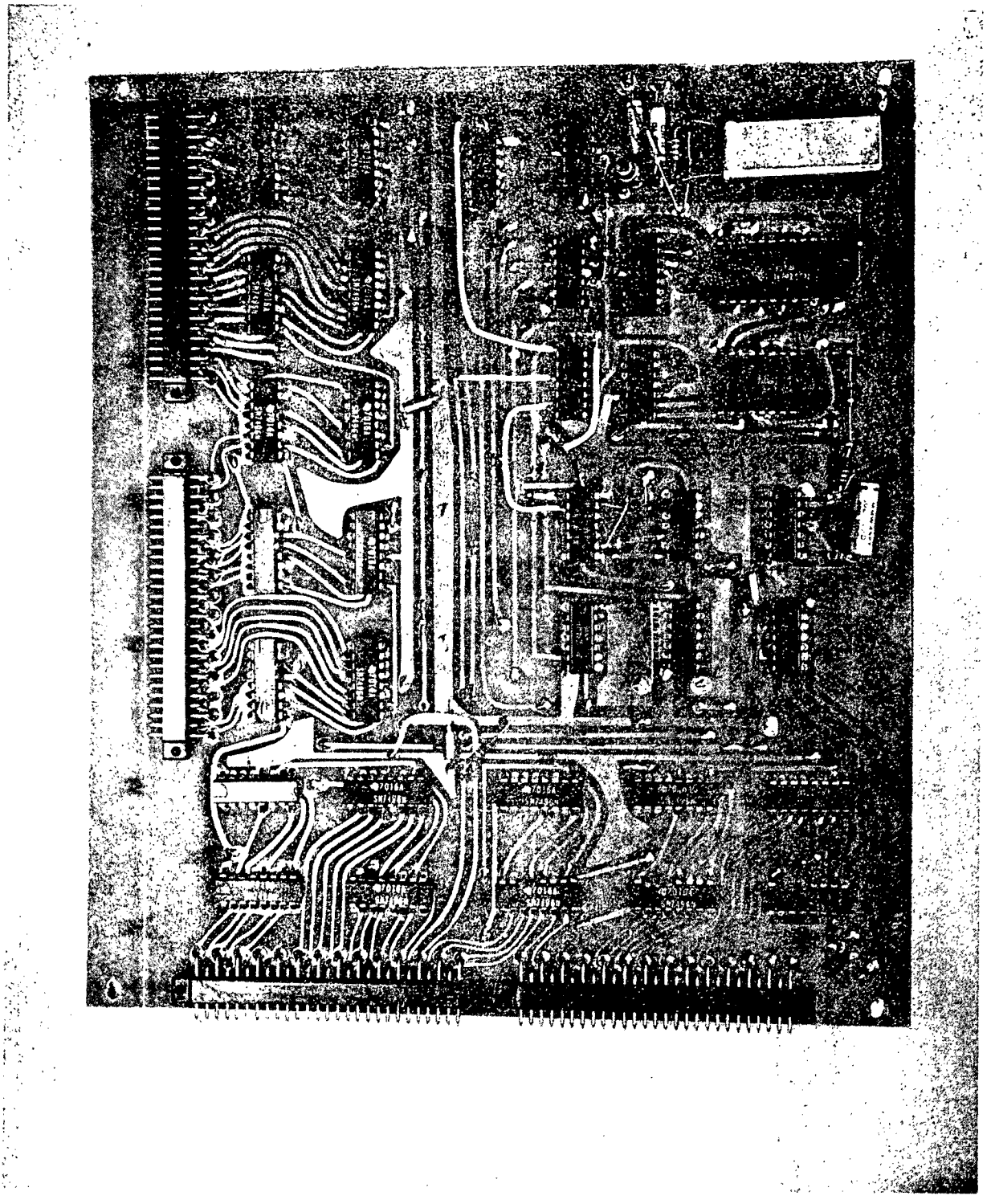


Fig. 23. Data Encoder Board

JK flip flop (MC7473). The output of the first stage provides a 50 kHz bus and the Q and $\bar{Q}$ outputs of the second stage are defined as the 0^{o} and 180^{o} phases of the 25 kHz clock. Applying the 180^{o} clock line to the D input of a type D flip flop (MC7479) with the 50 kHz line on the clock input, the Q and $\bar{Q}$ outputs become the 90^{o} and 180^{o} phases of the clock.

The synchronization pattern generator is composed of two 16 input data selectors (SN74150), their inputs preset to logical "1" or "0" according to the desired synchronization pattern format. The 0^{o} clock (25kHz) is divided in a 4-bit counter (MC7493) to supply the four control lines to the data selectors. A following JK flip flop (MC7473) provides Q and $\bar{Q}$ outputs which strobe on the data selectors alternately for sync bits 1-16 and 17-32. The sync pattern is shown on the following page along with the data bit allocations.

The outputs of the data selectors are gated with $\bar{P}$ and $\bar{R}$ signals (derived by division of the clock) in a NAND gate (MC7420). The output of the NAND gate is then clocked through a D flip flop with the 180^{o} clock phase and becomes the synchronization pattern, L, which is combined with the data bit stream from the shift register memories in a MC7451 to form the composite data frame, 32 bits of sync and 96 bits of data.

The control section governs the transfer of data from the buffer registers (on the various boards) to the shift

Encoder Bit Allocation

	Bits	Position
Synchronization Pattern	32	1
Mode (Solar, albedo, high Z)	2	2
Event Counter	12	3
Upper Scintillator I. D. (Angle)	8	5
Lower Scintillator I. D. (Angle)	8	7
PHA S1	9	4
PHA S2	9	6
PHA A1	9	11
PHA A2	9	16
A13 event	1	17
A12 event	1	18
A23 event	1	19
A22 event	1	20
Time of Flight S1 to S2	8	8
Singles Rate	1	9
I.D.	1	10
Temperature Data	1	12
I.D.	1	13
Azimuthal Data	1	14
I.D.	1	15
Logic Events	9	21
Available for future use	3	22

Synchronization pattern: 01010110101001011010011010101111

register, clocks out the data at the correct time, resets the buffer registers and controls the acquisition of new data. The main control lines are the P and R signals, as the logical OR'ing of these lines is coincident with the sync and data periods of a frame. The shift registers are clocked out by a signal derived from a dual AND-OR-INVERT gate (MC7451). The 0^{o} phase clock is used and this is inhibited for the duration of "1" (the sync period). Two gates are used because of fan-out limitations of one gate.

Data from the buffer registers are normally transferred to the shift register at the beginning of the sync period. However, if an event is being processed at this time the shift should not take place. The decision is implemented by logic line W from the decision logic board , a logic "1" indicating no event is being processed. This W signal along with $\bar{P} \cdot \bar{R}$ ("1" during sync period), D (one half the clock rate) and the output of a D flip flop (MC7479) are applied to a 4-Input NAND gate. The flip flop's purpose is to prevent more than one preset pulse during each frame. The clock input to the flip flop is from a NAND gate (MC7420) whose inputs are $\bar{P} \cdot \bar{R}$ and the Q output of the flip flop. When the conditions for preset are satisfied, a 100 nanosecond one-shot (MC8601) is triggered to provide Y signal or "buffer clear." It also changes the state of the D flip flop used to inhibit further preset pulses. At the end of the synchronization period, the D flip flop is reset as the $\bar{P} \cdot \bar{R}$ signal goes to "0".

The preset signal is fed into a buffer (one half a quad NOR gate, MC7402) to provide the power to preset 96 bits in the shift register. This signal along with W and the output of a JK flip flop go to a NAND gate (MC7420), whose output is X, a signal used to control the acquisition of new data by controlling the discriminator strobe inputs (S_1/S_2 discriminator board) and gates on the decision logic board. The JK flip flop is used to inhibit acquisition of new data until after the buffer registers have been read out for an event that occurs during the data period of the frame. This is done by clocking (25 kHz 0^{o} clock) the state of $\bar{W}$ to the output of the flip flop, where the signal is summed with P + R ("1" during data period). The summed signal is used to hold the flip flop until the beginning of the next sync period.

The databit stream for the shift register is combined with the sync bit stream in an AND-OR-INVERT gate (MC7451) to form the composite frame.

The following outputs are used or available for use in other parts of the electronics:

$\bar{R}$: Frame rate for commutation

$\bar{P}\cdot\bar{R}$: Logic Events Control

Y: Reset buffers

X: Control Signal Gates

50 kHz clock

Four phases of 25 kHz clock

10. Azimuth Detector Board

The purpose of the azimuth detector is to determine the azimuth angle between the S_1, S_2 scintillators and the sun. This is accomplished by mounting phototransistors (32) on the periphery of the gondola that look out toward the horizon with large vertical acceptance angles. The outputs of the phototransistors, compared two at a time, then indicate the sun's position relative to the gondola. See Fig. 24, 25.

A clock line from the Data Encoder at the data frame rate is applied to two decade counters (CD4017D), a "units" and a "tens" counter. Following the 32nd clock pulse, a signal appears at the "3" output of the tens counter and the "2" output of the units counter. These are AND'ed together (CD4019D) and used to reset all the shift registers and the D flip flop. The next clock pulse (33rd) causes an output from the "33" AND gate, setting a logical "1" in the first bin of the "odd" bits bank of shift registers (CD4015D). This turns on the analog switch (CD4016D) associated with phototransistor #1. Likewise the 34th clock pulse enters a logical "1" into the "even" bits bank of shift registers ("odd" and "even" here referring to the labeling of the phototransistors.)

Hence with a "1" present in the first bin of both sets of shift registers, phototransistors #1 and #2 are connected through the analog switches to a differential comparator (MA710). It's output is a "1" or "0" depending on the relative amplitudes of the two input signals which are

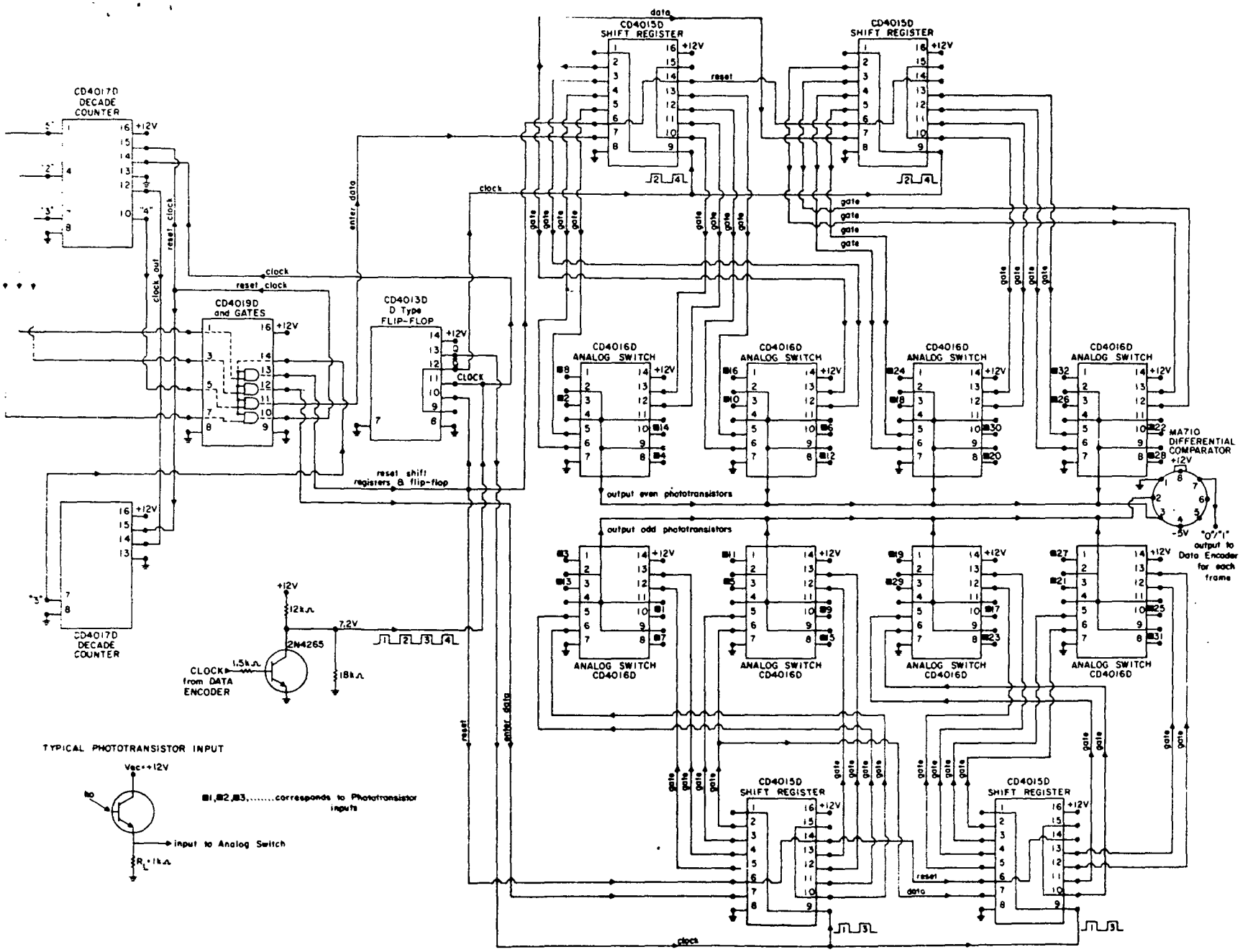


Fig. 24. Azimuth Detector Board Schematic

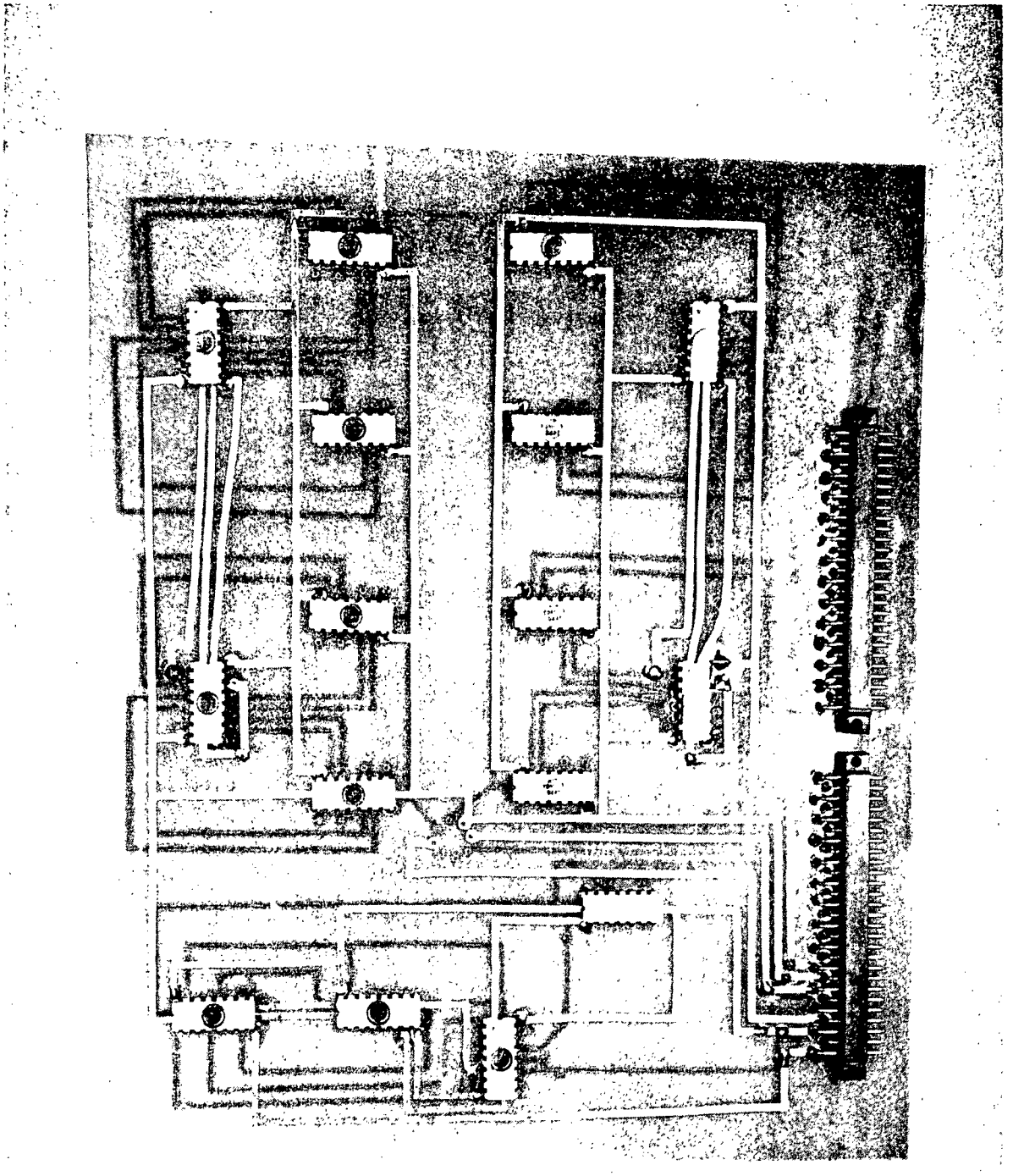


Fig. 25. Azimuthal Detector Board

proportional to the intensity of the light striking the phototransistors.

The 35th clock pulse causes an output from the "35" AND gate which resets both decade counters to zero. As clock pulses continue, the D flip flop alternately clocks the "even" and "odd" shift registers, and hence commutates through the 32 phototransistors. Phototransistors 1 and 2 are compared with the 34th clock pulse, 3 and 2 with the 35th pulse, 3 and 4 with the 1st clock and so on. Therefore a comparison of all 32 phototransistors is made, each frame indicating the comparison of another two. Examination of the differential comparator along with an identification signal thus provides the information on the relative amplitudes of the two input signals and the intensity of the light striking the phototransistors.

The 35th clock pulse causes an output from the "35" AND gate which resets both decade counters to zero. As clock pulses continue, the D flip flop alternately clocks the "even" and "odd" shift registers, and hence commutates the 32 phototransistors.

11. Temperature Monitor Board

The temperature monitor board measures the temperature at various selected locations in the experiment package to aid in data analysis. Temperatures to be monitored include the inside and outside of the gondola, the S_1 and S_2 scintillator tanks, batteries and various places in the electronics.

The monitor is basically a temperature dependent oscillator whose frequency is measured. See Fig. 26. The oscillator is a multivibrator that has thermistors switched sequentially into one of the collector loads. The resistance of the thermistor controls the charging rate of the timing capacitor and thus the period of the multivibrator.

The frequency is counted by a 12 bit counter (3-MC7493). After the counter is full (4096 counts), the output, after being translated to MOS logic levels, clocks a decade counter (CD4017D) one position. The outputs of the decade counter are connected to analog switches that place each thermistor in turn into the multivibrator circuit.

With the output of the binary counter connected to a bit in the data encoder shift register, the states of the last bit in the counter are observed. The time for the bit to go from "0" to "1" to "0" (4096 counts) gives the frequency (f=4096/time). Reference to a calibration curve of frequency vs. temperature provides the desired result.

12. Logic Events Board

Eight different counting rates are monitored sequentially by the system electronics, and are referred to as the logic rates. These counting rates are defined in the Table I, where the rate number, the detector logic and type of particle are given. A_1 refers to the anticoincidence detector around S_1, A_{11} and A_{12} refer to the top and bottom 45" x 41" sheets of scintillator in A_1, and A_{13} refers to the sum of the four

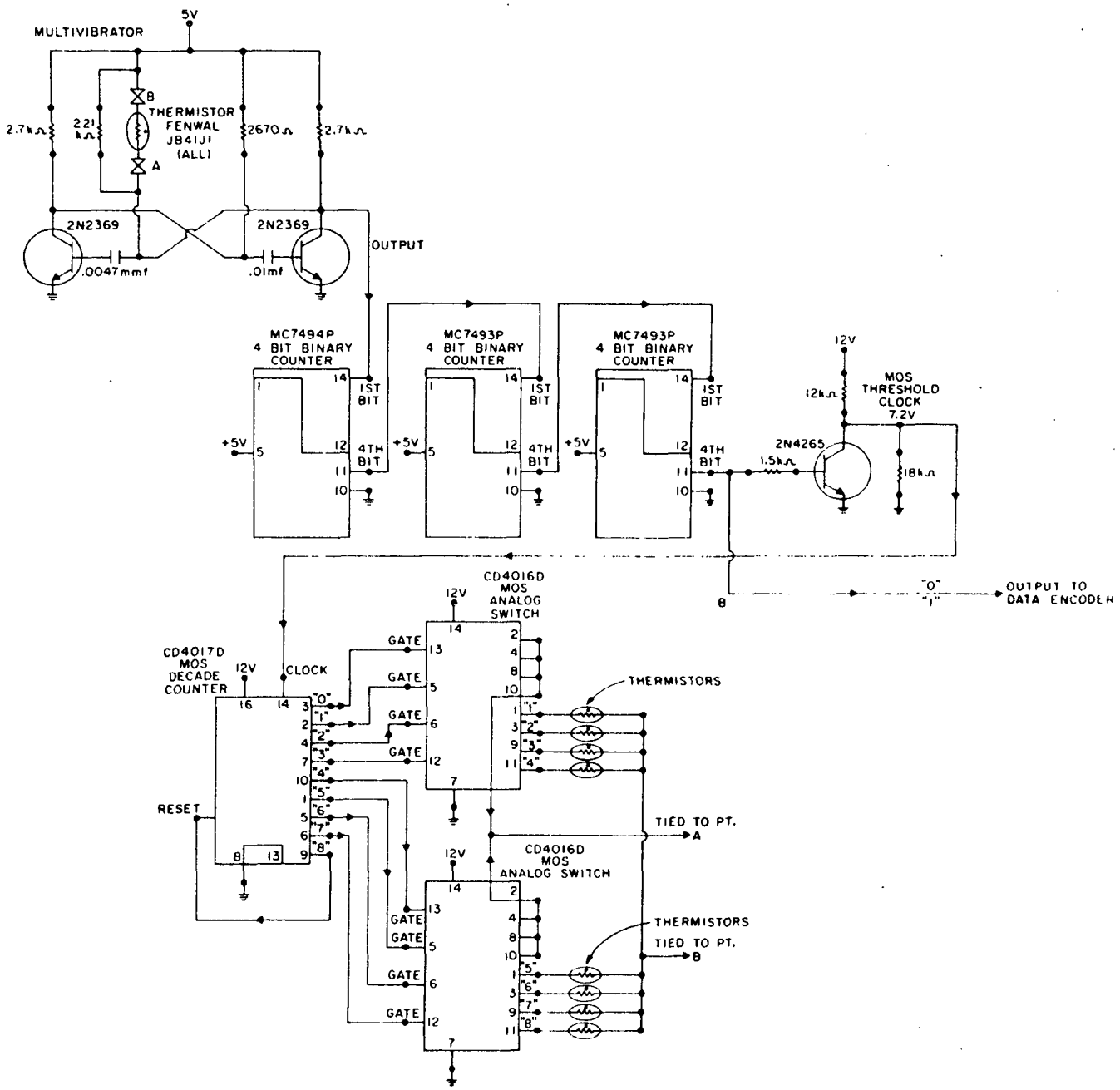


Fig. 26. Temperature Monitor Circuit Schematic

TABLE I

Rate	Detector Logic	Type of Particle
1	$\bar{A}_1\ S_1\ S_{22}\ \bar{A}_2'$	Neutrons and γ-rays
2	$A_{11}\ S_1\ A_{12}\ \bar{A}_{13}\ A_{21}\ S_2\ \bar{A}_{22}\ \bar{A}_{23}$	Medium energy charged particles
3	$\bar{A}_1\ S_1$	γ-rays
4	$\bar{A}_2\ S_{21}$	γ-rays
5	$A_{11}'\ S_1\ A_{12}\ \bar{A}_{13}\ A_{21}'\ S_2\ A_{22}\ \bar{A}_{23}$	Multiply charged penetrating particles
6	$A_{11}\ S_1\ \bar{A}_{12}\ \bar{A}_{13}$	Low energy charged particles
7	$A_{11}\ S_1\ A_{12}\ \bar{A}_{13}\ A_{21}\ A_{22}\ S_2\ \bar{A}_{23}$	Penetrating particles
8	$A_{11}\ S_1\ A_{12}\ A_{21}\ S_2\ \bar{A}_{22}\ \bar{A}_{13}\ \bar{A}_{23}\ S_1'$	Electrons, downward moving
9	$A_{11}\ S_1\ A_{12}\ A_{21}\ S_2'\ A_{22}\ \bar{A}_{13}\ \bar{A}_{23}\ S_2$	Penetrating particles, upward moving

curved sheets of A_1 (sides). An identical notation identifies the A_2 components. S_2', S_{21}, S_{22} and S_2 refer to the S_2 scintillator; the differences are in the delay and pulse width of the logic signals derived from S_2. Similarly, S_1' and S_1 refer to the S_1 scintillator. A_{11}' and A_{21}' have high signal threshold requirements. A bar across a detector reference demands an absence of a signal from that detector.

The schematic of the electronics on the logic events board is shown in Fig. 27 . All gates used in this board are OR (or NOR) but negative logic is employed over most of the board ("0" = TRUE), converting these to AND (or NAND) gates, and will subsequently be referred to as AND gates.

In order that these events correspond to the indicated type of particle, stringent timing and threshold requirements have to met, resulting in 19 separate logic inputs from the 8 detectors. The correspondence of the inputs with a specific detector, together with the pulse width and delay from the time of origin are shown in Table II. The logic event inputs generated on the various adder boards are connected to the LEB (logic events board) via twisted wire pairs, feeding into a series of line receivers (MC 1020). The line receiver outputs are connected to AND gates (MC1004 and MC1006) to produce the logic rates shown in Table I. The use of two different gates here results in a power saving feature, as the MC1004 has output pull-down resistors which are omitted on the MC1006. In those cases where 8 input signals are

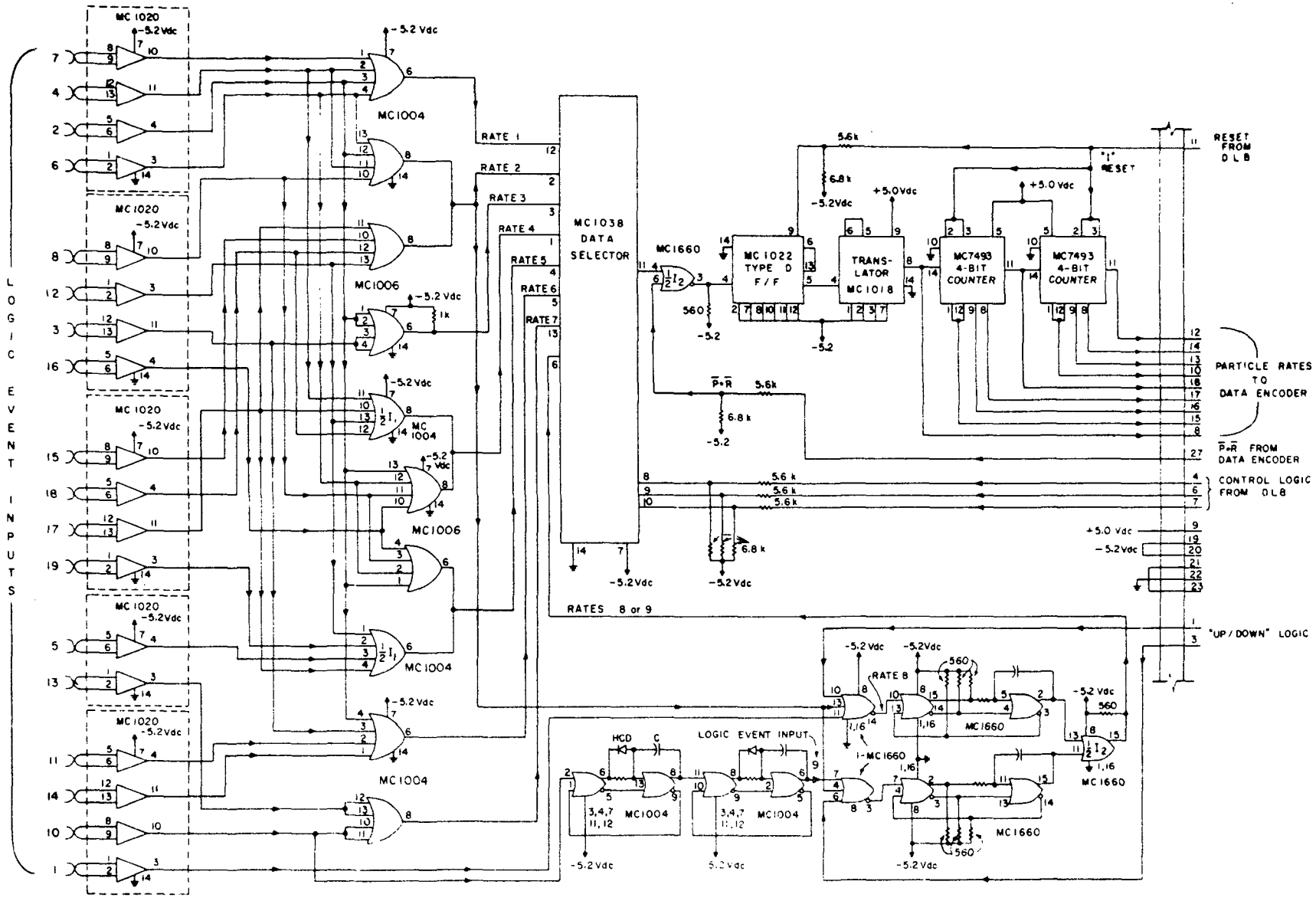


Fig. 27. Logic Events Board Schematic

TABLE II

Logic Input	Detector	Delay (nsec)	Pulse Width (nsec)
1	S_1'	0	103
2	S_1	95	20
3	$\bar{A}_1$	90	75
4	A_{11}	95	21
5	A_{11}'	95	21
6	$\bar{A}_{13}$	75	45
7	$\bar{A}_{12}$	75	45
8	A_{12}	92	23
9	S_2'	85	20
10	S_{21}	15	20
11	S_{22}	15	95
12	S_2	70	43
13	$\bar{A}_2$	0	50
14	$\bar{A}_2'$	0	115
15	$\bar{A}_{22}$	65	55
16	A_{22}	70	43

Logic Input	Detector	Delay (nsec)	Pulse Width (nsec)
17	$\bar{A}_{23}$	65	55
18	A_{21}	70	43
19	A'_{21}	80	40

AND'ed output wired OR'ing is used. Hence an MC1006 is combined with an MC1004 as only one pull-down resistor is needed.

Input 9 is generated from Input 10, which operates a 50 nanosecond one-shot constructed from two MC1004 OR/NOR gates. Another 20 nanosecond one-shot following is triggered after the first one-shot turns off, resulting in a 20 nanosecond pulse delayed 50 nanoseconds from the input.

Rates 1 through 7 are available directly from the outputs of the AND gates, and represent seven of the eight input rates that are commutated thru by the data selector, MC 1038. The control for this selector comes from the decision logic board and advances the data selector one position each telemetry frame. The eighth input (Rate 8) represents downward moving electrons on one commutation cycle and upward moving (Rate 9) penetrating particles on the next cycle.

Logic input 1 and Rate 2 are two inputs to a MC 1660 gate along with the "UP/DOWN" logic signal, to form Rate 8, corresponding to electrons. Derived input 9, Rate 7 and the "UP/DOWN" logic are the inputs to anoter gate, forming Rate 9, or upward moving penetrating particles. The outputs of these two gates are stretched 20 nanoseconds, OR'ed and applied as the eighth input of the data selector.

The output of the data selector is gated by the $\bar{P} \cdot \bar{R}$ signal from the encoder, so that counts accumulate during the time that the 96 data bits are being read out. The 9-bit counter consists of a D type flip-flop (MC 1022) and two 4-bit counters (MC 7493). The nine outputs control the state of 9-bits of the shift register in the data encoder.

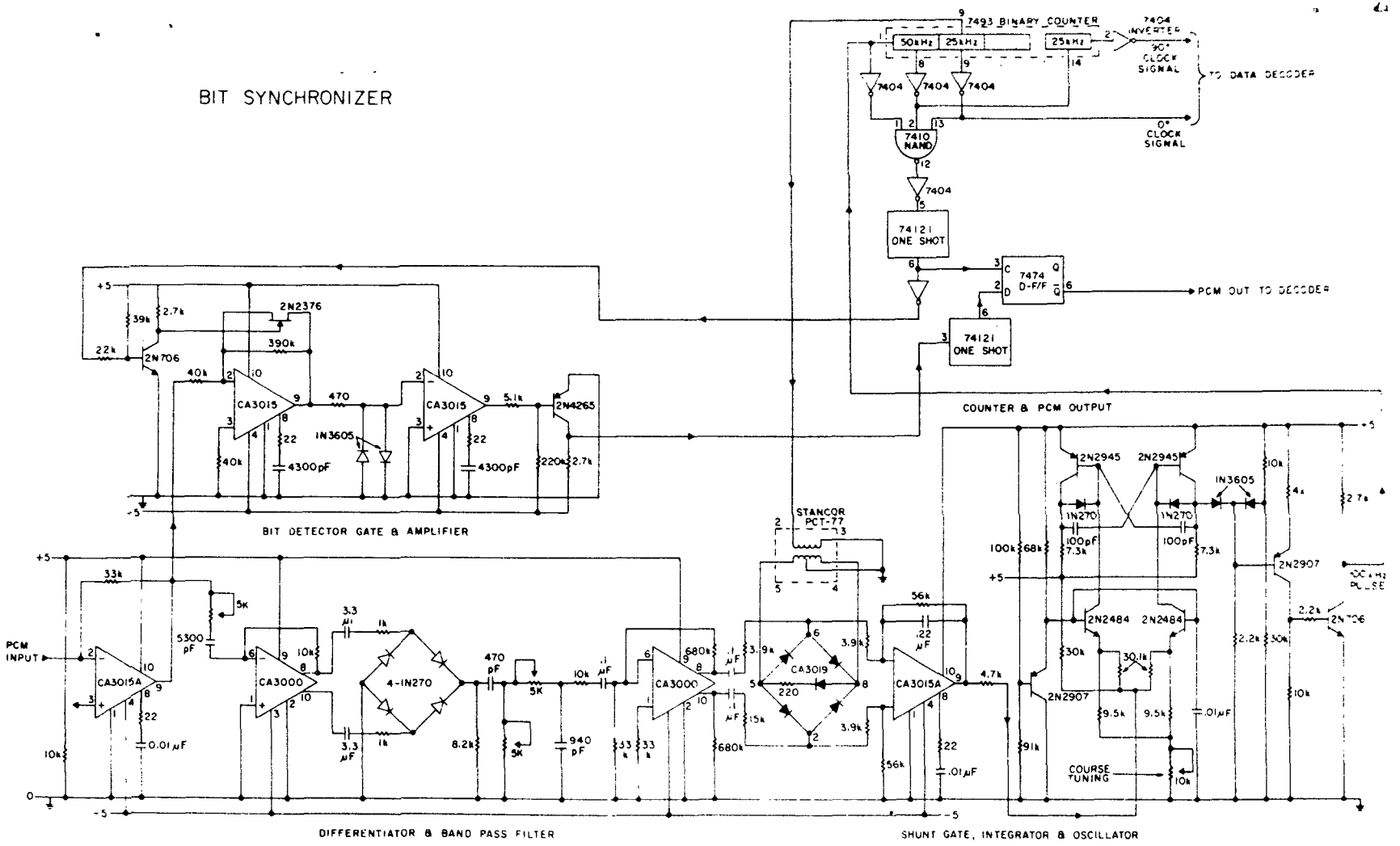


Fig. 28. Bit Synchronizer Circuit Schematic

13. Power Conditioning Board

Power for the experiment will be supplied by Yardney Silver cells, arranged as packs of 6.0 volts, each with 80 ampere-hour rating.

Those sections requiring regulation (all TTL and ECL circuits for example) will be supplied regulated voltages using IC regualtors with or without external pass transistors depending on the particular load requirements. The IC regulators will be types MC 1463 and MC 1469.

14. Bit Synchronization

A PCM telemetry system requires time synchronization of the ground data decoding equipment with the airborne PCM generator. The purpose of a bit synchronizer is therefore to generate a ground clock in sync (but with a permitted phase difference) with the airborne clock. Once the ground clock is generated, it is then used to "clean up" the telemetered PCM which may have been subjected to fading or other distortion. The synchronization used here is a phase-locked loop with the loop oscillator locked in sync with the airborne clock. The bit synchronizer thus provides clean PCM data along with necessary clock phases to the data decoder.

The bit synchronizer is composed of four principal parts (see Fig. 28), a differentiator/doubler/filter section, a shunt gate/integrator/oscillator section, a bit detector gate/amplifier section and a counter/PCM output section.

The differential/doubler/filter section receives the raw PCM input signal. After buffering and level shifting in the

input amplifier (CA3015), the signal is differentiated in the second stage (CA3000), with a balanced differential output. Each pulse corresponds to a level transistion at the input. The output is full wave rectified (4-IN270 diodes) and filtered in a three section RC bandpass filter. After amplification (CA3000), the balanced differential output is applied to a shunt gate.

In the shunt gate/integrator/oscillator section, the input signal from the previous section is applied to a shunt gate (CA3019) along with a 25 kHz gate drive signal derived in the counter/PCM section. When the loop is locked, the gate drive frequency is identical to the input frequency, except for a phase difference. This phase difference appears as a dc voltage out of the gate that is amplified and integrated (CA3015) and the error voltage is then applied to an astable multivibrator used as the loop oscillator. The error voltage controls the charging current for the timing capacitors and so varies the frequency. A coarse frequency control is incorporated to achieve initial lock, after which the feedback maintains lock. The oscillator signal (100 kHz) is buffered and applied to the counter/PCM section.

The oscillator signal fed to counter/PCM section is devided by two (50 kHz), then divided by two again (25 kHz). This 25 kHz signal is fed back to the shunt gate. The oscillator, the 50 kHz and 25 kHz signals are each inverted and fed to a NAND gate, whose output is also inverted. Thus

once every 1/25 kHz = 40 microseconds, a 10 microsecond pulse is generated. This pulse triggers a one-shot (SN74121) for a period of 23 microseconds. This one-shot signal is fed to the bit detector gate/amplifier section.

The 23 microsecond one-shot signal is used to operate a gate that has the buffered PCM input signal applied. With the one-shot pulses at a 25 kHz rate, the gate is opened whenever it's possible for a new logic level to be present. With the NRZ telemetry format, each logic level is held for the full period, i.e. a "1" will be held at a "1" level for 40 microseconds and if the following bit is also a "1", the logic level simply remains at the "1" level for another full period. The gating signal (23 microseconds) is adjusted to fall inside a given data bit's period, so the output of the gate will be a series of 23 microsecond pulses when "1" is present at the input. These pulses are squared up by a diode limiter circuit and amplified and are fed back to the counter/PCM section.

The restructured PCM pulses operate a one-shot of 32 microseconds in the counter/PCM output section. These pulses are applied to a D flip flop and clocked out using the 23 microsecond wide pulse stream. The outputs therefore are clean PCM signals along with two clocks lines, at 0^{o} and 90^{o} phase, in synchronization with the PCM.

15. Data Decoder

The equipment consists of two standard 7" x 19" panel mounted chassis. The first contains the electronics and programming functions and the second a neon display of the PCM bit pattern. The electronics section is entirely TTL integrated circuit logic. It consumes 15 watts at 5 volts while the neon display consumes 20 watts at 135 volts.

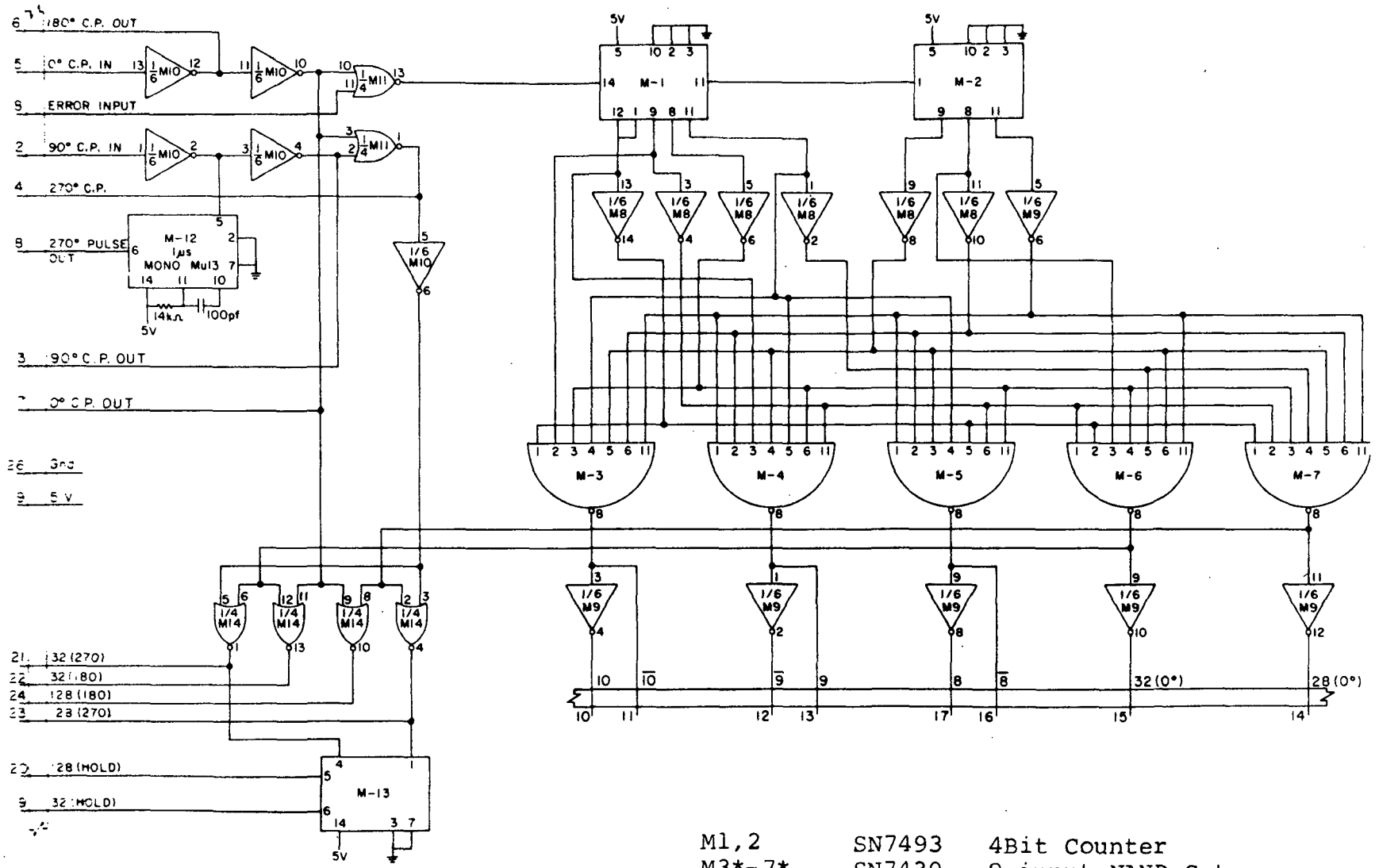
The electronics section may be divided into several functional units, the counting unit, synchronization circuit board, error counters, data control board, and data storage. The main counting unit receives an input clock from the bit synchronizer and generates all necessary internal timing pulses. The synchronization board inspects the incoming data to find the correct synchronization pattern. The bit errors entered in this board are counted in the error counter board which gives an output pulse to the counting unit causing it to shift the bit stream by one bit. In this manner, the bit stream is inspected until the synchronizing pattern is found. The search and lock modes are provided in the error counter board to insure that the identified pattern is the true synchronization pattern and to prevent the unit from searching due to bit errors caused by atmospheric noise or other transient phenomena.

The data control board provides the proper driving fan out for the S/R clocks and storage latch transfer pulses. Circuitry is provided to read out several 8, 0 and 10 bit words for analysis. A timing circuit is also incorporated so that

transfer of the bit stream to temporary storage may be carried out on a continous or a timed basis. The event interrogator compares event bits in storage with the incoming bit stream to determine the presence of a new event. The event pulse generated is used to trigger the serial word output in a manner such that the output is obtained only when the unit is locked onto the bit stream and a verified signal is present.

A. Main Counting Unit. Both clock phases (0^{o} and 90^{o}) required for operation of the data decoder are initially inverted to provide both isolation from the driving source and the complimentary phase clock for internal timing purposes. A second inversion then reconstructs the initial clock phases. In the case of the 90^{o} clock, the inverted phase (270^{o}) is gated with the 180^{o} clock to provide a 360^{o} cutoff. An inverted 0^{o} clock is gated with the 270^{o} error output from the error counters board and drives a 7 bit binary counter, made from the 4 bit counters M1 and M2. The error input is used to provide an extra count in the timing unit to search the bit stream (see explanation in error counter description). See Fig. 29.

The outputs of the 7 bit counter are inverted and the proper combination of inverted and normal outputs are used to provide internal timing pulses by appropriate gating in the 8 input NAND gates M3-7. These gates provide timing pulses at the 8th, 9th, 10th, 32nd, and 128th clock pulses. The 32nd and 128th pulses are gated with 0^{o} and 90^{o} clock pulses to



M1,2	SN7493	4Bit Counter
M3*-7*	SN7430	8-input NAND Gate
M8*-10*	SN7404	Hex inverters
M11*,14*	SN7402	Quad 2-input NOR Gates
M12*	SN74121	Monostable Multivibrators
M13*	SN7474	D-Flip Flop

*Pin14: Vcc(5V); Pin 7: Ground

Fig. 29. Data Decoder - Main Counting Unit.

provide both 180° and 270° phases for these pulses, necessary for internal timing requirements.

The 270° clock pulse is also used to drive multivibrator M12 which provides a 1 microsecond pulse at 270° during each clock period that is used for internal timing.

The 32nd (270°) and 128th (270°) pulses are applied to the preset and clear inputs of D-flip flop M13. The output of M13 is used to provide gating for the data and I.D. sections of the bit stream. These outputs are referred to as 32 (270°) hold and 128 (270°) hold, respectively.

B. Synchronization Board. At the initiation of each frame, the 128 (270°) hold is applied to a NAND gate (¼S19, Pin 2) simultaneously with the data input. This allows the following 32 bits to be clocked into the 5 bit Shift Registers, S1-7 on the 90° clock. An input inverter 1/6S18, Pin 9 is provided for normal-inverted sync pattern. The 32 (0°) and 90° latch clock (derived from the output of multivibrator S20) are gated and open the storage latches for parallel storage of information from the S/R's. The latch clock must have a lower cutoff than 180° so as not to interfere with the subsequent operation of the identification cycle (See Fig. 30).

The latch outputs are all inverted so that either the normal or inverted latch output is available for application to the preset input of the appropriate bit in the S/R's (i.e. latch position 27 must be connected, either normal or inverted, to preset input of bit 27 of the S/R's).

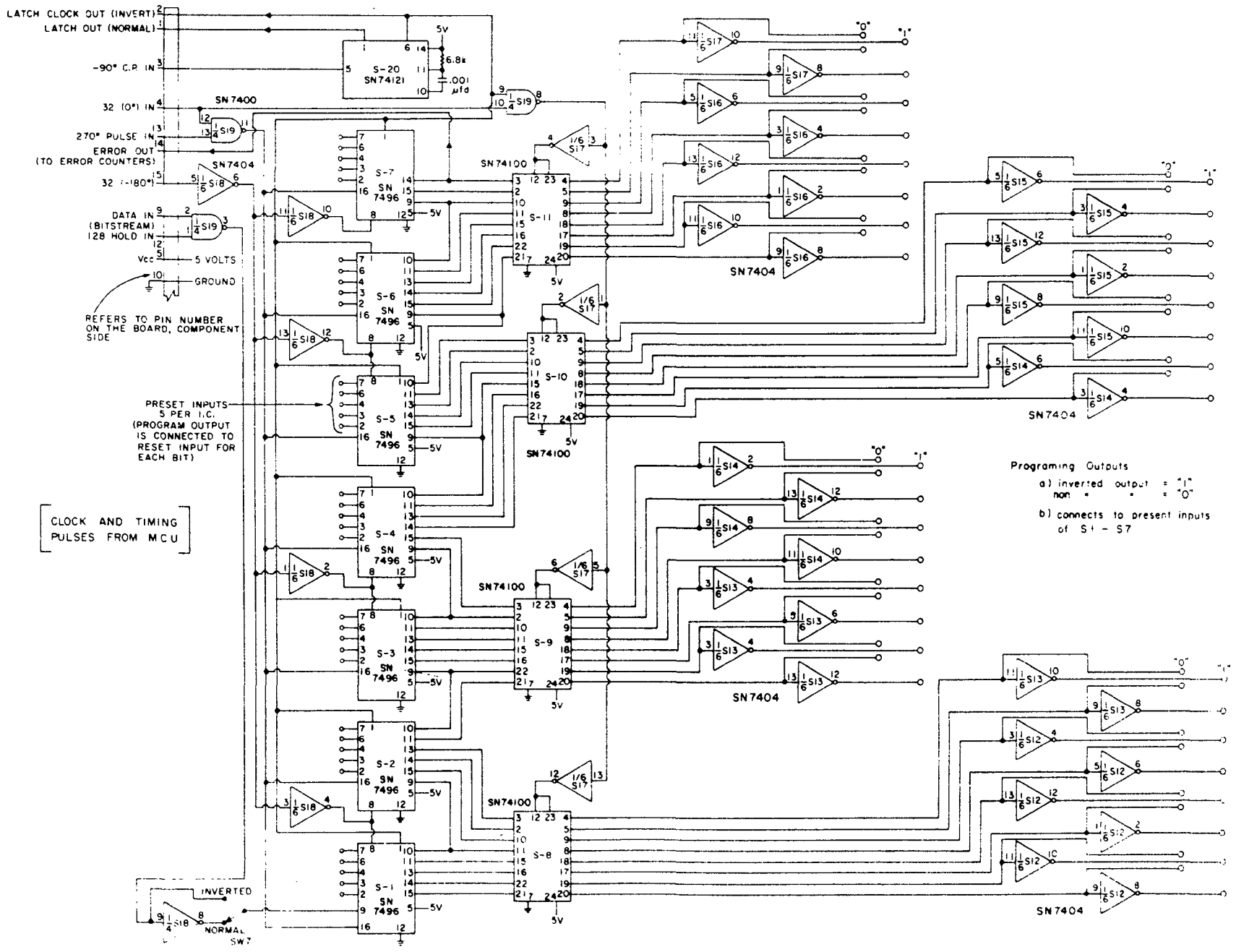


Fig. 30 Data Decoder - Sync Board

The 32 (180^{o}) pulse is applied to the preset enable of the S/R's, while the 270^{o}, 1 microsecond pulse is gated with the 32 (0^{o}) pulse and the inverse is applied to the clear inputs. The programming logic is as follows:

1.) the inverted latch output corresponds to programming a "1" for the particular bit being considered. The normal output represents a "0".

2.) e.g. suppose a bit is programmed for a zero (normal latch out connected to preset input), and a "1" is clocked into this position at the 32nd clock pulse. A "1" then appears at the preset enable, and at 32 (180^{0}) is shifted into the S/R. Since preset overrides clear, the "1" remains in this position at the end of the identification procedure.

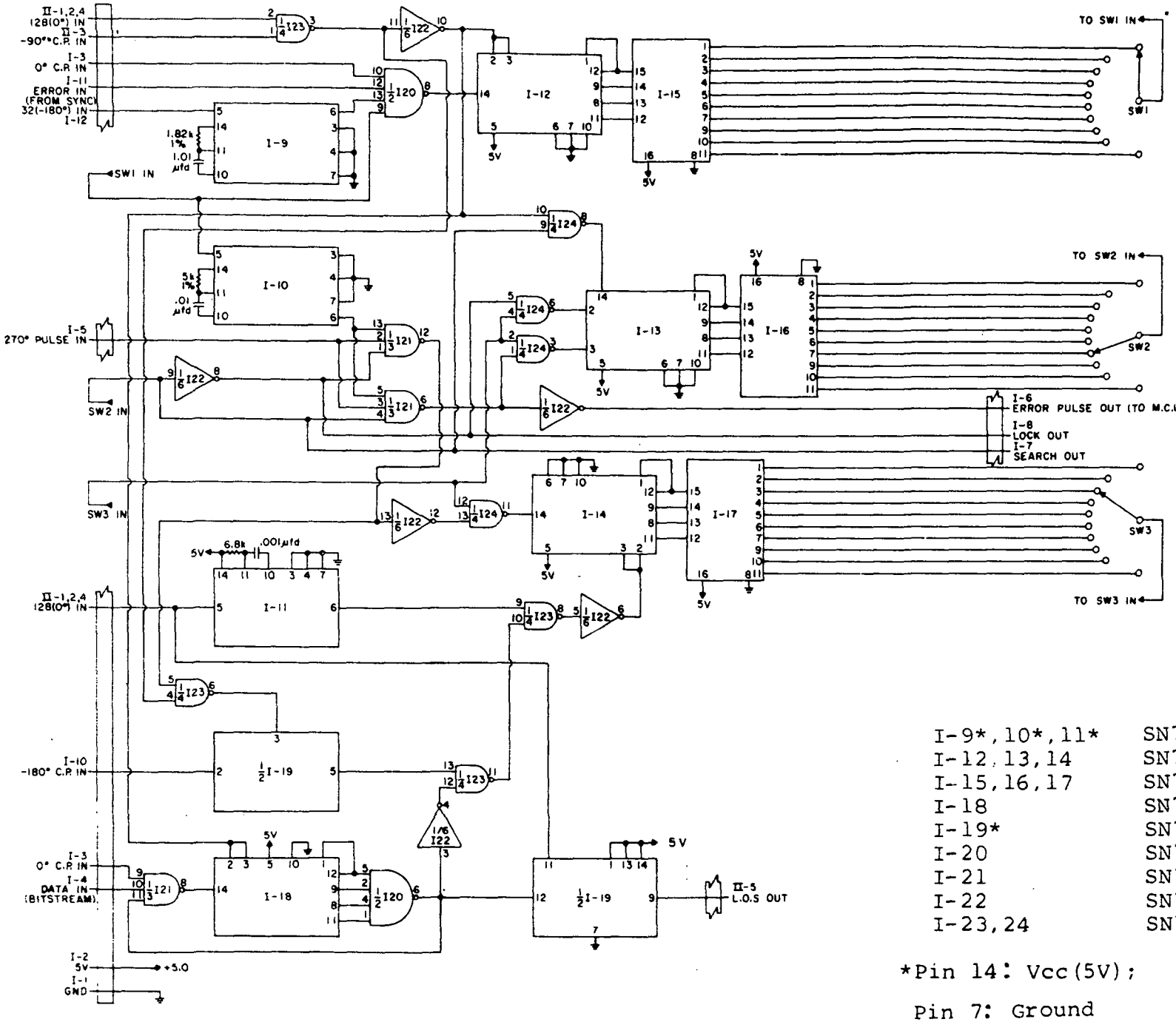
3.) A similar analysis is made for "0" programming.

When all the errors have been entered into the S/R's, the number of bit errors is then serially clocked out to the error counters board.

C. Error Counters Board: The bit error output from the sync board is clocked into the first decade counter (I12) of this board and accumulates the number of bit errors registered in the identification cycle. Gating to this counter insures the counting of errors only in the 32 bits succeeding the identification cycle, and only until the counter has achieved the desired number of counts. Decoder I15 is used to give a decimal selector for bit error programming (front panel switch SW-1). See Fig. 31.

Upon reaching the desired count, the falling edge of the output of 10 position switch SW-1 triggers multivibrator I10 which provides a gating pulse to NAND gates I21. If the unit is in the search mode, the 270^{o}, 1 microsecond pulse is gated to the main counting unit error input and the reset gates of decade counter I13. If in the lock mode, the 270^{o} pulse is gated to decade counter I14.

(1) Search. In the search mode, decade counter I14 counts 90^{o} frame rate pulses until a desired number of counts are reached. When the count is reached, the selected output from decoder I16 provides a negative pulse to the input gate of the counter, thus closing the input to further frame rate pulses. Until the desired count is reached, the decoder output is in the "1" state and thus is applied in a normal fashion to 1/3 I21 Pin 4 and inverted to 1/3 I21 Pin 1. The first gate provides routing of the 270^{o} pulse to the Main Counting Unit and the reset gates of I13. The



I-9*, 10*, 11*	SN74121
I-12, 13, 14	SN7490
I-15, 16, 17	SN7442
I-18	SN7493
I-19*	SN7474
I-20	SN7420
I-21	SN7410
I-22	SN7404
I-23, 24	SN7400

*Pin 14: Vcc(5V);

Pin 7: Ground

Fig. 31. Data Decoder - Error Counters

second sends the 270^{o} pulse to decade counter I14 when in the "lock stage."

When the unit is in the search mode, the reset gates of I13 are enabled, allowing this counter to return to zero every time the desired number of bit errors is exceeded. When the desired search frame count has been reached, the unit is then locked onto the sync pattern.

(2) Lock Mode. In the lock mode, the 270^{o} error pulse, if present, is not routed to the Main Counting Unit, but to the input gate of I14. In the absence of an error pulse, the inverse 90^{o} frame rate is applied to the clock input of D flip flop I19 Pin 3, thus clocking a "0" into this unit (the D input is a 180^{o} clock pulse). The Q input is gated with the signal loss indicator and enables the reset gate of I14 which causes this counter to be reset to zero by the 5 microseconds output of the multivibrator I11 (activitated by the 0^{o} frame rate pulse). If an error pulse is present, a "1" is clocked into I19 Pin 3 thus disabling the reset gates. The error pulse is simultaneously applied to the input gate of the counter, the output of decoder I17 enabling this gate. In this manner if a consecutive specified number of frames with bit errors exceeds a desired number decoder I17 changes to a zero state, disabling the input gate to I14 and resetting I13 to zero, thus re-initiating the search mode.

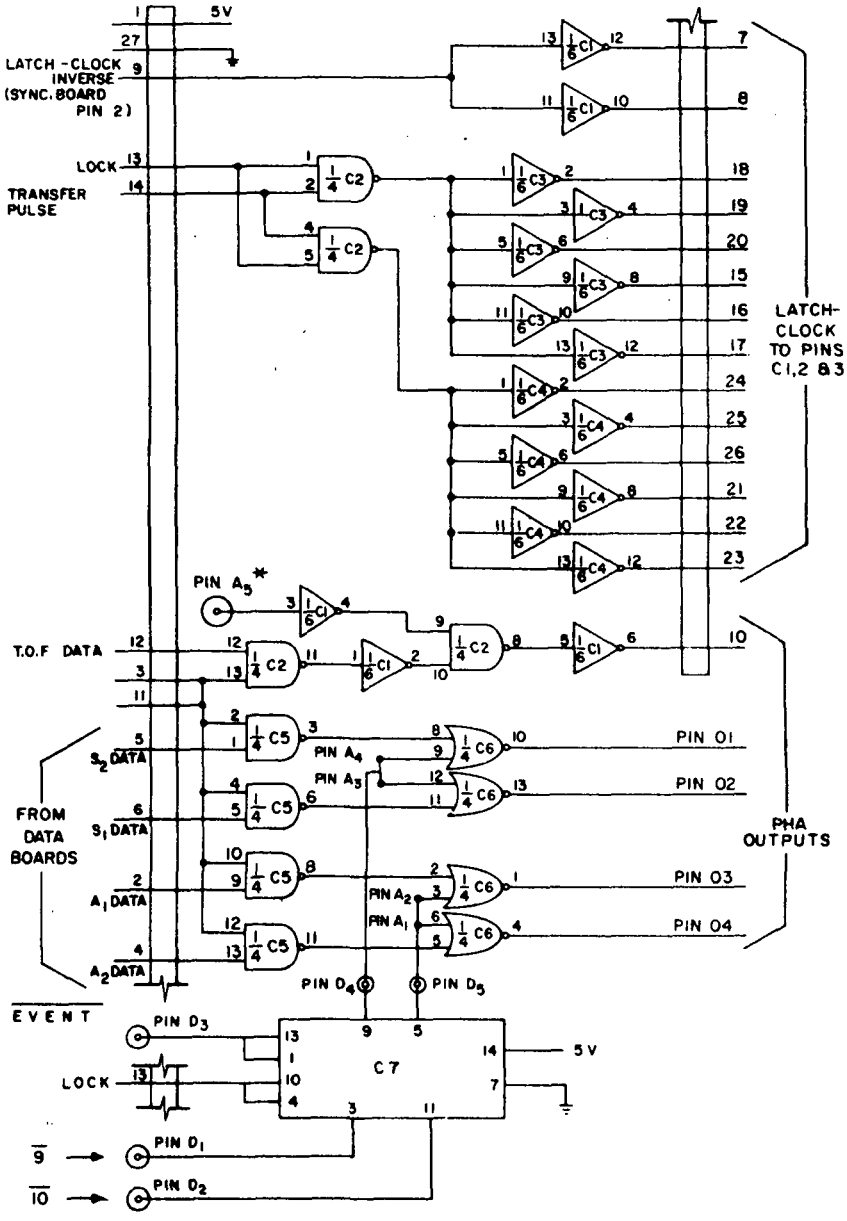
This procedure prevents time lost in reverting to "search" when an excessive number of bit errors occur in a

non-receptive manner (such as might be caused by transient atmosphere interference with the telemetry signal).

The loss of signal indicator counts the data bits applied to I18 and must count 16 "1" bits to insure that the signal is preset (logic "1" appears 18 times in the sync pattern). Upon reaching the count, the decoded output disables the input gate and enables the reset gate of I14. The decoded output is also applied to D flip flop 1/2 I19 Pin 12 for temporary storage.

D. Data Control Board. The data control board contains the clock drivers for the data boards and the serial output gates for the words to be pulse height analyzed. The latch clock (multivibrator S-20) from the sync board is applied to inverter drivers to provide the proper fan-out for the data board S/R clocks. This clock is also gated with the transfer pulse and then applied to the latch inverter drivers to provide parallel data transfer to the Data Storage Latches.

The serial P H A output is generated as follows (See Fig. 32). The inverse event pulse is applied to the clear input of C-7. The preset input is connected to the lock output (from error counters) and the D-input is held at a "1" level. The clock is the 8, 9 or 10 inverse pulse. In this manner, a "0" output of 8, 9 or 10 bit length is available at the Q output. The data to be pulse height analyzed is gated with a 180^{o} clock and this output is applied to a "NOR" gate, the other input of which is the Q output of the above flip flop.



C-1*	SN7404	Hex inverter
C-2*,5*	SN7400	Quad NAND
C-3*,4*	SN7404	Hex Inverter
C-6*	SN7402	Quad NAND
C-7*	SN7474	D-Flip Flop

*Pin 14: Vcc(5V); Pin 7: Ground

Fig. 32. Data Decoder - Data Control Board

The output of the NOR gate is then the information contained in the 8, 9 or 10 bits immediately following the event pulse. These bits may be taken from any portion of the bit stream (from the data S/R) and thus any 8, 9 or 10 bit word may be serially clocked out of the bit stream. The lock function at the preset input is provided to insure that a word will not be inspected when the bit stream is not locked in.

E. Event Interrogator and Storage Transfer Time (Auxiliary Data Control Board). The I.C's on the rear third of the error counters board and the auxiliary data control board form a functional unit (See Fig. 33).

An inverse event pulse applied to the B input of multivibrator E-5 while input A-3 is connected to "search", generates a 12 bit-width pulse at the $\bar{Q}$ output when the data decoder synchronizer is in the lock mode. This output activates a NOR gate allowing a 270^{o} clock pulse to be applied to the clock inputs of S/R's E-1, 2 and 3. At each new event, the event information is then clocked into these S/R's and this data is compared at the frame rate with the bit stream accumulated in S/R's D-3, 4 and 5 of the first data board by means of exclusive NOR gates I-1, 2 and 3. The gate outputs are combined in NAND gates I-4 and 5 and a pulse indicating an event appears if any one of the data bits differ from the bits held in storage in E 1, 2 and 3.

Transfer of the bit stream to storage (Fig. 34) is effected by either this event pulse or the framerate pulse selected by SW-4, on a continuous or timed basis (SW-5). The timing mechanism is triggered by the trailing edge of the transfer to storage pulse and enables multivibrator I-8 to be fired by the rising edge of the next frame rate pulse. This inhibits the transfer pulse until the multivibrator returns to the quiescent state. Two decade counters are provided to give three orders of magnitude in the inhibiting time for the transfer pulse.

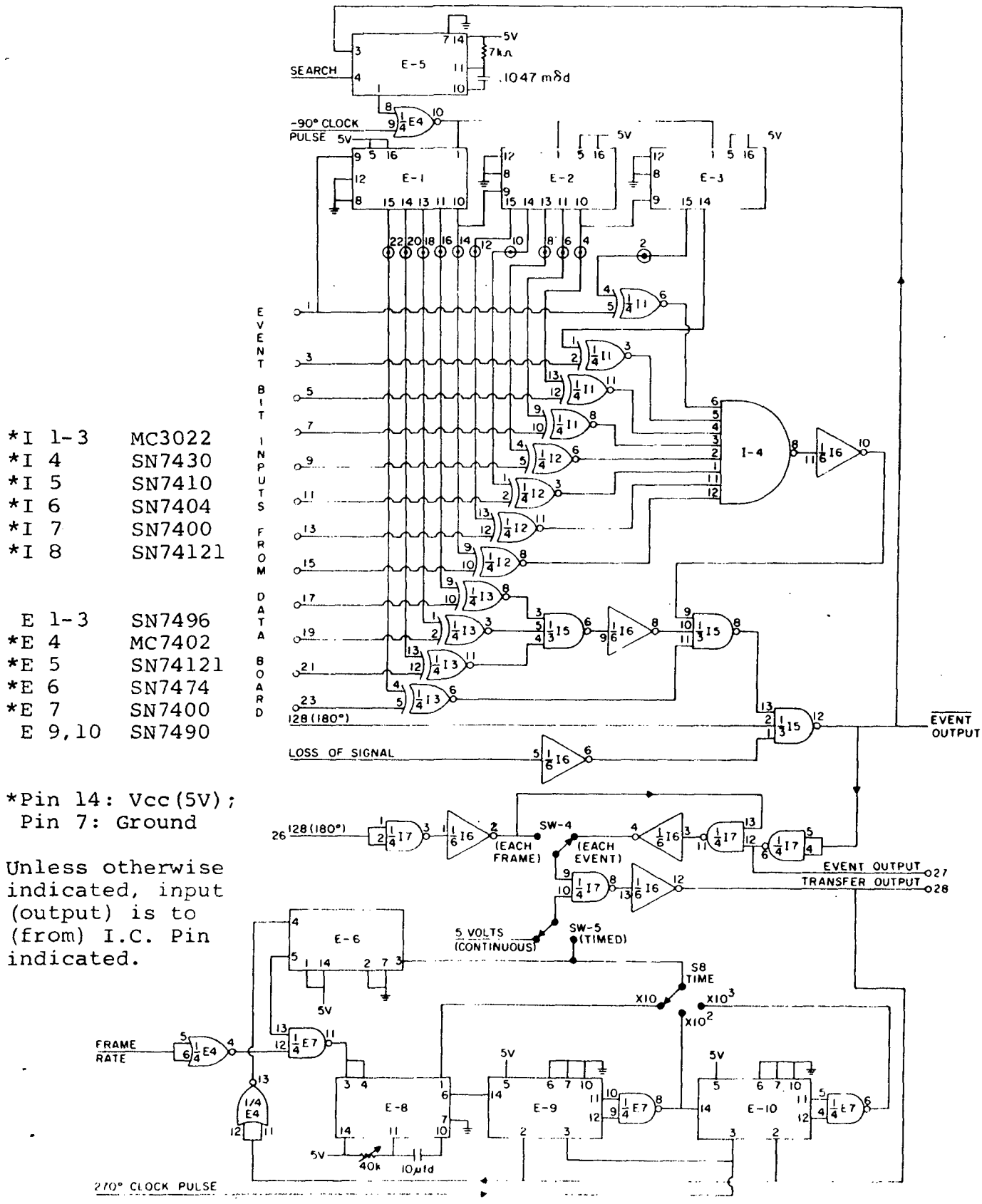


Fig. 33. Data Decoder - Event Interrogator & Transfer Timer

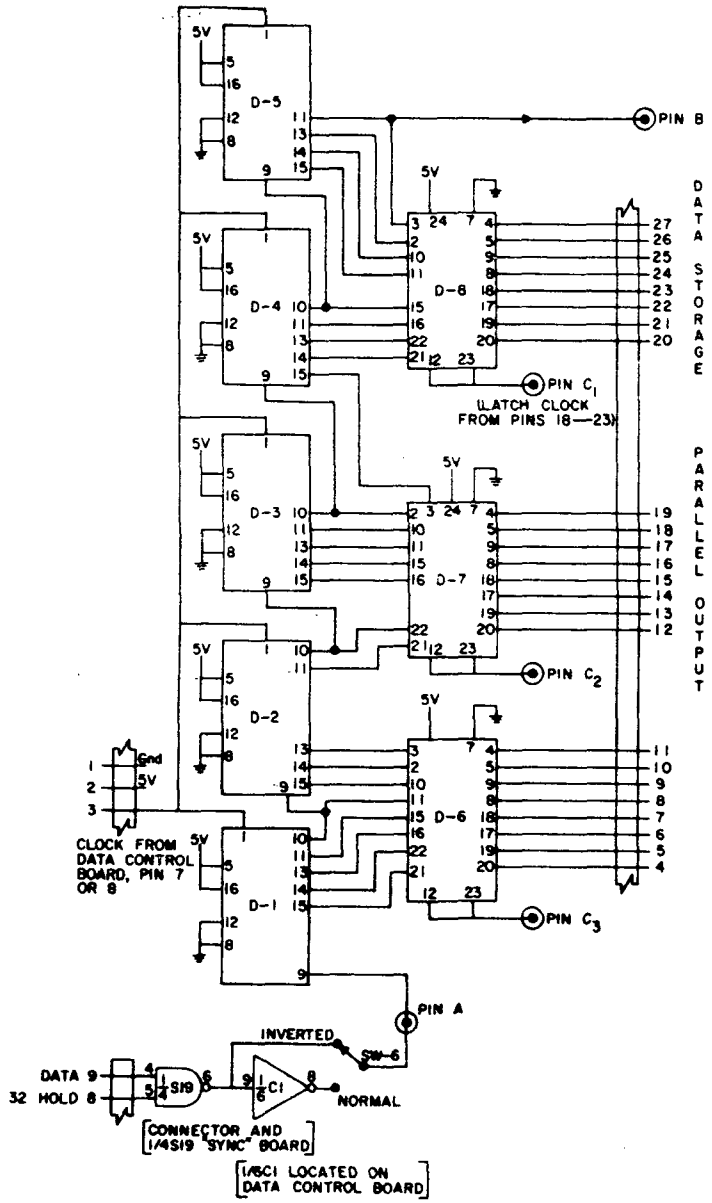


Fig. 34. Data Decoder - Data Board.

D 1-5 SN7496 5 bit S/R
D 6-8 SN74100 8 bit Latch

4 identical serial in-parallel storage out data boards have been contructed. Wiring differences are noted below:

Board 1) a) Parallel output D-5(14,15), D-4(10,11,13,14,15) and D-3(10 11,13,14,15) to event interrogator
b) Serial word out (PHA-S_1) from D-2 Pin 10 to control board

2) a) Serial word out (PHA-S_2) from D-4 Pin 14 to control board

3) a) Serial word out (TOF) from D-5 Pin 13 to control board
b) Serial word out (PHA-A_1) from D-3 Pin 13 to control board

4) a) Serial word out (PHA-A_2) from D-4 Pin 10 to control board

Photographs of the front and rear views of the data decoder are seen in Figs. 35 and 36.

16. Acknowledgments

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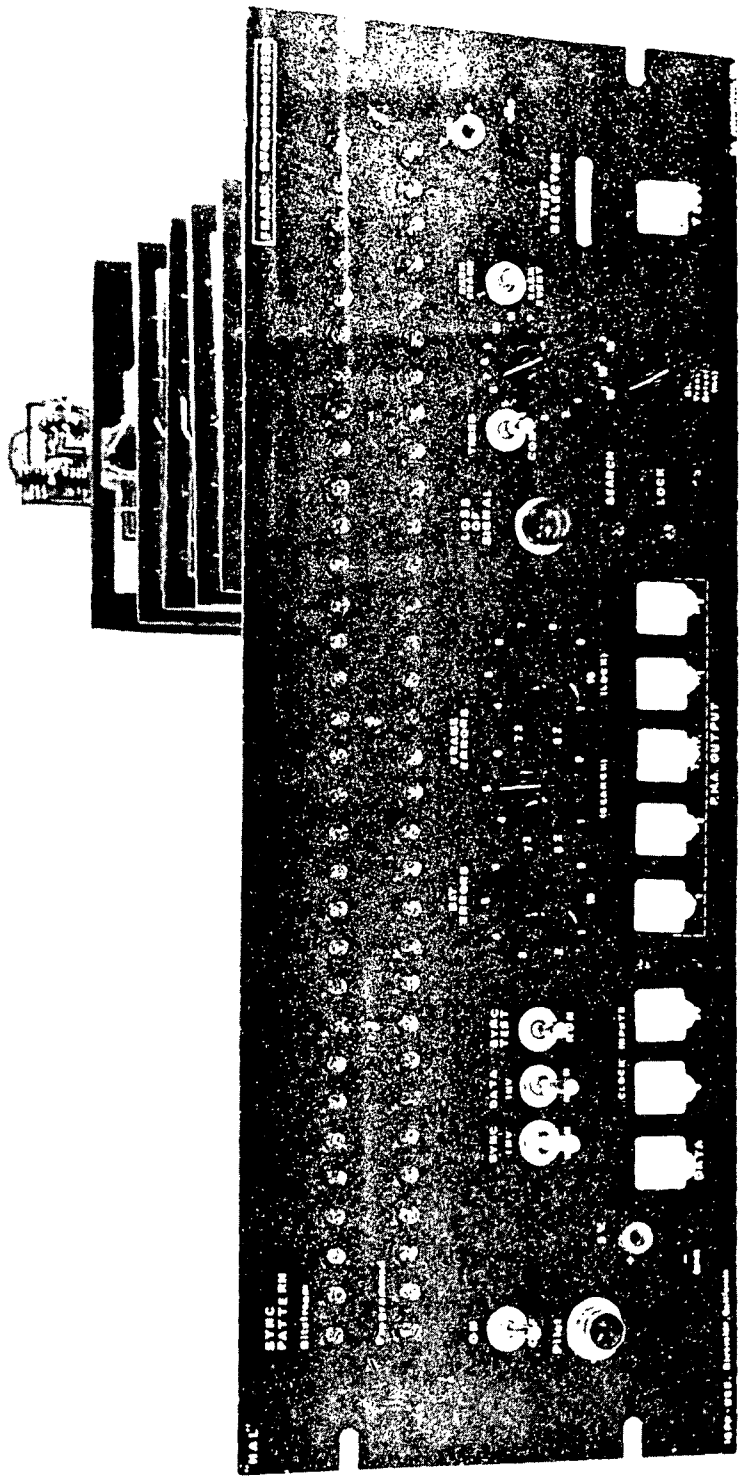

Fig. 35. Data Decoder Front View

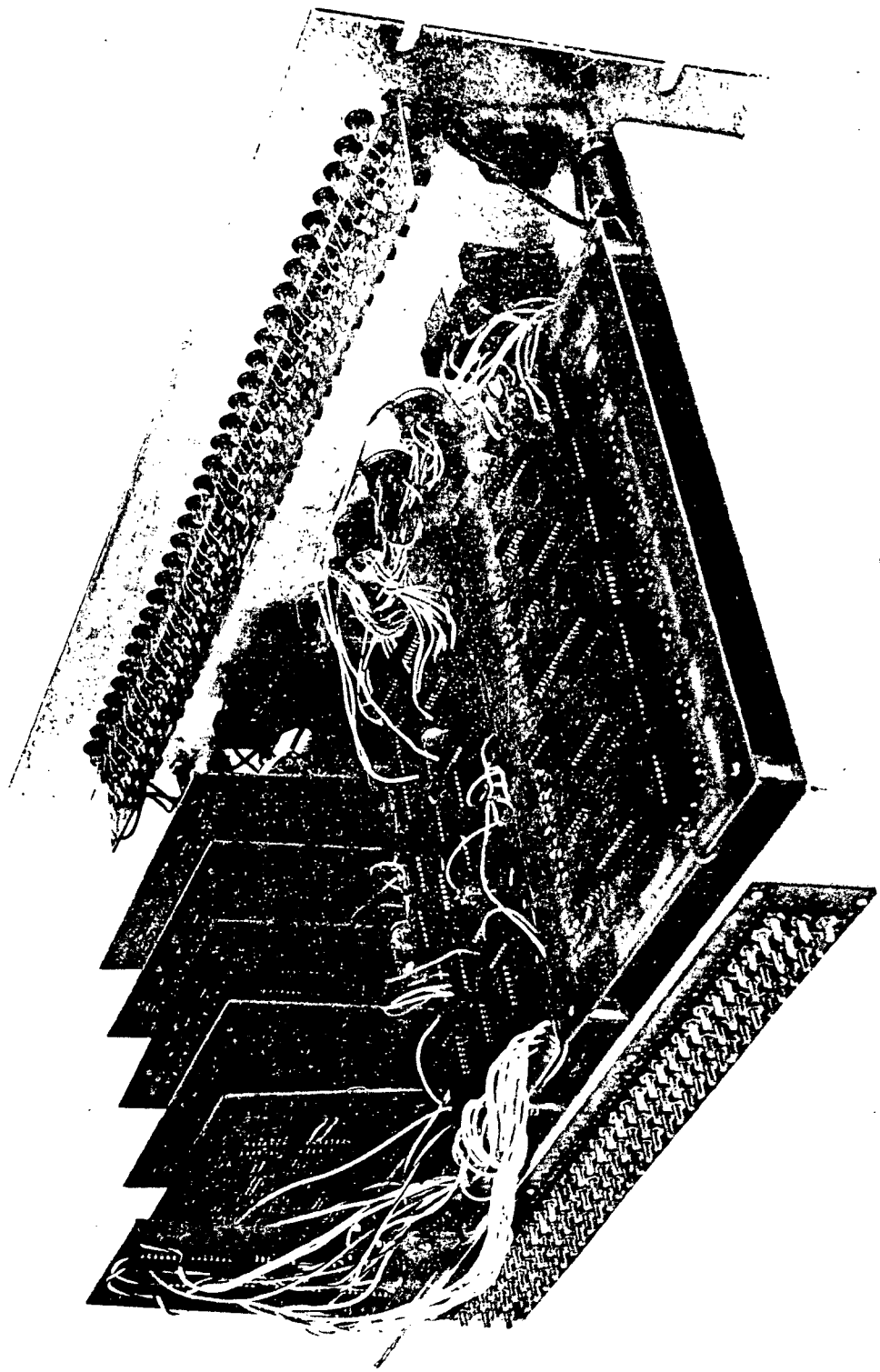

Fig. 36. Data Decoder Rear View