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UNIVAC DEFENSE SYSTEMS DIVISION

CONCEPTUAL DESIGN AND FEASIBILITY EVALUATION MODEL
OF A 10^8 BIT OLIGATOMIC MASS MEMORY

FINAL SUMMARY REPORT
VOLUME 1. CONCEPTUAL DESIGN

NASA CONTRACT NAS8-26670

DI-2749-A (REV. 5/71)

FEBRUARY 1972

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CONCEPTUAL DESIGN AND FEASIBILITY EVALUATION MODEL OF A 10^8 BIT
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FINAL SUMMARY REPORT
VOLUME 1. CONCEPTUAL DESIGN

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February 1972

PREPARED FOR

George C. Marshall Space Flight Center
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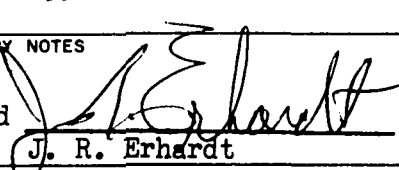| 1. DOCUMENT NO. PX 6676	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.	
4. TITLE AND SUBTITLE Conceptual Design and Feasibility Evaluation Model of a 10^8 Bit Oligatomic Mass Memory Volume 1. Conceptual Design		5. REPORT DATE February 1972	
		6. PERFORMING ORGANIZATION CODE	
7. AUTHOR (S) A. L. Recksiedler and C. L. Lutes		8. PERFORMING ORGANIZATION REPORT NO.	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Univac Defense Systems Division St. Paul, Minn. 55165		10. WORK UNIT NO.	
		11. CONTRACT OR GRANT NO. NAS8-26670	
		13. TYPE OF REPORT AND PERIOD COVERED	
12. SPONSORING AGENCY NAME AND ADDRESS George C. Marshall Space Flight Center Marshall Space Flight Center Alabama - 35812			
		14. SPONSORING AGENCY CODE	

15. SUPPLEMENTARY NOTES

Approved *[signature]*
J. R. Erhardt

16. ABSTRACT

The Oligatomic (Mirror) Thin Film memory technology is a suitable candidate for general purpose spaceborne applications in the post 1975 time frame. Capacities of around 10^8 bits can be reliably implemented with systems designed around a 335 million bit module. The recommended mode was determined following an investigation of implementation sizes ranging from an 8×10^6 to 100×10^6 bits per module. Cost, power, weight, volume, reliability, maintainability and speed were investigated. The memory includes random access, NDRO, SEC-DED, non-volatility, and dual interface characteristics.

The applications most suitable for the technology are those involving a large capacity with high speed (no latency), non volatility, and random accessing. General purpose flexibility allows organizations to be tailored (power, speed) to particular applications. Advances in LSI on magnetic volumetric efficiency will improve design parameters after 1975.

17. KEY WORDS Oligatomic Mirror Mass Memory Space Applications	18. DISTRIBUTION STATEMENT		
19. SECURITY CLASSIF.(OF THIS REPORT) Unclassified	20. SECURITY CLASSIF. (OF THIS PAGE) Unclassified	21. NO. OF PAGES	22. PRICE

UDI-2536-2 (REV. 5/69)

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1.0 INTRODUCTION

Univac has performed a conceptual design of a 10^8 bit oligatomic thin film mass memory system. A feasibility evaluation model in support of the design was built and delivered. This memory system is intended for on board use in space applications such as the Space Shuttle.

The result of the conceptual design is a preliminary Part CEI (Contract End Item) specification, for a memory module for use in a system with a capacity of 10^8 bits. This specification, PX 5714, is included within an appendix of this report.

To obtain these recommended designs initial investigations of general requirements established a base line design around which several architectures could be investigated. Design details were then investigated in terms of minimum weight, power and volume as well as maximum reliability, maintainability and speed. The applications required a 1975 implementation of the memory technology. Although the time criteria imposed a design freeze of the technology at a rather early state, the design selected is a low risk implementation of an operational memory. The studies performed are explained in this volume.

A feasibility model in support of the current state of development has been built and delivered to NASA. This model is described in Volume II.

The Operator's Manual is Volume III of PX 6676. It contains the cirucit diagrams available in Volume II, and the knob-operating procedures of interest at the model only.

A Program Plan was developed and submitted for the next development phase. PX 6411-8 describes a development which can be immediately undertaken and completed within an 18 month time frame. The deliverable item would be a flexible, fully populated memory module, compatible in fit, form and function to the CEI memory described in PX 5714.

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The above documentation is supported by the calculations performed in the trade studies described in this volume.

The basic parameters of the CEI memory module are:

- modules per 10^8 bit system: 3
- capacity per module:
    useable data bits: 33, 554, 432 (2^{25})
    total bits, including extended
        Hamming code, spares & dummy bits: 46,258,992

- no. of random accessible words: 1, 048, 576, (2^{20})
- addressable word length 32 (2^5) bits
- read characteristics:
    NDRO
    2.5 microsecond cycle time
- non-volatile
- Dual interface:
    Serial to 1.1 MHz data bus
    Parallel to computer I/O channel
        200 KHz maximum transfer rate

- Reliability features
    Power transient protection
    Hamming code over data and address field
    · Parity bit
    Degraded modes of operation

- Capable to withstand multiple launches
- Capable to withstand extra atmosphere radiation fields
- Physical Parameters (per module)
    Weight: 45.3 kg max (100 lbs.)
    Volume: 0.045 cu meters max (1.6 cu. ft.)
    Power: 113 watts, nominal

2.0 SUMMARY

Univac's requirements under the contract were to perform the following:

- Plans
  - Deliver a Project Plan detailing how work is to be accomplished under this contract.

    The Project Plan was delivered, dated 22 April 1971

  - Deliver a Program Plan delineating how a follow-on design, development, fabrication, test and delivery of a full 10^8 bit prototype could be submitted within an eighteen (18) month period.

    The Program Plan, PX 6411-8, included as an Appendix, was delivered in August 1971. It provided a 3 phased effort to deliver an "Engineering Development Model, Oligatomic Mass Memory Module."

- Design
  - Conceptually design a reliable mass storage unit with a capacity of 10^8 bits, for on-board use in a space application such as the Space Shuttle. The design is to include trade studies including; system architectures, error detection/correction, fault isolation, packaging and redundancy. The design is to minimize size, power, and weight and maximize reliability, maintainability and speed.

    The design and supporting trade studies are described in this report.

  - Deliver a Preliminary Part I CEI Specification.

    The Preliminary Part I CEI specification, PX 5714, included as a appendix, was delivered in September 1971.

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· Feasibility Model

- Fabricate, test and deliver to Marshall Space Flight Center,
a feasibilty model of the mass storage system for evaluation
purposes. The model is to be limited in capacity to that necess-
ary to prove feasibility of the approach, and to include special
test equipment required for operation.

The Feasibility Evaluation Model is described in Volume 2.
It was delivered in February 1972, and consists of a Memory
Unit and an Exerciser Unit.

· Reliability

- The memory design shall be capable of satisfactory operation when
exposed to the environment expected for space applications such
as the Space Shuttle. The launch, airborne, and space borne
environments are incorporated in the Preliminary Part I CEI Specs
as described within this volume.

· Technology

- The design shall use the Oligatomic Film (Mirror) Technology

The trade studies utilized the parameters indigenous to the
Oligatomic Thin Film Technology. The delivered Feasibility
Model represents a particular state in the development of the
Oligatomic technology.

· Reports Requirements

- Detailed reports of trade studies, monthly progress reports and
a final summary report are required. All technical reports are to
use the International System of Units.

. Reports Requirements (Cont.)

- Monthly reports were submitted in the report sequence
  PX 6411- n

- Preliminary trade study reports were periodically generated.
  These reports are utilized in this Final report.

. Period of Performance

- The period of performance requires completion by February 9, 1972

Univac's approach to meet these requirements was to establish two projects,
one for the Conceptual Design, and one for the Feasibility Evaluation
Model. These projects are summarized in Volume I and Volume II, respect-
ively, of this report. Volume II is self contained. The following is a
summary of the Conceptual Design.

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Initially, 10^8 bits were assumed to be best packaged in a single physical container. The final recommendation is to assemble the memory system from modules containing 33,554,432 data bits organized as 2^{20} 32-bit words. Total system capacity of 10^8 bits is then implemented with three modules. This packaging allows form factors which are better suited to the environment. The study concluded that cost advantages occur for this size module. Penalties in size and weight were absorbed by the separate packaging. These penalties, while undesirable, were not felt severe in terms of development cost (risk) advantages thus obtained. The existing recommendation includes extensions beyond the current technology state which would be acceptable for a general purpose mass memory without requiring interim breakthroughs.

The user parameters of interest are defined as:

Maximum speed,	Minimum power,
reliability,	weight,
maintainability,	volume.

The proper combination of these parameters will yield a minimum cost/ minimum risk memory. An objective of the trade studies is to provide the guidelines for such a memory design. This objective was a primary goal maintained through the study and in the development of the Part I CEI specification.

All trade parameters except speed were considered in the trade study, and the cost relationships here also developed. Variations affecting speed are equally applicable to all trade study candidata systems and are considered separately. The trade study has accomplished its purpose of selecting the most applicable system from all candidate systems considered while avoiding the expense of generating a complete design for each system. The study method had distinct phases prior to the CEI recommendation.

Ground rules were established for evaluating each trade parameters. Trade parameters for each candidate system were evaluated based upon the same set of ground rules. The results are adequate for relative comparisons between options. Specific values for each option are less meaningful and should be viewed as limited by the study ground rules.

An exact evaluation of the weight, power, and volume trade parameters requires a complete detailed design. Exact cost, reliability and maintainability evaluations require production quantity and schedule requirements, test and qualification specifications, field maintenance plans and application requirements in addition to a detailed design.

Mission parameters could not be optimized from existing data. In particular, a Space Shuttle may be utilized in potentially fifty different missions, each mission contributing separate requirements to the memory structure. Therefore, the memory system is to represent a general purpose design unconstrained by the particular application.

A base line design was established to define the design variables. The design variables were then reviewed for appropriate designs. Twenty-four potential design implementations or options were selected which would yield the most data on the desired design parameters. Calculations were undertaken for each of the design implementations. By comparing results of these calculations, a final recommendation was made. The final recommendation was significantly different than the base line definition and the implementations selected for study. Thus, if any preconceived ideas were initially present, they were overruled through the study effort.

The final recommended design is constrained to be a mass memory system flyable in 1975 with a low risk based on existing technology. As the technology base develops further, the technology will advance further. Additional efforts to identify technology advances have been identified although not completely investigated. Many approaches exist to improve the technology. Continual improvement is foreseen over the next five year period.

3.0 GENERAL REQUIREMENTS

The requirements of a general nature imposed on the memory system are described within this section. They include:

- Capacity
- Modularity
- Word Size and Interface
- Maintainability and Packaging
- Environment
- Redundancy
- Speed

3.1 Capacity

Memory capacity required for the system is undefined until particular applications are determined. However, from the basic study parameters, a guideline requirement of 10^8 bits is given. These bits may be used as:

- Flight Critical Programs
- Non-Flight Critical Programs
- Data Storage

The Flight Critical Programs have been studied by Univac for the booster within the Space Shuttle system (Contract No. NAS8-30186). A 10^8 bit capacity would allow these bits to be redundantly stored with approximately 1/8 to 1/10 of the total memory capacity available. Thus, the main portion of the memory capacity available could be utilized for non-flight critical programs (example: data compaction programs) or data storage, i.e., data buffer applications.

3.1.1 Flight Critical Programs

During the flight of a Space Shuttle system, the data management system (DMS) includes computers which provide a computational center for all avionics subsystems. Each of the DMS computers contains its own memory. The computer memory and mass memory design result from different design

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requirements. The computer memories must operate with high speed processors while simultaneously receiving sensor data and transmitting control data. A primary factor in the computer memory design is the speed. Cost is a lower priority design factor.

The role played by the mass memory in performing the flight mission tasks results from the primary requirements except the mass memory stresses cost above speed. The per bit cost of the computer memories will be greater than the per bit cost of the mass memory. By relying upon the mass memory for storage whenever possible, the required computer memory size is reduced. Thus, an overall cost savings is generated. A significant reduction in computer memory size is realized by sizing the computer memory to hold only those programs that are required simultaneously instead of sizing it to hold all the programs used during the mission. From Univac's sizing study, the required memory capacity for the booster during major mission phases is:

- Boost   - 1,400,000 bits
- Coast   - 1,350,000 bits
- Re-entry - 1,330,000 bits
- Cruise   - 1,020,000 bits
- Landing -   860,000 bits

Some of the programs are used during more than one flight phase making the total capacity requirements less than the sum of the requirements given above. The estimated total flight program capacity requirements are 3,120,000 bits. A reduction of greater than 50% in computer memory size is available by storing mission flight programs in the mass memory until they are required.

The flight programs are critical not only to mission success but also to crew safety. A FOFOFS (Fail Operate Full Operate Fail Safe) requirement dictates quadruple redundancy or its equivalent where crew safety functions are involved. The mass memory allows a redundancy capability

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for the portion of the memory used to store critical flight programs. Use of the mass memory results in no additional memory requirements because the computer and also associated memories require the same redundancy for flight critical requirements.

3.1.2 Flight Non-Critical Programs

Other programs used during the flight are not critical for flight safety. These programs need not be multiply redundant. They are programmed to be executed during flight. Guarantees must be made that programs are correct when read into the computer memory. This guarantee can be implemented through operating techniques such as a checksum scheme. The test for program correctness is then made by the computer rather than the mass memory. This test technique verifies the data transmission across the computer/mass memory interface as well as proper operation of the mass memory. The programs which control in orbit experiments can fall into either a _mission_ critical or mission non critical category. If the total mission is devoted to conducting a single experiment and the success of the experiment is dependent upon program control, then the program is mission critical. If the experiment can be conducted without using the computers or the buffer store with no detriment to the experiment or mission, the experiment has then gone along for the ride and has a status of not being mission critical. A gray area in between exists as to definition of mission criticality.

All programs carried in the mass memory require protection from on board modification through the WRITE memory instruction. When data is being written into the mass memory, an incorrectly interpreted address will cause the data to enter the wrong location. Incorrect addressing could cause a program required later in the flight to be permanently destroyed. The requirements for correctness in the on board write address is thus greater than the requirements for correctness in data being written into the memory.

3.1.3 Data Buffer

The main portion of the memory is available for recording data during the mission. The recorded data includes both experimental and flight record data. The requirements on data recorded in mass memory differs from the requirements on data read during flight. If a sensor output is being periodically recorded, a trend analysis of the data can be used to eliminate most of the incorrect data of value. Further, the computer may be utilized to compact data periodically prior to transmission to the earth for further analysis. On line correction of experimental data is possible when the mass memory acting as a buffer is incorporated into a computer controlled hierarchy.

Each bit of flight record data may carry unique significance. Thus, errors in this data are not subject to trend analysis.

The general purpose nature of the mass memory is best served with random accessing to each word. Particular experiments or recording modes may allow reductions in accessing circuitry. Reductions in weight, power and size would then be accompanied by increased reliability. However, there is no criteria to determine optimum blocks or sequential accessing schemes. Complete random accessing allows the greatest application flexibility.

3.2 Modularity

The flight program contribution to memory requirements has been estimated at 3.1×10^6 bits per copy for the booster. These programs are both mission and flight safety critical, and a quadruple redundancy requirement may apply. If four copies of the flight program are stored, 12.4×10^6 bits of storage would be required within 4 modules for the booster.

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The orbiter flight program should be larger than the booster flight
program because of additional flight modes and different requirements
from similar flight modes. The size of a flight program would indicate
that a modularity of at least 2^{22} bits or approximately 4×10^6 bits
be considered minimum.

At least fifty missions are to be performed by this system, each mission
having its own peculiar memory requirements. Optimizing the memory
module size thus is a partial effort and cannot be fully carried out for
any particular mission. A memory capacity of 10^8 bits is an order of mag-
nitude above the memory capacity required for storage of flight programs.
Modularity can be considered within these two limits of capacity.

3.3 Word Size and Interface

The mass memory interfaces would both be to DMS computers and on-board
experimental equipment. These can be considered separately. The infer-
face between the computers and a mass memory is assumed to be time multiplexed
data bus. The data bus interface is not precisely defined. However, some
general requirements can be specified. The data bus will either request
or deliver data records having a record length compatible with the computer
word length. Although DMS computers have not yet been specified, many
current off the shelf avionics computers considered to be potential candi-
dates have a 32 bit word length. Therefore, for the purpose of this study,
it is assumed that the DMS computer will have a 32 bit word length. Each
record transferred between the mass memory and the DMS computer will have
an integral multiple of 32 data bits. In addition to the data, data valida-
tion codes may be transmitted to insure correct data transfers. Implementa-
tion of validation codes is a technique of implementing a FOFOFS require-
ment, without invoking total redundancy.

Interfaces between the mass memory and the experiments are completely
undefined. This interface can be defined only after detailed experiment

definitions are available. The primary communication between the experiments and a mass memory will be for the storage of sensor data. Some experiments may request data from the main memory. A generalization on sensor derived data (which may not hold true for any specified application) is that the data length will be short, generally 8 to 10 bits in length. Thus, some packing of sensor data can be assumed. To keep a compatible format with the 32-bit defined format of the computer, packing to a 32 bit word length can be assumed. If sensor data rates are slow, the data formatting and packing functions can be done by the computer. With high data rates, this function must be performed by additional special purpose hardware designed for the experiment set which interfaces the general purpose equipment, i.e., the computer and the memory. For high data rates, the mass memory should have a parallel input/output channel. This channel should be designed to handle the maximum data rate as well as conforming to the 32-bit computer word.

3.4 Maintainability and Packaging

The Space Shuttle application requires that ground support and turn around time be minimized. To achieve this requirements, the mass memory must have self test and fault isolation capabilities. Fault isolation must indicate failures to an LRU, i.e., lowest replaceable unit level. Packaging should allow easy removal and replacement of LRUs. Packaging should also meet standard mounting and volume specifications, e.g., limited to a 1 or 1½ ATR case size. These standardized dimensions should also allow for lower cost implementation.

3.5 Environmental Specifications

Environmental specifications must reflect the use of the mass memory in a man rated type vehicle. The memory should meet the applicable environmental specifications of MIL-E-5400 K for Class III equipment. Applicable environmental specifications are found in paragraphs:

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3.2.2.4.1 Temperature

3.2.2.4.1.1 Operating

3.2.2.4.2.1 Non Operating

3.2.2.4.2 Altitude

3.2.2.4.3 Temperature Altitude Combination

3.2.2.4.4 Humidity

3.2.2.4.5 Vibration

3.2.2.4.6 Shock

3.2.2.4.10 Explosive Conditions

3.2.11   Electromagentic Interference Characteristics

Typical launch and extra atmosphere mission environments have been
included in the appendix within document PX 5714.

3.6 Redundancy

The mass memory should be capable of accepting and storing data after
failure of its two most critical parts and of delivering data after the
failure of three of its most critical parts. This is the FOFOFS
redundancy requirement. This requirement may exist for the mission or
flight critical programs/data only. Mission critical data may or may not
have the strict redundancy requirement. There is no redundancy requirement
on the storage of non-critical data. However, a failure during the storage
of non critical data which could affect the integrity of critical data
must be considered as failure of a critical part. Although the high
reliability may require extreme component implementation and cost, it also
represents the extreme condition of redundancy which the memory may have
to meet. Thus, in meeting the FOFOFS requirements the memory may be const-
ructed so that lesser redundancy requirements are also met. In order to
achieve high memory usage efficiency, the memory must be capable of operating
both in multiple-redundant and in non redundant modes.

3.7 Speed

It is assumed that the serial data bus will consist of two transmission
lines, one line containing clock and start of message pulses. The other
line will carry address, command and data. The clock frequency is assumed
to be 1 mHz. The mass memory, in receiving a command on the data bus,
will respond by either transmitting data, receiving data or receiving an
address. All transmissions on the data bus will be synchronized with the
1 mHz clock. Data transmitted or received will be in short 32-bit compa-
tible records. Thus, the memory shall be capable of transmitting or
receiving data over this bus at a speed of 1 usec/bit with asynchronous
delays between record transmissions. The initial assumption of 32 usec
between requests is made. Thus, adequate time is available to perform
all logic tests conceivalbe as well as echo type tests for correctness of
data transmission.

A word parallel channel, capable of delivering words at a 200 KHz rate is
sufficient for applications involving a computer I/O channel.

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4.0 INITIAL BASELINE SYSTEM

Based upon the general systems requirements a preliminary set of archi-
tectural options can be generated. Figure 4.1 shows three options.
These architectures are used to determine a baseline design for this
study.

The first option is constructed of 6 identical modules with each module
containing 16.8 million bits of data storage for a total capacity of 100.7
million bits. The main advantage of this option lies in its modularity.
Memory addresses will be transmitted as binary words. With an address
length of N bits 2^N words can be addressed. With 32 bit words and N large
enough to individually address all words in the 100.7 million bit memory
there exists sufficient excess addressing capability to address the words
in two additional 16.8 million bits modules. Thus this design is expandable
or contractable in 16.8 million bit increments to more efficiently meet a
variable capacity requirement. Interconnections between four of the modules
are shown to indicate possible data flow paths used for checking and correct-
ing redundant data outputs and inputs.

The second option uses four 25.2 million data bit modules to achieve a 100.7
million bit total. This option should show an overall weight and power
savings over the first option for the 100.7 million bit total. Each memory
module requires a power supply, timing and control logic, address decode
logic, etc. Many of these functions require identical mechanizations in-
dependent of module size resulting is a savings when fewer but larger modules
are used. Four modules is the minimum number capable of meeting quadruple
modular redundancy.

Option # 3

Data bits/unit 50.3M
Total data bits 100.7M
Internal Redundancy

Option # 2

Data bits/unit 25.2M
Total data bits 100.7M

Figure 4.1 Architectural Options
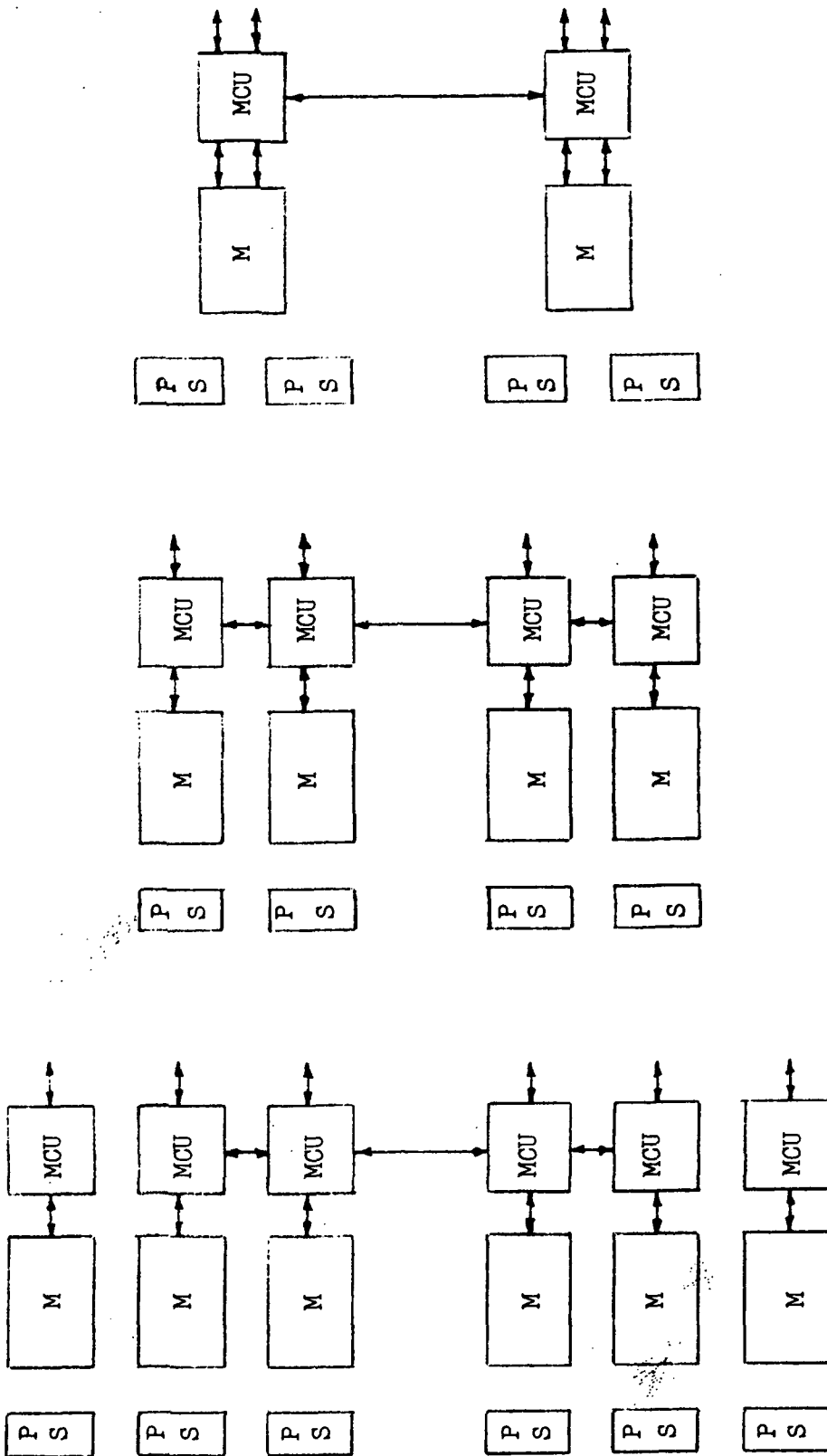
Option # 1

Data bits/unit 16.8M
Total data bits 100.7M

Option # 1A (4 modules)

Total data bits 67.1M

The third option takes advantage of some inherent redundancies within each memory module. For example if a failure in a word line or in circuitry associated with a single word line occurs only a small portion of memory is disabled. By incorporating redundancy within a module, duplicating only those functions which if failed would cause a total module failure should result in a total hardware reduction, with a resultant weight and power savings. Error correction and detection codes provide one means of incorporating fault tolerance with this design option. The first option is selected for the baseline design. This selection allows a greater flexibility while investigating a general purpose design.

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4.2 Baseline Definitions

To develop cost, weight, power, maintainability and reliability trade parameters , the implementation variables must be delineated and bounded. The heart of the oligatomic memory consists of magnetic planar films overlaid with word and digit lines which is termed a stack. Operation of the memory requires the electrical selection of specific word and digit line intersections. Trades can be made in the physical design of the stack and in the word and digit line selection logic. The memory design must meet certain application requirements which specify its speed, interface and fault tolerance. Design variations exist for meeting the application requirements. These discussions develop in detail the design variables.

The baseline system will consist of six identical modules with each module containing 16,777,216 (2^{24}) data bits. The data bits are divided into 524,288 (2^{19}) 32 bit words. Each word will contain four parity bits in addition to data, and no further error correction and detection techniques.

Stack

Unfolded Central Stack - 86.4CM(34 inches) long, 8.13CM
(32 inches wide)

Unfolded Stack plus Selection Gate Boards - 132.1CM(52 inches)
long,111.8CM(44 inches) wide

Folded Stack plus Selection Gate Boards - 43.2CM(17 inches)
long, 40.6CM(16 inches) wide 8.1CM
(93.2 inches) high, 16 layers thick
at .051CM (.02 inches per layer)

Housed Folded Stack 44.5CM(17.5 inches) long 43.2CM(17 inches)
wide 8.9CM(3.5 inches) high

Volume - 17,059 cubic CM(1041 cubic inches)

5.0 DETAILED DESIGN REQUIREMENTS

5.1 Stack Physical Parameters

The oligatomic memory consists of a magnetic thin film (100Å) overlaid with two sets of orthogonal conductors. A storage bit results at each conductor intersection. The basic memory element is called a substrate and has a large number of line intersections (over 100,000 is typical). Several of these substrates are mounted and interconnected on a circuit board termed a centerboard (see figure 5.1). Substrates are mounted on both sides of the centerboard. The total memory (excluding electronics) is composed of interconnected centerboards termed a stack. The total memory when opened can be visualized as a planar array with:

n_s = number of digit lines per substrate

n_c = number of substrates along the length of the digit side of a centerboard

m_s = number of word lines per substrate

m = number of substrates along the width of the word side

n_b = number of centerboards in digit direction

m_b = number of centerboards in word direction

Tht total number of digit lines (assuming two sides of centerboard used) is:

$$N_t = 2\ n_s \cdot n_c \cdot n_b \qquad (1)$$

Tht total number of word lines is:

$$M_t = \cdot m_s \cdot m_c \cdot m_b \qquad (2)$$
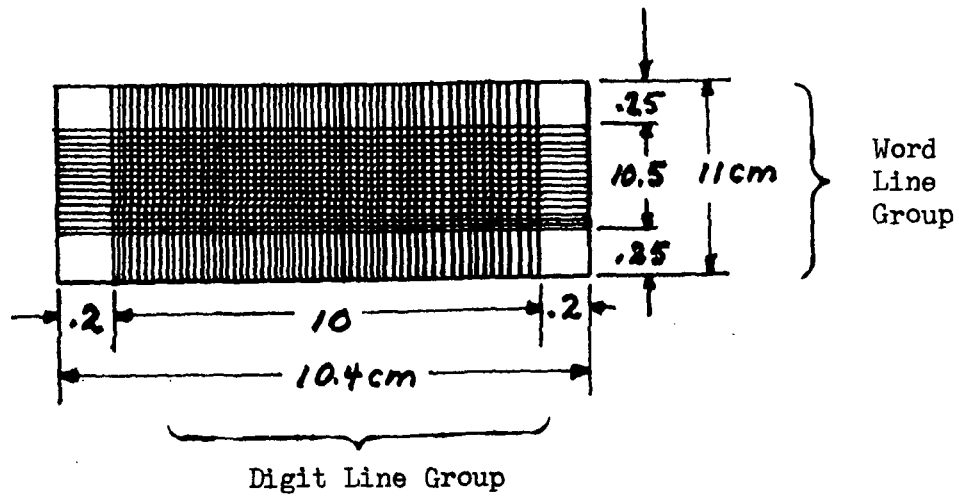
a. Substrate
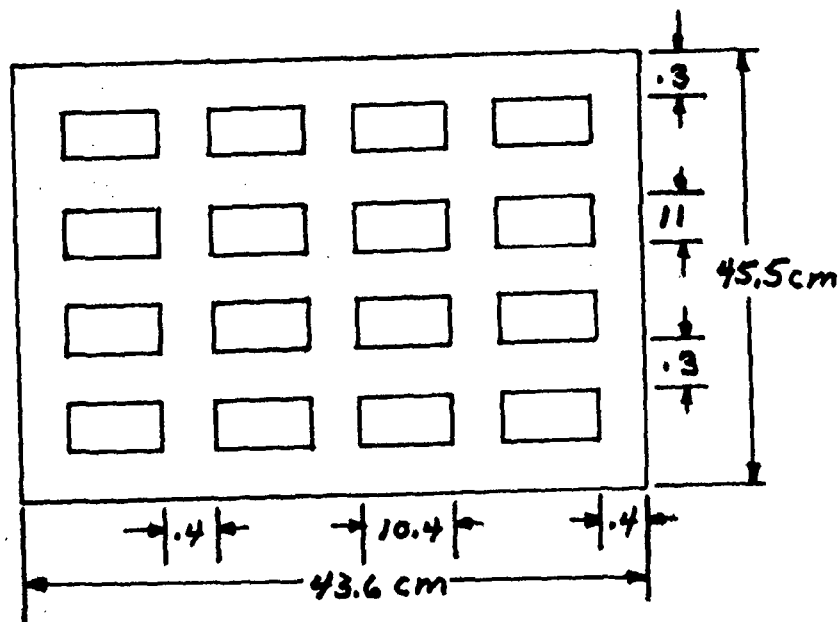
b. Center Board

Figure 5.1   Typical Array Layout (typical dimensions)

The total number of bits is:

$$B_t = N_t \cdot M_t = 2 \cdot n_s \cdot m_s \cdot n_c \cdot m_c \cdot n_b \cdot m_b \qquad (3)$$

The total number of bits in the memory are not used for data storage.
There are three potential bit uses in addition to data storage. These
are for spares, reference digit lines, and error correction and detection
codes. In order to reduce the manufacturing cost of the memories by in-
creasing yield, spare word and digit lines are provided for each sub-
strate. For every n_d digit lines used there is one reference digit line
which is invisible to the user. The n_d + 1 digit lines is termed a digit
line group. All of the bits along the reference digit line are zero set.
On reading any digit line, its output is compared with the reference digit
line to interpret between a "one" or "zero". Error detection and
correction (EDC) bits are stored along with each data word in memory.
These are data bits requiring reference bits, but are not data bits avail-
able for the application.

Defining the parameters:

n_d = number of digit lines per reference line

n_e = number of spare digit lines per substrate

m_e = number of spare word lines per substrate

n_p = number of EDC bits with each word

n_w = total number of bits in each word including EDC bits

n_m = number of data bits in each word $(n_w - n_p)$

The total number of data bits in the memory is:

$$B_d = \frac{2 \cdot (n_s - n_e) \cdot (m_s - m_e) \cdot n_c \cdot m_c \cdot n_b \cdot m_b \cdot n_d \cdot n_m}{(n_d + 1) \cdot n_w} \qquad (4)$$

The number of word lines used is

$$M_d = (m_s - m_e) \cdot m_c \cdot m_b \qquad (5)$$

The number of digit lines used for data is:

$$N_d = \frac{2 \cdot (n_s - n_e) \cdot n_c \cdot n_b \cdot n_d \cdot n_m}{(n_d + 1) \cdot n_m} \qquad (6)$$

It should be noted that N_d must be an integer requiring that the numerator of equation 6 be evenly divisible by the denominator.

An overall data storage bit efficiency factor is given by

$$E_d = \frac{B_d}{B_+} = \frac{(n_s - n_e)}{n_s} \quad \frac{(m_s - m_e)}{m_s} \quad \frac{n_d}{n_{d+1}} \quad \frac{n_m}{n_w} \qquad (7)$$

The four terms in equation 7 are the spare digit line factor, spare word line factor, reference digit line factor and EDC factor respectively.

The study baseline memory design has parameter values of

$$n_s = 324$$
$$n_e = 0$$

$$m_s = 576$$
$$m_e = 64$$
$$n_d = 8$$
$$n_m = 32$$
$$n_w = 36$$
$$n_c = 4$$
$$m_c = 4$$
$$n_b = 2$$
$$m_b = 2$$

This produces the following memory capacity parameters:

$$N_t = 5184$$
$$M_t = 4608$$
$$B_t = 23,887,872$$
$$N_d = 4096$$
$$M_d = 4096$$
$$B_d = 16,777,216$$
$$E_d = .702$$

spare digit efficiency factor = 1.0

spare word efficiency factor = .889

reference digit efficiency factor = .889

EDC efficiency factor   = .889

The dimensions, volume, and weight of the memory stack are important parameters to be considered in the final design. The dimensions of each substrate are defined to be

l_s = length of substrate (digit direction)

W_s = width of substrate (word direction)

Spacings occur between each substrate when mounted on the centerboard and between the substrate and the centerboard edge. Defining these parameters:

Δl_s = length spacing between substrates

ΔW_s = width spacing between substrates

The spacing between substrates and the spacing between the centerboard edge and the substrates may be assumed to be identical. The centerboard length and width is then given:

$$l_c = (l_s + \Delta l_s)n_c + \Delta l_s \qquad (8)$$

$$W_c = (W_s + W_s)m_c + \Delta W_s \qquad (9)$$

The centerboards are stacked on top of each other with a spacing between the boards defined:

h_c = distance between centerboard centers.

The stack volume is then given by

$$V_s = l_c \times W_c \times h_c \times n_b \times m_b \qquad (10)$$

Several bit densities can be computed from the dimension and capacity parameters. Those of interest are:

Raw area density

$$R_a = \frac{B_+}{2\,l_c \cdot W_c \cdot n_b \cdot m_b} \qquad (11)$$

Raw volume density

$$R_v = \frac{B_t}{V_s} \qquad (12)$$

Area density of data bits

$$D_a = \frac{B_d}{2\,l_c \cdot W_c \cdot n_b \cdot m_b} \qquad (13)$$

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Volume density of data bits:

$$D_v = \frac{B_d}{V_s}$$

By knowing the stack density, p_s, the weight of the stack can be determined from

$$\text{Weight} = V_s p_s$$

A typical density factor is .05 pounds per cubic inch.

Characteristics of the baseline internal stack organization are:

Digit Lines

Useable Data Lines = 64 groups of 64 lines/group = 4096 lines

Data plus Parity/Spare Lines = 72 groups of 64 lines/group = 4608 lines

Total Digit Lines = 72 groups of 72 lines/group = 5184 lines

(include 1 dummy reference line for every 8 active lines)

Word Lines

Useable Word Lines = 64 groups of 64 lines/group = 4096 lines

Total Word Lines = 64 groups of 72 lines/group = 4608 lines

(includes 1 spare line for every 8 active lines to facilitate repair and manufacturing)

The physical characteristics of the stack are: (see figure 5.2)

Word Lines

2 groups of 288 lines each per substrate

Centerboard width – 4 substrates wide

Central stack width – 2 centerboards

SPERRY RAND

Electronics

Arrays

Power Supply
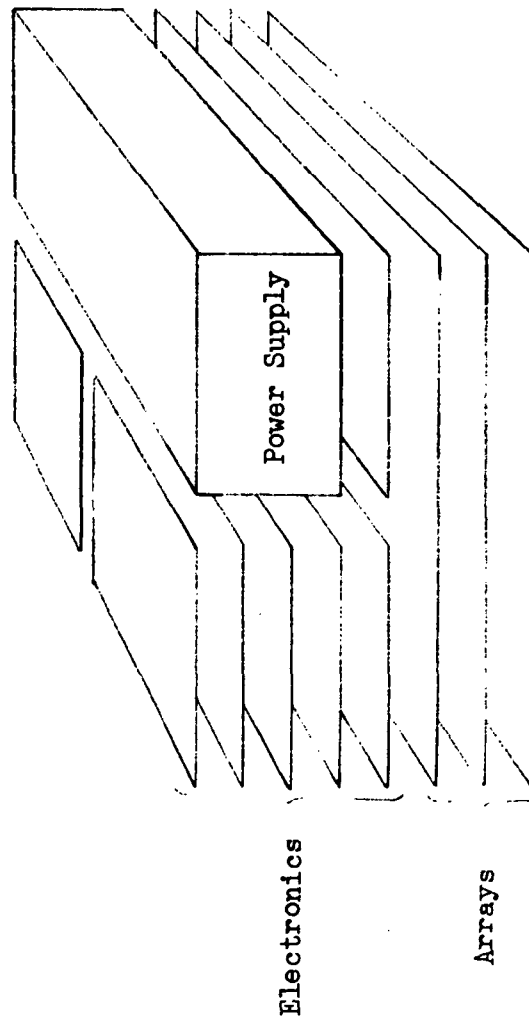
Figure 5.2   Physical Module Layout (folded)

Digit Lines

    Centerboard length - 4 substrates wide

    Central stack length - 2 centerboards (both sides)

Substrates

    Centerboard - 16 substrates one side, 32 substrates both sides.

    Stack - 4 centerboards, 128 substrates total

    Data Bits - 2^{17} bits per substrate, 2^{24} bits per stack.

Word Gate Boards

    Double sided

    Upper side - 64 hybrid word gate packages, (1 spare row of 8)

    Lower side - 64 hybrid word termination packages (1 spare row of 8)

    Stack - 4 double sided gate boards.

Digit Gate Boards

    Double sided

    Upper side - 36 hybrid digit gate packages (1 spare row)

    Lower side - 36 hybrid digit gate packages

    Stack - 8 double sided gate boards.

Hybrid Packages

    Width - 3.0 (1.2 inches) (across leads), length 3.8 (1.5 inches)

    Leads - 40 leads total, 20 leads each end.

5.2 Selection Logic

5.2.1 Memory Operation

A more detailed description of the Theory of Operation of an Oligatomic memory is under that title within Volume II of this report. A brief description of the affects of the circuitry requirements for the read and write operations is sufficient here.   The memory read operation is achieved by driving a word line with a high frequency current (10 MHz typical). This causes all digit lines intersecting with the driven word line to become excited. The frequency of the digit line signal is twice the word drive current frequency. The phase of the digit line signal is dependent upon the magnetization direction of the magnetic film immediately under the word-line/digit-line intersection. Thus the state of the memory bit is determined by the phase of the signal appearing on the digit line. A reference phase signal is generated through the use of a reference digit line. The magnetic domains at all intersections along the reference digit line are "zero" set.   The use of a reference digit line to obtain a phase reference has the additional advantage of providing noise rejection. Several reference digit lines are used throughout the memory and placed in close proximity to their associate digit data lines. Noise pickup on the reference digit lines and digit data lines will be approximately the same and be automatically eliminated in the phase comparison process.

The high frequency word line current is also required in the memory write function. To write a bit at the intersection of a word and digit line requires the high frequency word line current plus a pulse current on the digit line. The direction of current flow on the digit line determines whether a "one" or "zero" is being written.

Figure 5.3 is the memory block diagram showing the major functional blocks. The main interface with the memory is a common data register providing temporary semiconductor storage of the read data or the data to be written an address register containing the memory address, and a read or write command.
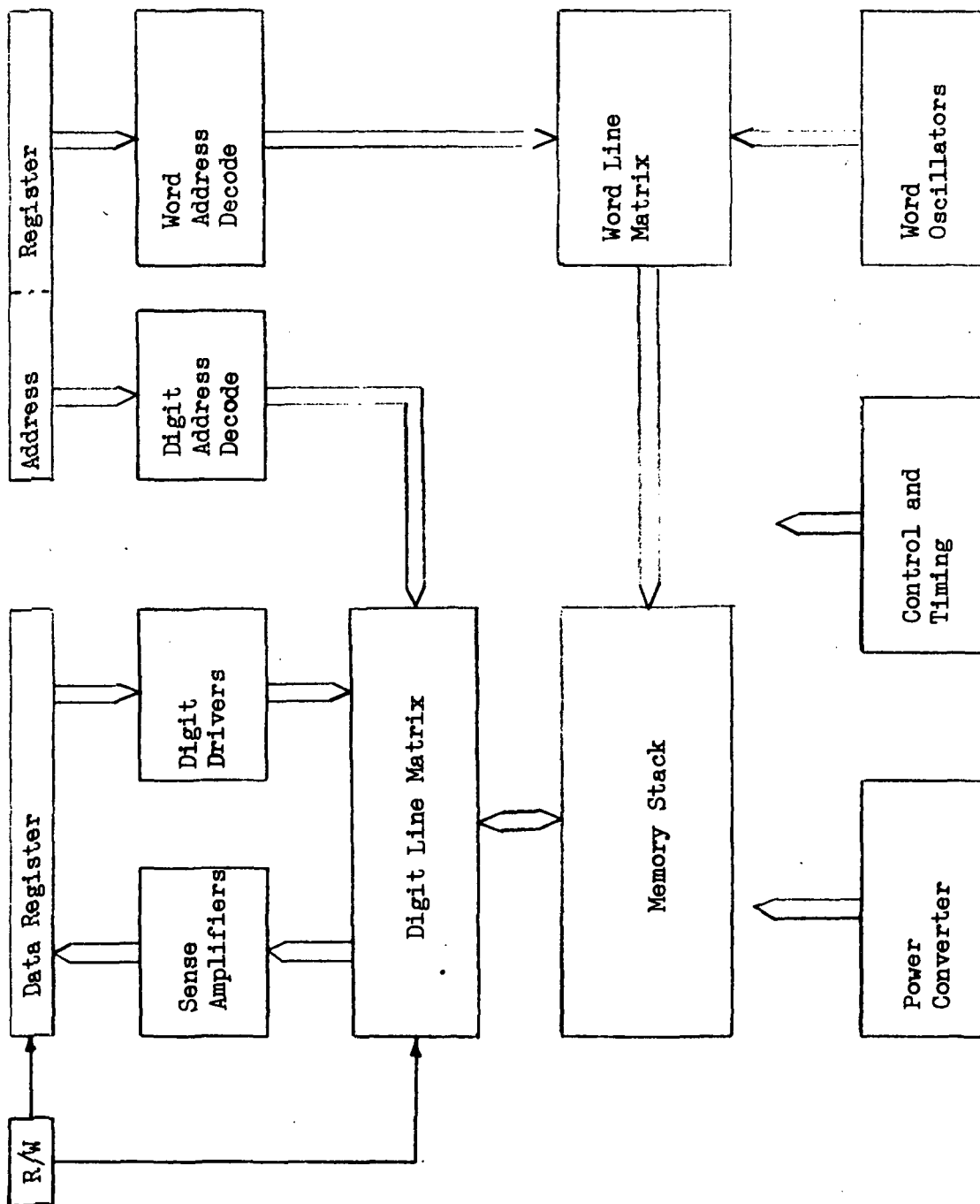
Figure 5.3 Memory Block Diagram
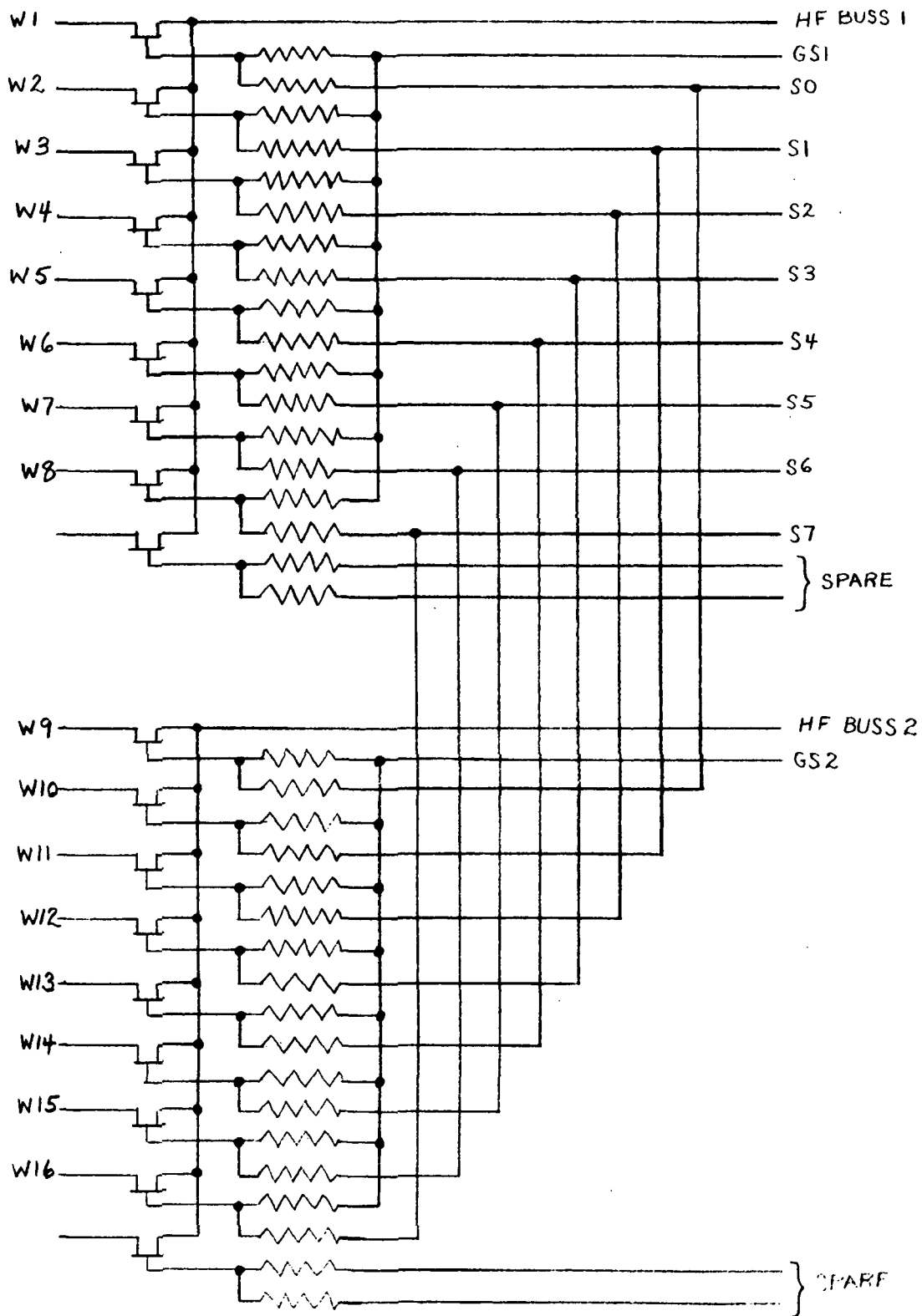
Figure 5.4   Word Matrix Circuitry

The address register is divided into two parts, a portion of the address
is used to select the desired word line and a portion to select the
desired set of digit lines. The word line matrix and word address
decode logic is used to select the desired word line. The word line matrix
gates the word oscillator outputs to the appropriate word line. The word
address decode generates the logic states required by the word line
matrix from the binary states of the address register. The digit line
matrix must be capable of gating both low level sensed outputs and digit
line write currents. The digit address decode logic provides the proper
logic states for the digit line matrix. The memory must also contain
control and timing logic and a power supply.

The heart of the read and write selection process is in the word line
matrix and digit line matrix. Development of circuitry for the word
line and digit line matrices is a continuing process. Present development
consists of a discrete component mechanization housed in a hybrid integrated
circuit package. Each hybrid package has 40 pins, 20 on each of opposte
ends. The package size is 1.2 inches (across the leads) by 1.5 inches by
.062 inches high.

5.2.2 Word Line Selection

Figure 5.4 is the schematic of the word line selection circuitry housed in a
single hybrid package. Each hybrid package provides 16 word line outputs
plus two spare word line outputs. The spare outputs are attached to spare
word lines in the stack. The spares are used during memory manufacturing
to eliminate malfunctioning word lines. Memory cost is reduced by the
increased yield obtainable through the use of spares. In the following
functional description reference to the spare circuitry is omitted. Each
word line is connected to a FET (Field Effect Transistor). The connected

word lines are divided into two groups of eight indicated as W1 through

W8 and W9 through W16.   To cause word current to flow in a

single word line three signals must be applied. First selection of one of

the groups must be made by applying the proper logic level signal to either

GS1 or GS2. Second one of the 8 word lines must be selected within the

group by applying the proper logic level signal to one line SO through

S7. Third the high frequency input must be provided to the selected group

on either HF BUSS1 or HF BUSS2.

There are numerous mechanizations available for achieving word line selection

using the word matrix hybrid circuit packages. In order to show some of

the word line selection mechanizations tradeoffs an example memory having

4096 word lines will be used. Since each hybrid circuit package is capable

of supplying 16 word lines a total of 4096/16 = 256 hybrid circuit packages

are required to supply the 4096 word lines. If a single high frequency source

is available to drive all bus lines then the word address decode logic must

provide logic signals to gate the high frequency source to a single word

line. Two parameters are of major importance in determining the logic

signals required to drive the hybrid circuits. The number of logic lines

between the word address decode logic and the word line matrix should be

maintained at a minimum and the loading upon each line should be kept at

a minimum. The loading produced by a single connection to an SO through S7

hybrid circuit input is that caused by 2 FET input resistors. The loading

produced by a single connection to a GS1 or GS2 hybrid circuit input

is that caused by 8 FET input resistors. When discussing the loading on

logic lines loading will be expressed in the number of FET input resistors
which must be driven.

Each hybrid circuit drives one of sixteen word lines. Sixteen lines can
be addressed using four binary digits, i.e., $2^4 = 16$. Representing the four
binary digits as A_1, A_2, A_3, A_4 the decoding logic for a single hybrid
circuit must generate eight states (or lines) from three of the address bits
and two states (or lines) from the remaining address bits. Other decoding
schemes can be used but in general require additional logic. The four
binary address digits capable of representing one of sixteen states are
said to be decoded into a two dimensional set having 8 x 2 states. The
decoding logic and hybrid circuit inputs for a four bit address code are

$$S0 = \bar{A}_1 \cdot \bar{A}_2 \cdot \bar{A}_3$$
$$S1 = A_1 \cdot \bar{A}_2 \cdot \bar{A}_3$$
$$S2 = \bar{A}_1 \cdot A_2 \cdot \bar{A}_3$$
$$S3 = A_1 \cdot A_2 \cdot \bar{A}_3$$
$$S4 = \bar{A}_1 \cdot \bar{A}_2 \cdot A_3$$
$$S5 = A_1 \cdot \bar{A}_2 \cdot A_3$$
$$S6 = \bar{A}_1 \cdot A_2 \cdot A_3$$
$$S7 = A_1 \cdot A_2 \cdot A_3$$
$$GS1 = \bar{A}_4$$
$$GS2 = A_4$$

with 4096 word lines there are 256 hybrid circuits required. The address
word length is 12 bits, i.e., $2^{12} = 4096$. These 12 bits must be decoded into
a two dimensional set with that set connected to the S0 through S7 hybrid
circuit lines having at least 8 states. Figure 5.5 shows the possible decoding

divisions between the two dimensions and the resulting number of lines

and loading for each decoding scheme. The figure shows that the 64 x 64

case requires the minimum number of lines and has minimum loading on the

maximum loaded line. Besides offering number of lines and loading

advantages the 64 x 64 case offers some hardware similarity advantages.

dimensions	SO-S7 loading	GS1&GS2 loading	number of lines
8 x 512	512	8	520
16 x 256	256	16	272
32 x 128	128	32	160
64 x 64	64	64	128
128 x 32	32	128	160
256 x 16	16	256	272
512 x 8	8	512	520
1024 x 4	4	1024	1028
2048 x 2	2	2048	2050

Figure 5.5 Decoding Alternatives for 4096 word lines

The 12 address bits are divided into two groups of 6 bits and each group

is decoded identically into 64 outputs. Thus requiring two identical

decoding networks. Designating the 64 outputs of each decoding network

as L_1 through L_{64} and M_1 through M_{64} and dividing the 256 hybrid circuits

into 8 groups of 32 hybrid circuits per group the connections to the hybrid

circuit inputs are made in the following manner. L_1 through L_8 are connected

to all SO through S7 inputs respectively in the first hybrid circuit group;

L_9 through L_{16} connected to all S0 through S7 in the second group, etc. M_1 through M_{64} are connected to a single GS1 hybrid circuit input in each group.

The optimum decoding logic for any number of word lines occurs when the dimension values are nearly square. Figure 5.6 shows optimum dimension values for various word line values.

Number of Word Lines	dimension	S0-S7 loading	GS1&GS2 loading	Number of Lines
16	8 x 2	2	8	10
32	8 x 4	4	8	12
64	8 x 8	8	8	16
128	16 x 8	8	16	24
256	16 x 16	16	16	32
512	32 x 16	16	32	48
1024	32 x 32	32	32	64
2048	64 x 32	32	64	96
4096	64 x 64	64	64	128
8192	128 x 64	64	128	192
16384	128 x 128	128	128	256
32768	256 x 128	128	256	384

Figure 5.6   Optimum Loading and Line Numbers for Various Memory Sizes

Memories having the number of word lines different than 2^N where N is an integer are partially populated cases of the next larger 2^N value and requires the same loading and number of lines as the next larger 2^N value.

Each hybrid circuit has two high frequency bus inputs. A second level of switching is achieved by switching power on and off of the high frequency buses. Switching of the high frequency supply to the high frequency buses can be accomplished using the same hybrid circuit word matrix circuitry. There are many options available for implementing two level circuitry. The first level requires a hybrid circuit for every 16 word lines. The second level produces an integer multiple of 16 high frequency bus sources. The word line portion of the address register must be divided into two groups with one group supplying the first level circuitry and the other group supplying the second level circuitry. The minimum number of address bits supplying each circuitry level is 4, i.e., three bits are required for forming the 8 S0 through S7 input states and 1 bit for forming the GS1 and GS2 input states. Thus the minimum number of address bits applicable for two level circuitry word line selection circuitry is 8 bits. The 8 bit address decodes into $2^8 = 256$ word lines.

For a fixed number of word lines(and thus a fixed address length) several mechanization options of two level circuitry exists. To explain these options the example of a memory having 4096 word lines will be used. The number of address bits required for 4096 word lines is 12. These 12 address bits can be split between the two circuit levels with four bits the minimum number allowable for either level in the following ways.

First Level	Second Level
8	4
7	5
6	6
5	7
4	8

The decoding of the address bits can be considered separately for each
level. Taking the case of 8 address bits for the first level, these 8
bits must be divided into two groups, one for the S0 through S7 decoding
and one for GS1 and GS2 decoding. A minimum of 3 bits are required for the
S0 through S7 decoding and 1 bit for the GS1 and GS2 decoding. The decoded
states form the dimensions as described above in the single level word
selection logic. The conclusions drawn from the single level selection logic
analysis i.e., that both minimum loading and the minimum number of logic
lines occurs when the dimensions are square or nearly square, is also true
for each level of the two level selection logic. The most economical decoding
for 8 address bits is then 4 bits for the S0 through S7 lines and 4 bits for
the GS1 and GS2 lines yielding a dimension of 16 x 16.
Each word line is driven from the output of an FET and each FET has a single
S0 through S7 control input and a single GS1 or GS2 control input. The
number of loads per logic state is thus the number of word lines divided
by the type of logic state (or dimension). Thus the load on the S0 through
S7 logic states is 4096/16 = 256. The number of logic lines from the word
address decode logic to the word line matrix for the first level circuitry
is the sum of the dimensions or 16 + 16 = 32. Each of the 5 options for
the two level 4096 word line example contributes a single square or near
square dimension option from which the loading and logic line number can be
computed. The five first level options produce the following results:

Option	First Level Address Bits	Dimensions	SO thru S7 loading	GS1&GS2 loading	Number of lines
1	8	16 x 16	256	256	32
2	7	16 x 8	256	512	24
3	6	8 x 8	512	512	16
4	5	8 x 4	512	1024	12
5	4	8 x 2	512	2048	10

These results show that the loading increases as the number of lines decrease.

The second level circuitry must decode the remaining address bits in each option. If there are N address bits remaining for the second level then 2^N high frequency busses will be created and $2^N/16$ hybrid circuit packages used. The second level circuitry loading and required number of logic lines is determined in the same manner used for the first level circuitry. For the five options the second level loading and number of logic lines becomes:

Option	Second Level Address Bits	Dimensions	SO thru S7 loading	GS1&GS2 loading	Number of lines
1	4	8 x 2	2	8	10
2	5	8 x 4	4	8	12
3	6	8 x 8	8	8	16
4	7	16 x 8	8	16	24
5	8	16 x 16	16	16	32

The total number of logic lines required for both levels and the worst case loading for each of the five options is:

Option	Worst case loading	Number of logic lines
1	256	42
2	512	36
3	512	32
4	1024	36
5	2048	42

Of these five options, only options 1, 2 and 3 are candidates for mechanization. Options 4 and 5 have worst loading, a greater number of logic lines, and require more hybrid circuits to mechanize than option 3. Option 3 has the least number of logic lines and option 1 has the best worst case loading. Option 2 has the same worst case loading as option 3 and more logic lines however requires less hybrid circuits to mechanize. Figure 5.7 gives the candidate options for various number of word line cases. Comparing figures 5.6 and 5.7 shows that the two level word selection logic can greatly reduce the number of logic lines between the word address decode logic and the word line matrix. The reduction in the number of logic lines results in a greater loading per line. For example with 4096 word lines single level circuitry requires 128 logic lines with worst case loading, of 64 while two level circuitry can reduce the number of logic lines to 32 with worst case loading of 512.

The word address decode circuitry required to drive the hybrid circuit logic inputs results from a tradeoff between speed, power and loading. Figure 5.8 is the equivalent circuit of the interconnection circuitry between the drive and hybrid circuits. The output of the drive circuitry is a step function with amplitude V_s. The drive circuitry has a resistive output

NUMBER OF WORD LINES	FIRST LEVEL				SECOND LEVEL				NUMBER OF LOGIC LINES
	NUMBER OF CIRCUITS	DIMENSION	SO-S7 LOADS	GSI,GS2 LOADS	NUMBER OF CIRCUITS	DIMENSION	SO-S7 LOADS	GSI,GS2 LOADS	
256	16	8×2	32	128	1	8×2	2	8	20
512	32	8×4	64	128	1	8×2	2	8	22
1024	64	8×8	128	128	1	8×2	2	8	26
	64	8×4	128	256	2	8×4	4	8	24
2048	128	16×8	128	256	1	8×2	2	8	34
	128	8×8	256	256	2	8×4	4	8	28
4096	256	16×16	256	256	1	8×2	2	8	42
	256	16×8	256	512	2	8×4	4	8	36
	256	8×8	512	512	4	8×8	8	8	32
8192	512	32×16	256	512	1	8×2	2	8	58
	512	16×16	512	512	2	8×4	4	8	44
	512	16×8	512	1024	4	8×8	8	8	40
16384	1024	32×32	512	512	1	8×2	2	8	74
	1024	32×16	512	1024	2	8×4	4	8	60
	1024	16×16	1024	1024	4	8×8	8	8	48
32768	2048	64×32	512	1024	1	8×2	2	8	106
	2048	32×32	1024	1024	2	8×4	4	8	76
	2048	32×16	1024	2048	4	8×8	8	8	64
	2048	16×16	2048	2048	8	16×8	8	16	56

Figure 5.7   Two Level Word Selection Options.
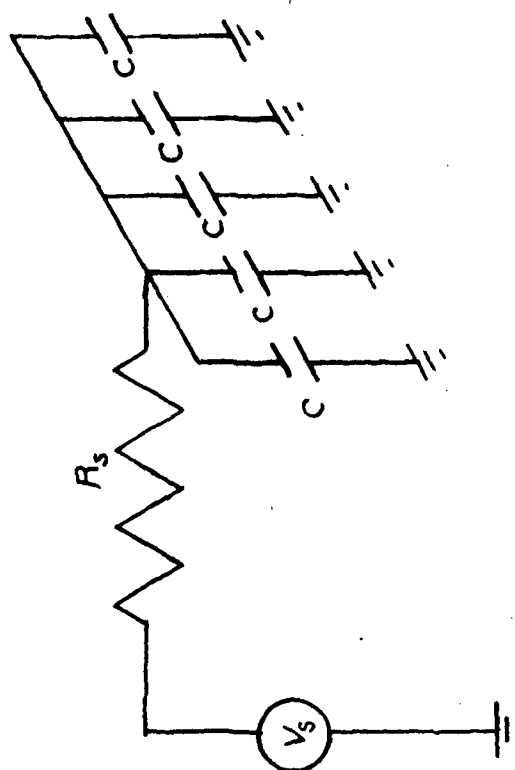
Figure 5.8   Equivalent Circuit of Hybrid Circuit Drive

impedance represented by R_s. The input of each hybrid circuit appears as a capacitive load represented by C. If N hybrid circuit inputs are connected to a single drive circuit the capacitive loading on the drive circuit is NC. The voltage as a function of time delivered to the hybrid circuit is given by:

$$V = V_s (1 - e^{-\frac{t}{R_s NC}})$$

The hybrid circuit FET is switched when V reaches a magnitude of V_c. This occurs at the time of $t = t_c$. Thus the switching time is defined by the equation

$$V_c = V_s (1 - e^{-\frac{t_c}{R_s NC}})$$

Solving this equation for t_c yields

$$t_c = R_s NC \, L_n (1 - \frac{V_c}{V_s})$$

The switching speed can be increased by reducing R_s. R_s can be decreased only by increasing the power into the drive circuit. The relationship between drive circuit output impedance and dissipated electrical power can be represented by the formula

$$P = E^2 / R_s$$

where P is the supplied power and E the power supply voltage. Assuming that C, V_c, V_s and E are constants the relationship between speed, power and the number of hybrid circuit loads becomes

$$t_c = KN/P$$

5.2.3   Bit Line Selection

During a write cycle the bit lines must be supplied with a dc write
current.   The polarity of the write current determines whether a "1" or
a "0" is written.   During a read cycle the bit lines supply a high
frequency signal which must be sensed.   The logic state is sensed by the
phase of the high frequency read signal.   The phase of the digit line
signal is determined by comparing its output with the output of a dummy
digit line.Figure 5.9 is a circuit diagram of the digit line selection
circuitry.   Sixteen digit lines are connected to inputs B0 through B15.
The digit lines are divided into two groups of eight.   A dummy line is
provided for each digit line group and connected to D0 for digit lines
B0 through B7. (group 1) and to D1 for digit lines B8 through B15 (group
2).

Each digit line and dummy line is connected to a FET switch.   In both
read and write select, a single digit line FET and a dummy line FET is
made to conduct.   The selection of the desired digit line is accomplished
in the same manner as word line selection was accomplished with the word
line circuitry.   Two sets of logic signal inputs is used.   One set consist-
ing of 8 logic inputs on lines S0 through S7 selects one digit line in each
group.   The other logic input set on lines GS0 and GS1 selects the desired
group.   For example to select the digit line connected to B3 for either a
read or a write operation logic line S3 and GS0 are both provided with a
true signal while all other logic inputs are held at a false level.   This
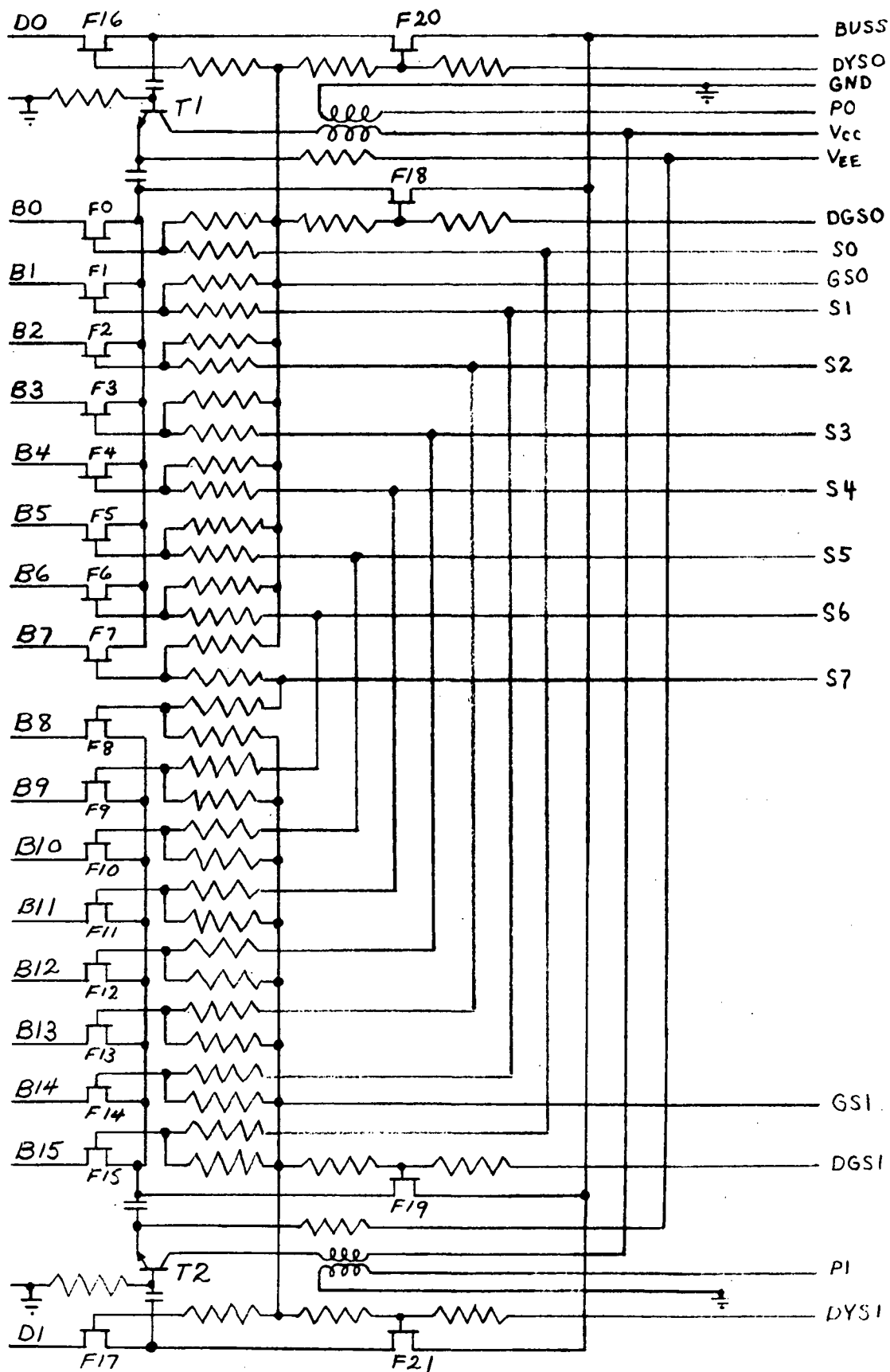
Figure 5.9 Digit Matrix Circuitry

causes FET's F3 and F16 to conduct. In a read operation the dummy line output from DO and the digit line output from B3 are both gated to transistor T1 which acts as a differential amplifier. Isolation capacitors allow only the high frequency digit and dummy line signals to pass through to the differential amplifier. The output of the differential amplifier is transformer coupled to the hybrid circuit output on PO. To write a bit on line B3 the proper polarity write current is supplied to the bus input and a true logic signal supplied to DGSO. The logic input on DGSO causes F18 to conduct.

Dummy lines can be written by write current on the bus line and causing F16 and F20 to conduct to write DO or F17 and F21 to conduct to write D1. F16 and F20 are caused to conduct by supplying a true logic level to DYSO and DGSO and a true logic level supplied to DYS1 and DGS1 causes F17 and F21 to conduct.

The organization of the digit line selection logic differs from the word line selection logic in that more than one bit line is selected at each read or write cycle. The bit lines are divided into N groups where N is the number of bits written or read at each memory request.

This includes both data bits and error detection and error correction bits if included. The address decoding logic is shared by each group.

5.3 ERROR CORRECTION AND DETECTION

5.3.1 Application

There are several reasons for mechanizing error correction and detection within the mass memory. In an avionics application where the memory is

used to store critical flight programs an undetected memory error can cause the loss of the mission or even the vehicle. Systems can be organized so that a corrective action can be taken in the event of an error. Typical corrective actions are to read a redundant copy of the data in error or to switch to a backup system. To initiate either of these actions the memory error must be detected. There are other organizations such as triple redundancy with majority voting which do not require the specific function of error detection, however the reliability of these organizations can be increased by incorporating error detection capabilities. In order to facilitate ground checkout and maintenance it is desirable to incorporate error detection within the memory.

Errors in communications systems exist in two types. The first type is random bit errors traced to a transient or permanent component malfunction. This type of error is characteristic of magnetic memory technologies, when a previously operational unit begins to show failures. The second type of error is a failure within the medium, when signal fading causes loss of transmission of a series of bits. This type of error is less common in magnetic memory systems than in communication systems. Thus, although error correction advances are made to handle error strings of multiple bit length, the beneficiary of these codes is the communication applications, rather than the normally equivalent memory applications.

A criteria for sufficiency of the error correction capability is to detect and correct a single bit. To maintain on line data validity, the capability to detect a second error while correcting the first is desirable and re-commended. The cost of implementing further hardware at this stage is

a step function, therefore another technique to utilize spare lines may be employed. The technique would be especially applicable when a serial bus is available at the interface. Extra pulses to advance the shift register may be inserted to bypass the normal synched transmission of the word, effectively inserting a bit position or deleting a bit position to provide a corrected word. The capability to repeatedly correct words with single errors is limited by the number of spare bits implemented in the design.

To maintain cognizance of the current state of the memory, a memory map is required. Assume erroneous bits are to be deleted in the page of memory currently addressed. The pattern of erroneous bits, i.e., extra internal clocling pulses required, is to be inserted from the map to a recirculating register parallel to the normal address/data register. This implementation provides repeated error correction capability in the bit dimension. The case of errors in the word dimension becoming intolerable is handled through the standard software techniques of bypassing sections of the memory.

Error correction can significantly increase the memory system reliability. All error correction mechanizations inherently include error detection to mechanize error correction and error detection requires the inclusion of additional bits in each memory word. In the following discussions n will represent the number of information bits (or data bits) stored in each memory word and K will represent the number of added error detection or error correction bits. Thus the total number of bits in each word is n + K.

5.3.2 Error Detection

The detection of a single bit error is most simply mechanized using a parity concept. To implement parity only one bit must be added to each memory word independent of the length of the memory word. An exclusive-or of all the data bits in the word is taken and the additional parity bit either set to the results of the exclusive or (termed even parity) or to the complement of the exclusive or (termed odd parity). Upon reading the word from memory errors are detected by reconstructing the parity bit from the read data bits and comparing the reconstructed result with the stored parity value. The data is assumed correct if the reconstructed and stored parity bit compare. The capability of the parity concept is detection of a single erroneous bit.

5.3.3 Error Correction

An error correction mechanization incorporates enough additional bits to allow the error to be isolated to a single bit. The error is then corrected by complementing the erroneous bit. The number of k correction bits must be sufficient to address all of the bits in the memory word, i.e., both the data bits and correction bits. The correction bits must allow one other combination to indicate that no error has occurred. With n data bits a single error correction code requires that

$$2^K \geq n + K + 1$$

Figure 5.10 shows the maximum value of n for several values of K. The column shows the value of K, the second column the maximum number of data bits which can be corrected with the given value of K, the third column the total word length (i.e., n + K) and the fourth column the efficiency computed from the ratio of n to n + K. For data lengths other than shown a value of K is required which produces a value of n larger than the desired length. E. G. if n is 32, the value of K must be 6 resulting in a total word length of 38 bits.

K	n	n + K	efficiency
1	0	1	0%
2	1	3	33%
3	4	7	57%
4	11	15	73%
5	26	31	84%
6	57	63	90.5%
7	120	127	94.6%
8	247	255	96.9%
9	502	511	98.2%
10	1013	103	99.0%

Figure 5.10 Single Error Correction Data and Correction Bit Lengths

The Hamming code is a single error correction code requiring K correction bits. The Hamming code is best described through an example. The example will contain 4 data bits which according to figure 9 requires 3 correction coding bits for a total word length of 7 bits. To define an error correction code the method by which the correction bits are formed and the method of detecting and correcting an error must be described.

In order to describe these processes more concisely a mathematical shorthand will be used. First the binary operations of add (+) and multiply (·) will be defined by

$$0 + 0 = 0$$
$$0 + 1 = 1 + 0 = 1$$
$$1 + 1 = 0$$

which is an exclusive or function and

$$0 \cdot 0 = 0$$
$$0 \cdot 1 = 1 \cdot 0 = 0$$
$$1 \cdot 1 = 1$$

which is the logical and function.

The four bit data word to be represented by a vector $\bar{D}$ such that

$$\bar{D} = \begin{vmatrix} D_1 \\ D_2 \\ D_3 \\ D_4 \end{vmatrix}$$

For example if the data word contains (1010) then $D_1 = D_3 = 1$ and $D_2 = D_4 = 0$ giving

$$\bar{D} = \begin{vmatrix} 1 \\ 0 \\ 1 \\ 0 \end{vmatrix}$$

Generation of the 7 bit encoded word can be represented as the matrix equation

$$\bar{C} = \begin{vmatrix} 1 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix} \cdot \bar{D} = \begin{vmatrix} D_1 + D_2 + D_4 \\ D_1 + D_3 + D_4 \\ D_1 \\ D_2 + D_3 + D_4 \\ D_2 \\ D_3 \\ D_4 \end{vmatrix} \qquad (1)$$

From this it can be seen that the third, fifth, sixth and seventh encoded bits are the original data bits and the first, second and fourth encoded bits are formed from parity generation on subsets of the data word bits. Figure 5.11 is a block diagram of the encoding requirements of the above
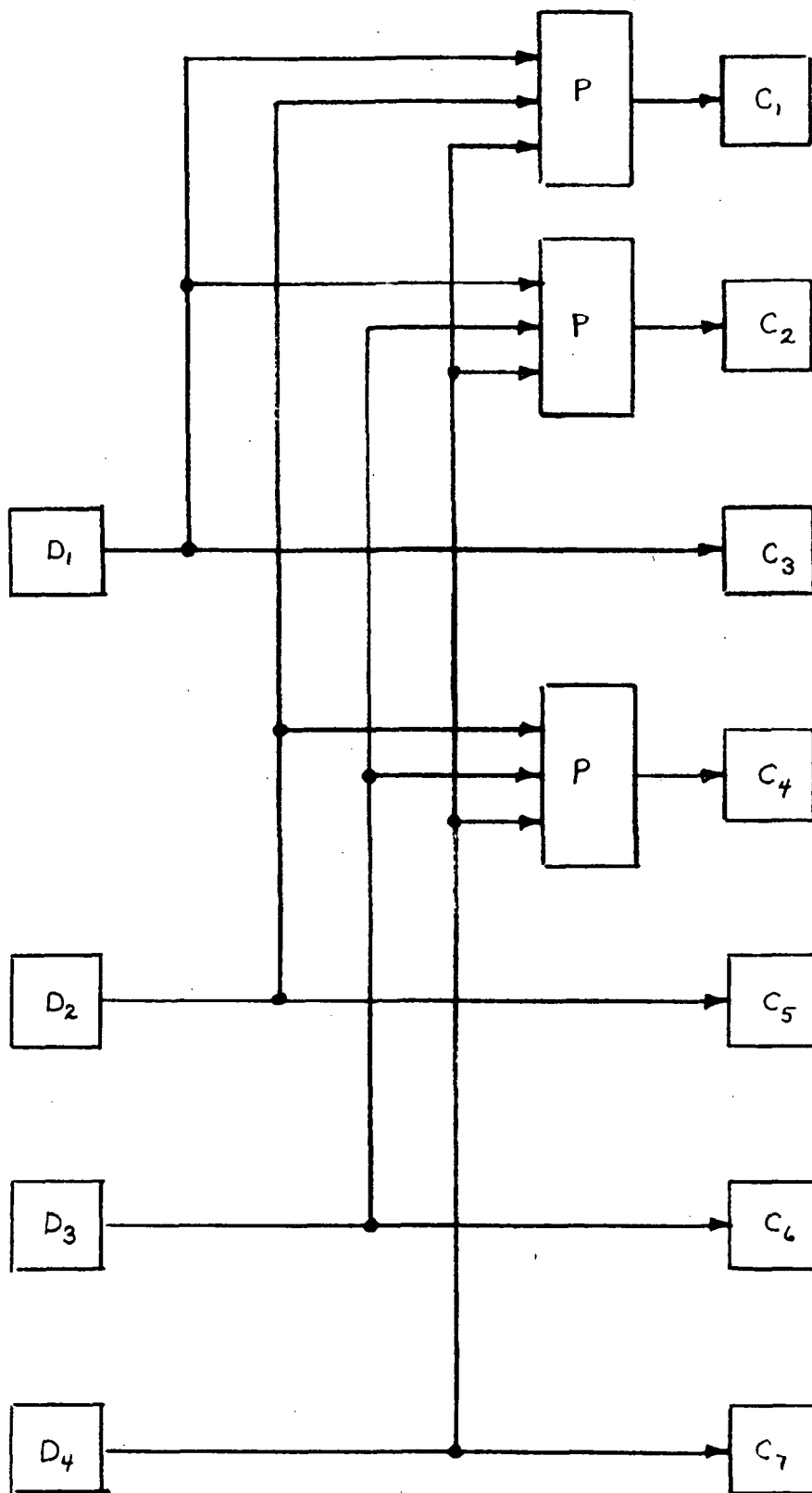
Figure 5.11   Encoding Block Diagram

equation. The blocks marked P generate the parity from the three inputs.

The decoding process takes the 7 encoded bits and reconstructs the original 4 data bits under the conditions that either one or none of the encoded bits have changed state. The decoding process consists of first generating a three bit word called the syndrome. From the syndrome the determination of whether an error has or has not occurred and which bit is in error is made. The syndrome is computed from the matrix equation

$$\bar{S} = \begin{vmatrix} 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{vmatrix} \cdot \bar{C} = \begin{vmatrix} C_4 + C_5 + C_6 + C_7 \\ C_2 + C_3 + C_6 + C_7 \\ C_1 + C_3 + C_5 + C_7 \end{vmatrix} \qquad (2)$$

Figure 5.12 is a block diagram of the syndrome generation process. Since the syndrome contains 3 bits it can contain 8 possible coded states. The interpretation given to each of the eight possible syndrome states is

S_1	S_2	S_3	ERROR
0	0	0	None
0	0	1	C_1
0	1	0	C_2
0	1	1	C_3
1	0	0	C_4
1	0	1	C_5
1	1	0	C_6
1	1	1	C_7

The above interpretation is that if all syndrome bits are zero no error has occurred and if an error has occurred the binary count contained in the syndrome bits
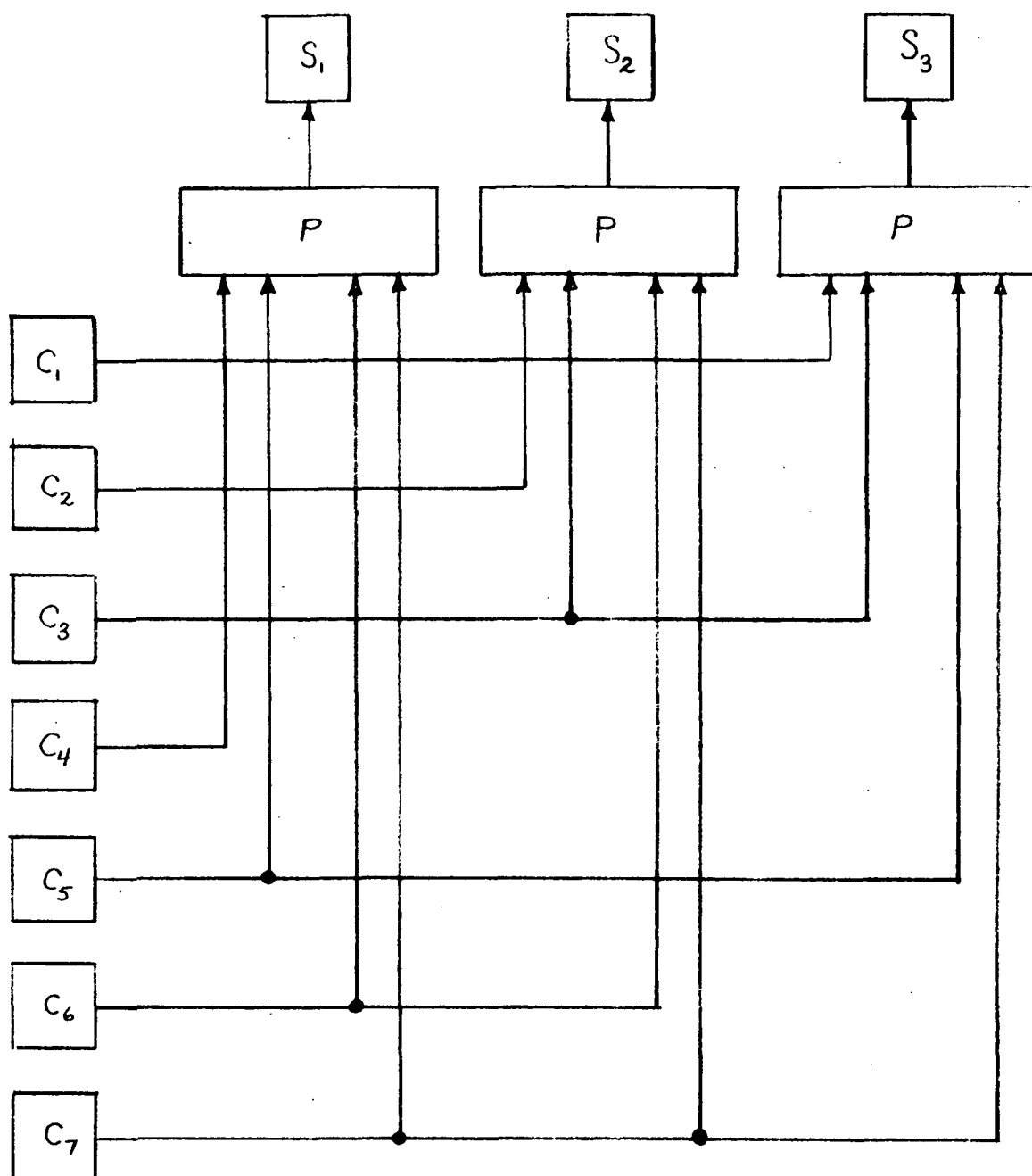
Figure 5.12 Syndrome Generation

addresses the bit in error. As an example assume the original data bits are (1010). Applying equation 1 yields an encoded word of (1011010). Applying equation 2 to this pattern yields a syndrome of (000) indicating no error. If an error has occurred in the 5th binary digit causing the encoded pattern to be read as (1011110) equation 2 would produce the syndrome (101) indicating the 5th binary digit was in error.

There are several means of mechanizing the correction procedure. The syndrome can be decoded into four logic states one for each data bit, with the appropriate data bit toggled if the decoded logic state exists. These logic states for the example are:

$$\bar{S}_1 \ S_2 \ S_3$$
$$S_1 \ \bar{S}_2 \ S_3$$
$$S_1 \ S_2 \ \bar{S}_3$$
$$S_1 \ S_2 \ S_3$$

A second method is to place the 7 bits read from memory into a shift register and the syndrome in a counter. The shift register is connected so that a cyclic or end around shift will occur. The register is caused to shift 7 times and with each shift the syndrome counter is counted down. When the syndrome counter is counted to zero the data bit to be corrected will always occupy the same position in the shift register and thus that position can be toggled.

Errors in a memory result from either noise or from hardware failures.
If an error correction mechanization is implemented to account for hard-
ware failures then consideration must be given to failures in the hardware
used to encode and decode the error correction and detection. A failure
in the error detection and correction logic can cause the erroneous
correction of correct data. Procedures can be simply mechanized to detect
failed error detection and correction logic. If a single error occurs in
the encoding logic used during the memory write cycle the error will be
corrected during the read cycle. However any other memory error
will then constitute a double error which will be erroneously corrected.
Encoding errors can be detected by using the syndrome generation logic
to check the encoded results. The syndrome output should always show no
error when checking the encoding logic.

The syndrome generation logic has two failure modes. First it can indicate
an error when no error exists and secondly it can indicate no error when
an error exists. The procedure to detect the first type of failure is to
proceed with the correction and then regenerate the syndrome on the corrected
data. If a syndrome logic failure has occurred the regenerated syndrome
will still indicate the existance of an error. To test for no error
indication when an error exists is a more difficult task. By complementing
the last encoded bit $(C_7$ in the example) all syndrome outputs should be 1 if
all syndrome outputs were origionally 0 (the condition with no error detected).
By complementing all encoded bits a new error free code results. A complete
failure mode analysis of the syndrome generation logic is required to

guarantee that all possible failure paths are tested. However the
two tests   1) complementing the last encoded bit and testing for all
syndrome outputs being 1 and 2) complementing the remaining
encoded bits and testing for all syndrome bits being 0, test all
syndrome failure modes which would result in no error detection when an
error exists.

Errors in the correction logic are checked by regeneration of the syndrome
after the completion of the correction. Failure in the correction logic
will result in a syndrome indicating an error when the second syndrome
is generated.

By adding one more bit to each memory word, additional detection capabilities
can be achieved. The additional bit is encoded by generating parity over
the Hamming encoded results. This additional bit provides single error
correction double error detection capabilities. With a parity bit added
four possible conditions exist which are:

Hamming Indication	Parity Indications
No Error	No Error
Error	Error
No Error	Error
Error	No Error

The first condition (no error indicated by Hamming or parity) indicates that
proper error free operation has occurred. The second condition indicates a
single error has occurred and can be corrected by the Hamming procedure.
The third condition indicates a single error in the parity bit has occurred.
The fourth condition indicates a double uncorrectable error has occurred.

```
11011010101101010101010101101010
10110110011011001100110011011001
10000000000000000000000000000000
01110001111000111100001111000111
01000000000000000000000000000000
00100000000000000000000000000000
00010000000000000000000000000000
00001111111000000011111111000000
00001000000000000000000000000000
00000100000000000000000000000000
00000010000000000000000000000000
00000001000000000000000000000000
00000000100000000000000000000000
00000000010000000000000000000000
00000000001000000000000000000000
00000000000111111111111111000000
00000000000010000000000000000000
00000000000001000000000000000000
00000000000000100000000000000000
00000000000000010000000000000000
00000000000000001000000000000000
00000000000000000100000000000000
00000000000000000010000000000000
00000000000000000001000000000000
00000000000000000000100000000000
00000000000000000000010000000000
00000000000000000000001000000000
00000000000000000000000100000000
00000000000000000000000010000000
00000000000000000000000001000000
00000000000000000000000000111111
00000000000000000000000000100000
00000000000000000000000000010000
00000000000000000000000000001000
00000000000000000000000000000100
00000000000000000000000000000010
00000000000000000000000000000001
```

Figure 5.13   32 Bit Encoding Matrix

```
00000000000000000000000000001111111
00000000000000111111111111111110000000
00000001111111100000000111111110000000
00011110000111100001111000011110000111
01100110011001100110011001100110011001
10101010101010101010101010101010
```

Figure 5.14   Syndrome Generation Matrix
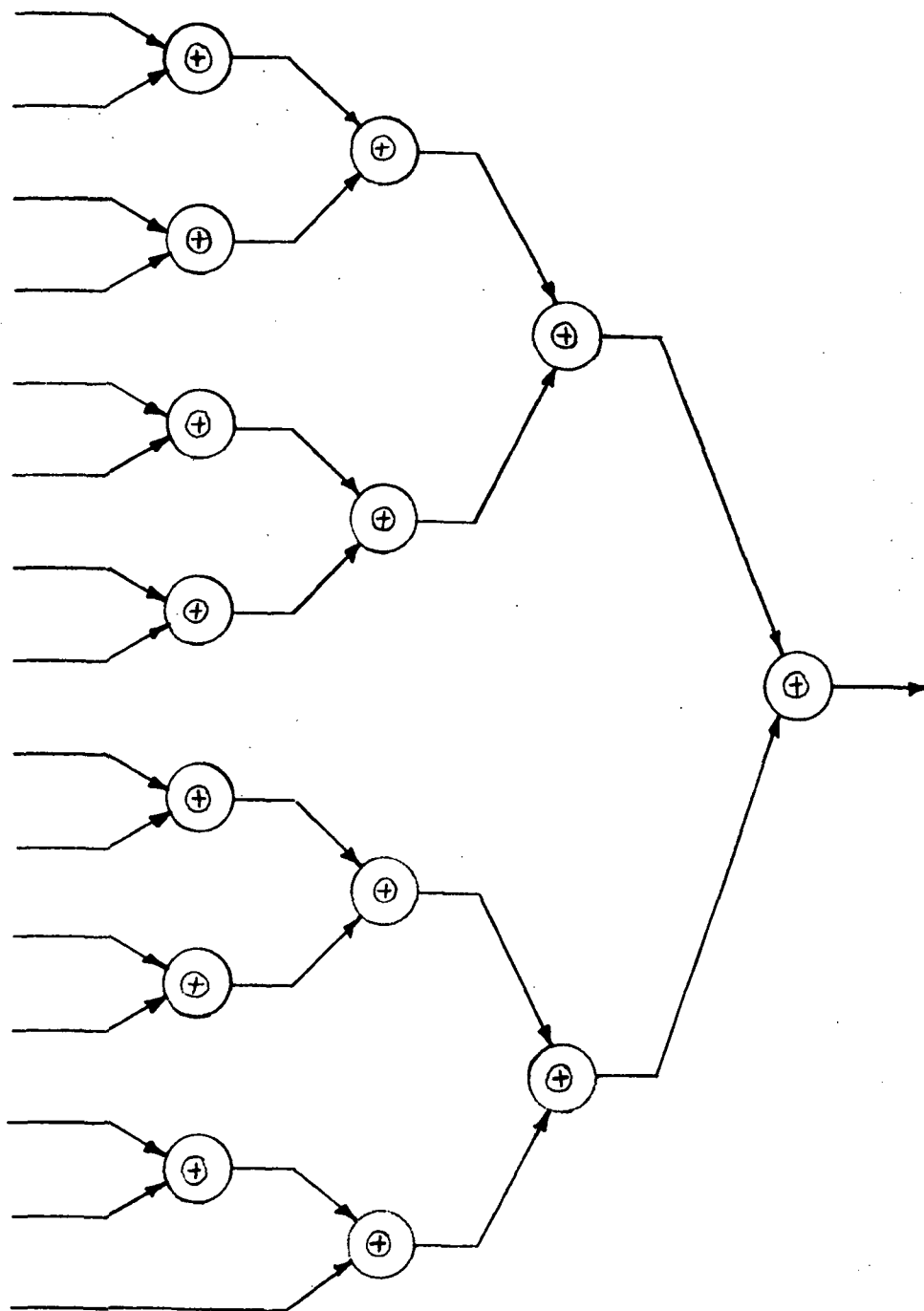
Figure 5.15   Parity Generation Logic

Since the memory will be 32 bit, data word length compatible it is likely

that a 32 bit data word length will be used, though any data word length

which is an integer multiple of 32 bits can be used. The encoding matrix

for 32 data bits is shown in figure 5.13 and the syndrome generation matrix

in figure 5.14. The hardware implementation of the encoding and syndrome

matrix requires multiple input parity generating logic. Parity generation

is obtained by using exclusive or gating.Figure 5.15 shows the logic

required to obtain a 15 input parity generation using 2 input exclusive

or gates. With 15 inputs 14 2 input exclusive or gates are required. In

general an N input parity generation network requires N-1 two input exclusive

or gates. The combined encoding and syndrome generation matrices for

several word lengths expressed as the number of required 2 input exclusive

or gates is given in figure 5.16. The first column gives the number of

data bits. The second column the number of 2 input exclusive or gates

Word length	Exclusive or gates	reduced design
16	75	57
32	174	122
64	403	249
96	643	363

Figure 5.16 Encoding and Syndrome Logic Requirements

required to mechanize the Encoding and Syndrome logic if each multiple

input parity tree is mechanized independently. Investigating the

intermediate logic terms generated in each parity tree mechanization shows that some terms are duplicated. Removing this duplication results in the number of 2 input exclusive or gates listed in the third column.

5.3.4 Reliability Enhancement

The main purpose of employing error detection and correction logic is to increase the memory reliability. The reliability model of the memory is a series string of elements including such items as power supply, memory control unit, timing and control logic, etc. One of these series reliability elements is the bit direction circuitry which includes the bit lines, bit selection logic, sense amplifiers and error correction detection logic. Because the bit direction circuitry contains the bit lines, sense amplifiers and bit selection logic it represents a significant portion of the total memory and a significant contributor to total memory reliability. In order to develop a reliability model of the bit direction circuitry for use in analyzing the error and correction logic a failure probability $P_{f_{s_b}}$ is defined. $P_{f_{s_b}}$ is the probability that a failure will occur in one Nth of the bit lines or one Nth of the selection logic or a specific sense amplifier during a given mission, where N is the number of data bits in a word. The total probability that a bit failure will occur in a memory without error correction and detection logic is then

$$P_f = 1 - (1 - P_{f_{s_b}})^n$$

In adding error correction and detection logic X additional bit lines per word must be added and the error correction and detection logic which is

defined to have a mission failure probability of P_{f_p}. The probability that a memory bit error will occur then is

$$P_f = 1 - \left[(1-P_{f_{sb}})^{N+X} + (N+X)(1-P_{f_{sb}})^{N+X-1} P_{f_{sb}} \right] (1-P_{f_p}) \qquad (2)$$

Equations 1 and 2 can be expanded to give

$$P_f = NP_{f_{sb}} - \frac{N(N-1)}{2} P_{f_{s_b}}^2 + \cdots \qquad (3)$$

and

$$P_f = P_{f_p} + \frac{(N+X)(N+X-1)}{2} P_{f_{s_b}}^2 + \cdots \qquad (4)$$

Measuring P_{f_p} as a ratio of $P_{f_{sp}}$ allows equation 4 to be rewritten as

$$P_f = K \, P_{f_{sb}} + \frac{(N+X)(N+X-1)}{2} P_{p_{s_b}}^2 \qquad (5)$$

Figure 5.17 shows equations 3 and 5 evaluated for a 32 data bit word length, (N=32) and for various values of k and $P_{f_{s_b}}$. The value of X was made equal to 7, the requirement for the Extended Hamming code. The figure shows that even in an extreme case where the error correction and detection logic is 8 times more complex than a single bit line circuitry and mission failure probabilities are high, a factor of 2 improvement in reliability is achieved and that a more typical improvement figure would be 20.

Figure 5.17 Effect on Failure Probabilities Of Error Correction
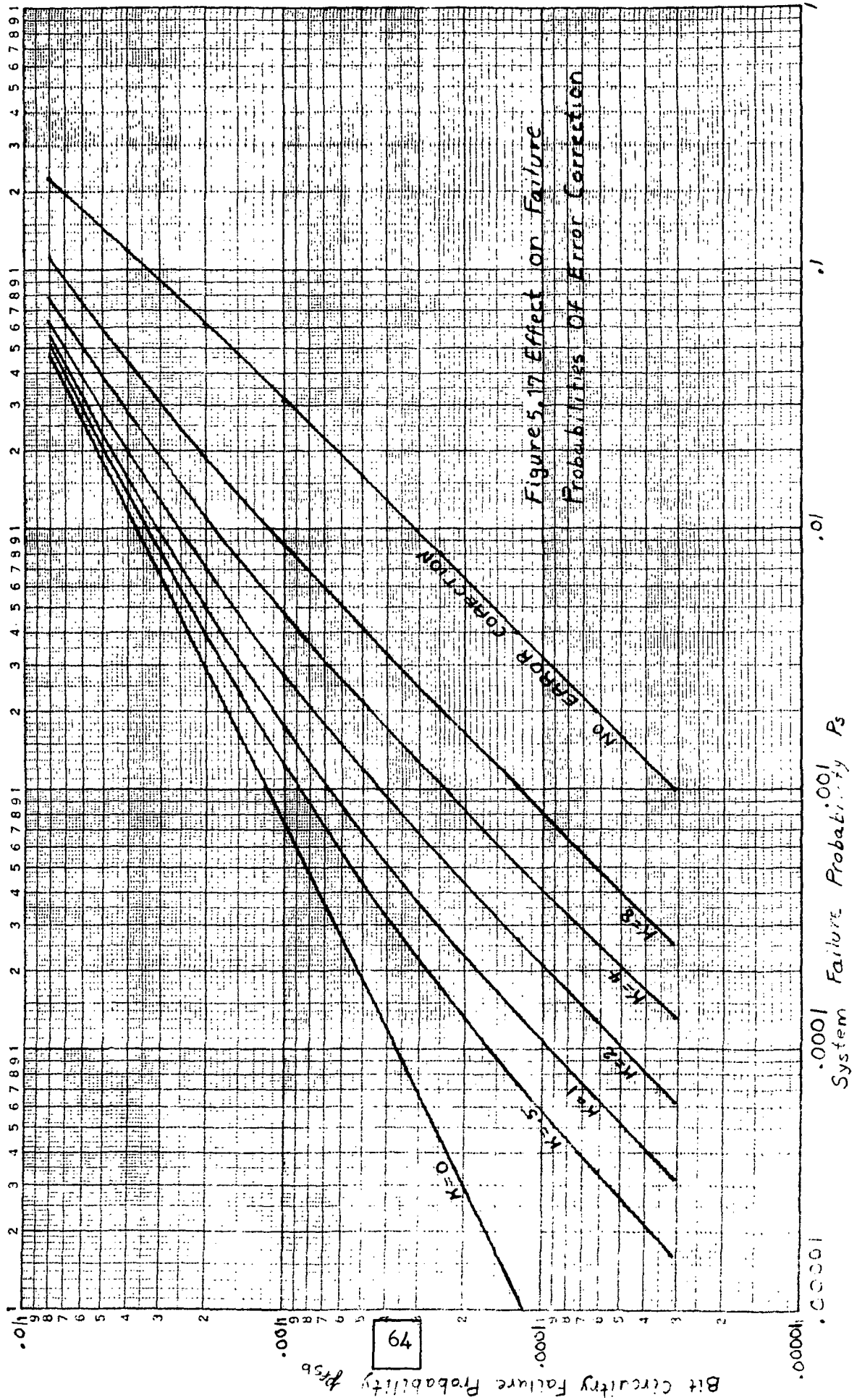
5.4 Operational Parameters

5.4.1 Digit/Word Current Margins

There exists boundaries on word and digit current magnitudes. If these
boundaries are exceeded a write operation can result in the wrong state
being written or destructive readout rather than non-destructive read-
out can occur during a read operation. Margins are an inherent character-
istic of all memories indicating the range of input signals over which
the memory will operate. Memory investigations to this point in time
have been primarily devoted to maximizing these current margins.

5.4.2 Line Length

The electrical characteristics of the word and digit lines exhibit
distributed line resistance and shunt capacitance to ground. The shunt
capacitance in conjunction with the line resistance causes the current
along the line to decrease in magnitude with distance from the current
drive source. Considering this phenomenon in conjunction with the word
current margins limits the maximum word line length. Setting the current
at the drive source end of the word line to the upper current margin
boundary, limits the word line length to where the minimum current margin
boundary is produced at the oppostie end of the line. Two methods
exist for decreasing the shunt capacitance and thus increasing

the word line length. The capacitance can be reduced by either increasing the separation between the magnetic film and the line or by decreasing the line width. Both of these methods result in a reduction of signal output during the read operation, reducing the memory signal to noise ratio. The shunt capacitance effect upon the digit lines is less severe causing a reduction in signal output only with no major effect upon margins.

5.4.3 Line Spacing

The spacing between adjacent word and digit lines determines the bit density.   Since maximum line length is limited as described above, line spacing dictates the number of bits along any line. If the line spacing is too small reading and writing a bit will disturb adjacent bits. Adjacent bit disturb is to some extent controllable by reducing line width and reducing film thickness.

5.4.4 Line Width and Film Thickness

Reducing line width or film thickness will reduce the influence of bits upon their adjacent neighbors. A reduction of line width or film thickness also reduces the amount of magnetic material used in recording each bit. The reduction in magnetic material results in a reduction of output signal during a read cycle and thus a decrease in signal to noise ratio. An additional effect of reducing line width is to increase the distributed line resistance. An increase in distributed line resistance causes the current loss along the line to increase resulting in a reduction of the maximum allowable line length.

5.4.5 Word Current Frequency

The frequency of the word current and thus the frequency of the

digit line sense signal influences the line length, the output

sense signal magnitude and memory speed. Increasing the frequency in-

creases the attenuation caused by the distributed line shunt capacitance,

thus reducing the maximum line length. The digit line sense signal

magnitude is directly proportional to word current frequency thus

the memory signal to noise ratio increases with word current frequency.

To read or write the memory a fixed number of word current cycles must

occur. By increasing the word current frequency the duration of each

cycle decreases thus increasing memory speed.

5.4.6 Array Design

This interplay of primary memory parameters presents a multivariable design

problem. The determination of the optimum memory configuration can occur

only after a lengthy testing and analysis effort. To date this effort has

produced an array having adequate margins and signal to noise ratios to allow

reliable operation with fair bit densities. Further studies of array para-

meters can be expected to offer significant improvements in density and

speed. Univac selected the present configuration with a conservative view

such that wide array margins exist. The major parameter values of the

present design (feasibility model) are:

maximum word line length	-	122 cm (48 in)
maximum digit line length	-	122 cm (48 in)
minimum word line spacing	-	.015cm (.006in)
minimum digit line spacing	-	.031cm (.012 in)
word current frequency	-	10 MHz
digit sense frequency	-	20 MHz
word line width	-	.0076cm (.003 in)
digit line width	-	.010cm (.004 in)

The line length must be shared between the film overlay length and the line termination circuitry. The termination circuitry requires approximately 25 cm of this length making 97 cm available for film overlays. The film substrates are made in approximately 5 cm squares with clearance space between each square. The result is that the maximum stack size has 2808 digit lines and 5616 word lines. Using these values it is possible to construct in a single stack 8,388,608 (2^{23}) data bits plus sufficient additional storage area for dummy digit lines, parity, error correction/detection codes and 12.5% spare word lines. This results in a requirements for 12 stacks of this size to obtain 10^8 data bits.

6.0 TRADE STUDY DEFINITIONS

6.1 Memory Option Definition

There are many design options available for inclusion in a 10^8 bit oligatomic

mass memory trade study. Gross considerations of trade factors such as

weight, reliability, maintainability and cost along with technological

constraints of present oligatomic memory development have led to three primary

designs which will be compared in the trade studies. Within each primary

design option there are suboptions which consider the selection of parity,

error correction/detection (ECD) and spare word lines within the design.

Figure 6.1 is a list of the primary and sub-options with governing character-

istics of each. Technology constraints restrict the number of bits which

can be placed upon a single memory array. These constraints exist because

of an interplay between digit/word current margins, line length, line spac-

ing, line width, film thickness and word current frequency. In order to show

this interplay basic characteristics of each effect will be discussed. Figure

6.2 shows how multiple stacks may be connected.

Option	Module size	Parity	ECD	Spare Word Lines
1	10^8 bits	NO	NO	NO
1A	10^8 bits	YES	NO	NO
1B	10^8 bits	YES	YES	NO
1C	10^8 bits	YES	YES	YES
2	16M bits	NO	NO	NO
2A	16M bits	YES	NO	NO
2B	16M bits	YES	YES	NO
2C	16M bits	YES	YES	YES
3	8M bits	NO	NO	NO
3A	8M bits	YES	NO	NO
3B	8M bits	YES	YES	NO
3C	8M bits	YES	YES	YES

Figure 6.1 Memory Trade Study Options

1. A 10^8 bit memory where 12 memory stacks are placed in a single package. This option provides best allowable packaging parameters, with potential loss in flexibility, form factors, and architectural options.

2. A 16 million bit module, thus requiring 6 modules to obtain 10^8 bits. Each module will contain 2 memory stacks. This option compares the baseline to a single stack per module. Other multiples of the stack can be extrapolated.

3. A 8 million bit module, thus requiring 12 modules to obtain 10^8 bits. Each module will contain 1 memory stack. This stack is above the minimum capacity required by the flight programs, and representative of a building block with low capacity.

For each primary option the same set of four reliability directed suboptions will be investigated.

These four suboptions are:

A. The memory will contain no parity, no error correction/detection (ECD) encoding and no spare word lines.

B. The memory will contain a parity bit for each 32 bit word but have no ECD encoding or spare word lines.

C. The memory will contain parity and ECD encoding (i.e., extended Hamming Code) in each 32 bit word but have no spare word lines.

D. The memory will contain parity and ECD encoding and 12.5% spare word lines.

An additional dimension of suboptions will be defined below (Section 6.2.16) as a variation of word selection logic.

6.2 Detailed Hardware Definitions

Figure 6.3 is a detailed memory block diagram showing the major memory elements. The functions required of the most complex suboptions (i.e., suboption C and D) are shown and indicated as ECD testing, ECD generation, parity testing and parity generation. In the less sophisticated suboptions these blocks

are eliminated as indicated by the suboption definition. The following is a brief description of each functional block including estimates of parameters important in establishing weight, power, reliability and cost.

6.1.2 Power Supply

It is assumed that the memory will require four different dc supply voltages. The power supply consists of a multi-winding transformer supplying four diode full wave rectifiers. Each rectified output is filtered and voltage regulated. Power transient protection is provided by automatically off sequencing the memory upon detection of a lower limit primary supply voltage. Off sequencing will await the completion of any memory cycle in process. The power supply filters provide sufficient energy storage for the execution of at least one memory cycle. Electrical on/off switching is provided on the primary. The total power supply contains the following parts:

transformer	- 1
chokes	- 4
capacitors	- 28
resistors	- 42
diodes	- 16
transistors	- 22
solder connections	- 260

It is assumed that the power supply will be designed for the specific application and will have an overall power efficiency of 70%.
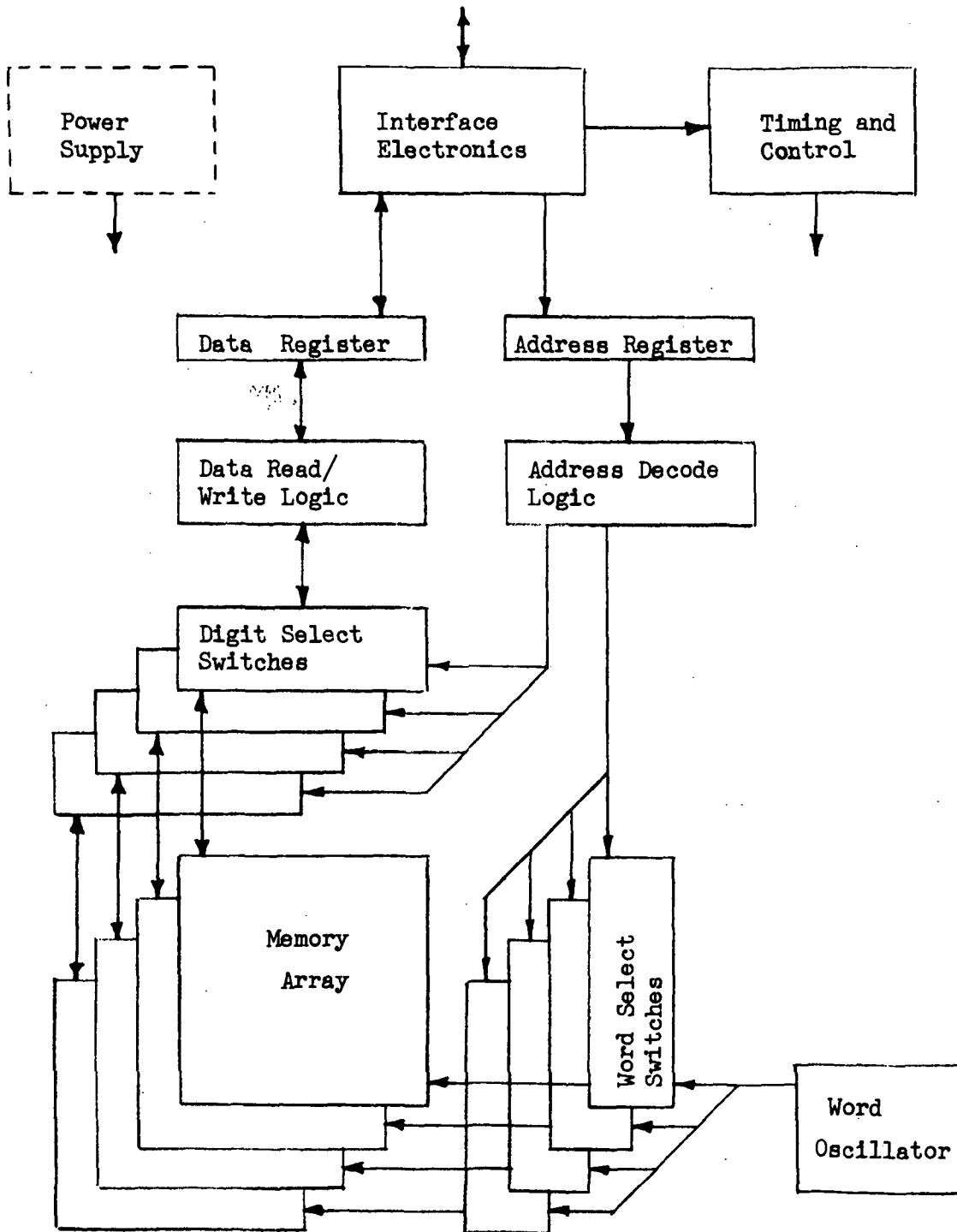
Figure 6.2   Typical Functional Memory Block Diagram
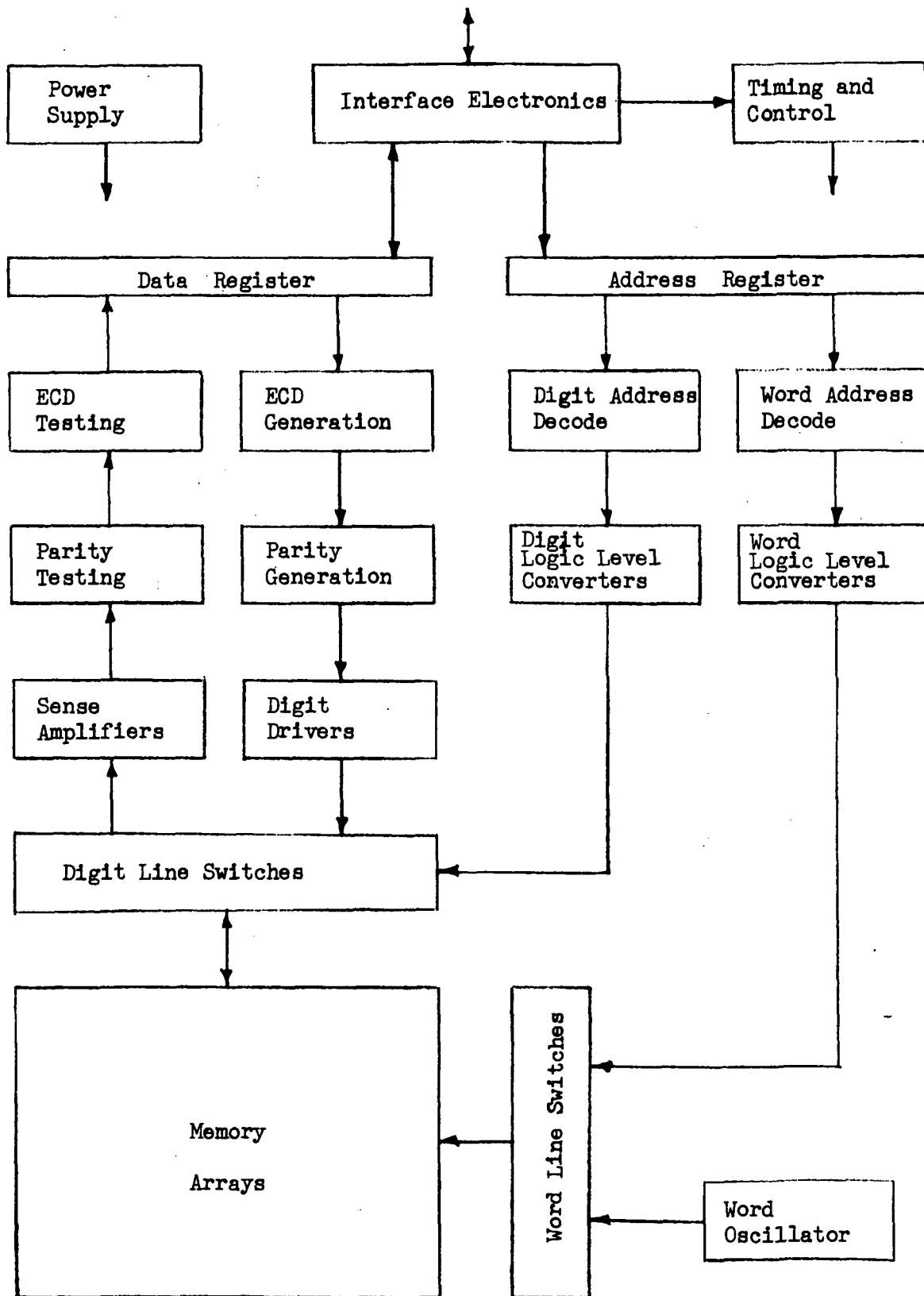
Figure 6.3   Detailed Memory Block Diagram

6.2.2   Interface Electronics

The interface electronics will receive and deliver data on two different
memory channels, one serial and the other parallel. Priority logic
will resolve conflicting requests between the two channels. The serial
channel will provide buffering to allow for the parallel channel to
operate while a serial to parallel or parallel to serial conversion
is occuring in the serial channel. It is assumed that the interface
electronics is mechanized using integrated circuits. The total number
of IC's required to mechanize the dual channel interface is dependent
upon the primary option mechanized. For each of the three options
the required number of integrated circuits are assumed as:

Option 1   (10^8 bits)   - 48 IC's

Option 2   (16 M bits)   - 47 IC's

Option 3   (8 M bits)   - 46 IC's

6.2.3   Timing and Control Electronics

The timing and control electronics provides the source of all logic
signals to cause the sequential memory operations to occur in a timely
manner. The word current oscillator is the internal primary
clock.   The timing and control logic is assumed to be mechanized
entirely with IC's. The timing and control circuitry is dependent upon
the suboption employed. For each suboption the following number of
IC's are estimated:

Suboption A	-	12 IC's
Suboption B	-	16 IC's
Suboption C	-	21 IC's
Suboption D	-	21 IC's

6.2.4 Data Register

The data register includes 32 flip-flops, one for each bit in the data word, independent of the option or suboption. Assuming two flip-flops per IC yields a total requirement of 16 IC's for the data register.

6.2.5 Address Register

The address register length is dependent upon the number of memory words and thus dependent upon the primary options. The number of address bits required to address each option is:

Option 1	-	22 bits
Option 2	-	19 bits
Option 3	-	18 bits

Assuming 2 flip-flops per IC the number of IC's required to mechanize the address register for each option is:

Option 1	-	11 IC's
Option 2	-	10 IC's
Option 3	-	9 IC's

6.2.6 ECD Testing

The ECD testing logic is required only in suboptions C and D.
The ECD testing logic consists of register storage for an additional
6 data bits read from memory, the syndrome generation logic, correction
logic incorporating parity testing results and fault indication
outputs. It is estimated that the total number of IC's required to
mechanize the ECD testing logic is 26.

6.2.7 Parity Testing

Parity testing is included only in suboptions B, C, and D. The number
of bits which must be tested is dependent upon the presence of ECD
codes. The estimated logic requirements for parity testing for each
suboption is:

Suboption A	- 0 IC's
Suboption B	- 4 IC's
Suboption C	- 5 IC's
Suboption D	- 5 IC's

6.2.8 Sense Amplifiers

Each sense amplifier must provide 80 to 90 db of gain with controlled
phase shift characteristics. The discrete components required to
mechanize a sense amplifier are:

transistors	- 9
resistors	- 33
capacitors	- 21
solder connections	-153

The number of sense amplifiers required is dependent upon the number of bits read from memory on each read cycle, and thus the suboption used. For each suboption the number of sense amplifiers required is:

Suboption A   - 32

Suboption B   - 33

Suboption C   - 39

Suboption D   - 39

6.2.9   ECD Generation

The ECD generation logic is required only in suboptions C and D. The ECD generation logic consists of generating 6 parity terms. To generate these 6 parity terms requires 11 IC's.

6.2.10   Parity Generation

The parity generation logic is used only in suboptions B,C, and D and consists of generating a single parity output for all bits to be stored in the memory. The number of IC's required is dependent upon whether ECD codes are mechanized and thus upon the suboption employed. The number of IC's required for each suboption is:

Suboption A   - 0 IC's

Suboption B   - 3 IC's

Suboption C   - 4 IC's

Suboption D   - 4 IC's

6.2.11   <u>Digit Drivers</u>

The digit drivers convert the logic level outputs of the data register, ECD generation logic and Parity generation logic to a current source for driving the digit lines during a write operation. The digit drivers are mechanized from discrete components with each digit driver consisting of:

transistors	- 5
resistors	- 8
capacitors	- 4
diodes	- 1
solder connections-	43

The number of digit drivers is dependent upon the suboption employed and for each suboption are:

Suboption A	- 32
Suboption B	- 33
Suboption C	- 39
Suboption D	- 39

6.2.12   <u>Digit Address Decode</u>

The digit address decode logic is dependent upon the primary option being mechanized. The digit address decode logic determines which set of digit lines are connected to the digit drivers or sense amplifiers depending upon a memory read or write cycle. The number of digits in

each set is dependent upon the suboption i.e., 32 for suboption A,

33 for suboption B and 39 for suboption C and D.   The number of sets

in each memory array is 64 independent of the primary option or sub-

options. The number of memory arrays is dependent upon the primary

option with 12 memory arrays required for option 1, 2 for option

2 and 1 for option 3. The digit address decode logic must generate

logic outputs enabling the digit line switches to select 1 set

out of 768 for option 1, one set out of 128 for option 2 and

1 set out of 64 for option 3. The digit line switches require

coincident inputs to select a digit line. The digital address

decode logic is divided into two sections, each section providing

half of the coincident input requirements. Each section decodes

a separate portion of the address register bits into independent

logic states. The number of logic states required by each section

for each primary option is:

Option	Section 1	Section 2
1	24	32
2	8	16
3	8	8

The number of IC's required to perform the digit address decoding for each option is:

Option 1	- 4 IC's
Option 2	- 2 IC's
Option 3	- 2 IC's

6.2.13 Digit Logic Level Converters

For each output of the Digit Address decode logic a level converter must be provided to change the logic voltage outputs to the voltage values required by the digit line switches. Each level converter requires the following discrete components.

transistors	- 4
resistors	- 7
capacitors	- 1
diodes	- 2
solder connections	- 37

The number of digit logic level converters required in each option is:

Option 1   - 56

Option 2   - 24

Option 3   - 16

6.2.14   Digit Line Switches

The digit line switches are manufactured in hybrid circuits.   The

hybrid circuits consist of placing resistors using a silk screening

process on a printed circuit substrate. Transistors, capacitors

and transformers are added as discrete components with the completed

circuit packaged as a sealed unit. Each hybrid circuit services

eight digit lines plus a dummy digit line and includes the phase

detection and pre amplifier circuitry. Each hybrid circuit contains:

transistors   -   11

resistors   -   31

capacitors   -   3

transformers   -   1

solder connections* -   225

More than one level of digit line switching is required. An example

is best used to show the requirements of additional switching levels.

Option 1A has a total of 27648 digit lines including the dummy lines.

This requires a total of 3072 digit line switch hybrid circuits on the

first level of switching. Thus there are 3072 outputs which must be

routed to 32 sense amplifier inputs or 96 outputs to each input.

*For reliability calculations it is assumed that the silk screened resistor
connections to the printed circuit are similar to a solder connection.

Connecting all 96 switch outputs to a sense amplifier input will result
in excessive noise and signal loss. By providing a second level of
switching the 96 inputs are reduced to 12. The maximum sense
amplifier fan-in is 16 thus a fan-in of 12 is acceptable. The
table below shows the first level, second level and total number of
hybrid circuits required for each option.

Option	First level	Second level	Total
1A	3072	384	3456
1B	3168	396	3564
1C	3744	468	4212
1D	3744	468	4212
2A	512	0	512
2B	528	0	528
2C	624	0	624
2D	624	0	624
3A	256	0	256
3B	264	0	264
3C	312	0	312
3D	312	0	312

6.2.15 Word Line Switches

The word line switches are manufactured using hybrid circuit technology.
Each hybrid circuit contains

transistors	-	20
resistors	-	20
solder connections	-	175

Each hybrid circuit can select one of 16 word lines, thus there is a
hybrid line switching circuit for each 16 word lines. The number of
hybrid circuits required is thus determined by the number of word
lines which in turn is dependent upon the primary option being considered.
For each primary option the number of hybrid circuits required are:

Option 1	-	3072
Option 2	-	512
Option 3	-	256

6.2.16 Word Address Decode

There are two options available for mechanizing the word address decode
logic. The memory contains several memory arrays, i.e., 12 for
option 1, 2 for option 2 and 1 for option 3. Some of the address register
bits determine the memory array being referenced. These bits are used
in the digit line switches to determine which memory array is used as an

input to the sense amplifiers or receives digit current during a write operation. Since switching between arrays is provided in the digit direction it is not necessary to provide switching between the arrays in the word direction. If switching between arrays is not provided in the word direction then word current will flow in one word line of each array during each read and write operation. Word current magnitudes are critical for proper memory operation and are generated by a controlled current source supplied by the word current oscillator. Individual word line impedance is not controlled to the same degree of accuracy as that required for word current magnitude. Therefore word lines cannot be driven in parallel. Thus in order to allow word currents to simultaneously flow in a word line in each memory array requires that each array be provided with its own current source.

The second option requires that the word address decoding logic provide outputs to select between the memory arrays. Each word address decoding output must be provided with a logical level converter. For each primary option the number of word address decoding outputs are:

        Option 1   -   448

        Option 2   -   192

        Option 3   -   128

If word current is allowed to flow in a single word line in each memory array the number of word address decoding outputs is 128.

A second level of suboptions will be defined and designated as x and y where suboption x allows word current flow in a single word line and suboption y allows word current flow simultaneously in one word line in each array. The number of IC's required to mechanize the word address decode logic for each primary option and sub-option is:

Option 1x	- 30 IC's
Option 2x	- 7 IC's
Option 3x	- 2 IC's
Options 1y, 2y, or 3y	- 2 IC's

The selection of suboptions A, B, C and D does not affect the word address decode logic.

6.2.17 Word Logic Level Converters

A word logic level converter must be provided for each word address decode output. The word logic level converters are the same as the digit logic level converters containing the following discrete components:

transistors	- 4
resistors	- 7
capacitors	- 2
diodes	- 2
solder connections	- 37

The number of word logic level converters required for each primary option and each x and y suboption is:

         Option 1x   - 448

         Option 2x   - 192

         Option 3x   - 128

         Options 1y,
                 2y, and
                 3y   - 128

6.2.18   Word Oscillator

The word oscillator produces a crystal controlled sinusoidal output at a frequency of 10 MHz. The output must have very low harmonic distortion for proper memory operation. The output of the oscillator is a current amplifier which will provide a constant 55 ma. of current to a word line. For those options having more than one word line driven at the same time a current driver for each line must be provided. The components required to mechanize the oscillator are:

         transistors   - 5

         diodes   - 2

         resistors   - 12

         capacitors   - 6

         crystals   - 1

         solder connections - 57

The components required to mechanize each current driver are

    transistors   - 5

    diodes   - 1

    resistors   - ·7

    capacitors   - 4

    solder connections - 45

The number of current drivers required is dependent upon the primary option and the x and y suboptions:

    Options 1x, 2x, and 3x - 1

    Option 1y   - 12

    Option 2y   - 2

    Option 3y   - 1

6.2.19 Memory Arrays

The number of memory stacks employed is dependent upon the primary option:

    Option 1   - 12

    Option 2   - 2

    Option 3   - 1

The number of lines on each stack is dependent upon the suboption employed:

Option	Word lines	Digit lines
A	4096	2304
B	4096	2376
C	4096	2808
D	4608	2808

The word and digit line spacing is .015cm. (.006 in) and .031cm (.012in) respectively. To account for spacing between substrates average line spacings of .017cm and .034cm will be assumed. This results in single stack dimensions and areas for each suboption of:

Option	Length	Width	Area
A	69.6cm(27.4in)	78.3cm(30.8in)	5455 sq. cm(846 sq.in.)
B	69.6cm(27.4in)	80.8cm(31.8in)	5625 sq. cm(872 sq. in.)
C	69.6cm(27.4in)	95.5cm(37.6in)	6648 sq. cm(1030 sq. in.)
D	78.3cm(30.8in)	95.5cm(37.6in)	7479 sq. cm(1159 sq. in.)

The above estimates of hardware required to achieve each memory function must be used to determine which option and suboption should be selected for implementation. The selection must be based upon the relative influence of each option upon the trade factors of cost, weight, volume, reliability, power speed, and maintainability. Since two of the primary options are modular designs requiring several modules to achieve the full 10^8 bit capacity, comparisons will be based upon implementing a full system having 10^8 bit capacity. Each trade factor will be evaluated separately.

7.0 TRADE PARAMETER EVALUATION

7.1 Cost

The most meaningful cost measure for determining the relative merit of optional system designs is total cost of ownership. Total cost of ownership has four visible factors.

Development, non-recurring
Cost to purchase, recurring
Logistics
Payload Delivery Cost

The non-recurring costs are measured from a given state-of-the-art to implement a recommended design. The costs may vary directly with the amount of risk in the development. The design options within the descriptions have been normalized to an existing state-of-the-technology. Thus no further consideration of this factor is required for option comparison. Cost comparisons with other technologies may be based on breakthroughs required for a viable memory technology, and consideration of the questions; "Does the memory technology fill a need in a given performance range?" and "Is the performance range wide enough to allow multiple applications?" The oligatomic technology provides optimistic answers to both of these questions.

In determining the recurring costs of a mass memory the relationship between the number of units produced and the cost per unit must be considered. Analysis of historical data on a new technology film memory provided the following results:

Production cost of the 18th unit was 48% the production cost of the first unit.
Production cost of the 50th unit was 38% of the first.

Figure 7.1 shows a graph of the relative production costs as a function of the number of units produced. In order to apply this curve to the cost analysis the expected number of units produced must be known. In fulfilling a 10^8 bit requirement, 6 times more option 2 units must be produced than option 1 units, and 12 times more option 3 units than option 1 units. As a point for comparison it will be assumed that 10 memories of 10^8 bit capacity are to be produced. The important cost computation for comparison purposes is the production costs of the total number of units required by each option to produce the desired number of 10^8 bit memories. That is the total production cost rather than the Nth unit production cost. This factor is computed from the integral under the curve. Normalizing costs to the first production unit in each option yields the cost for the first 10 option 1 units is 7.33 times the first option 1 unit cost, the cost for the first 60 option 2 units is 28.62 times the first option 2 unit cost and for the first 120 option 3 units is 50.95 times the first option 3 unit cost.

Figure 7.1 COST VARIATIONS DUE TO UNITS PRODUCED
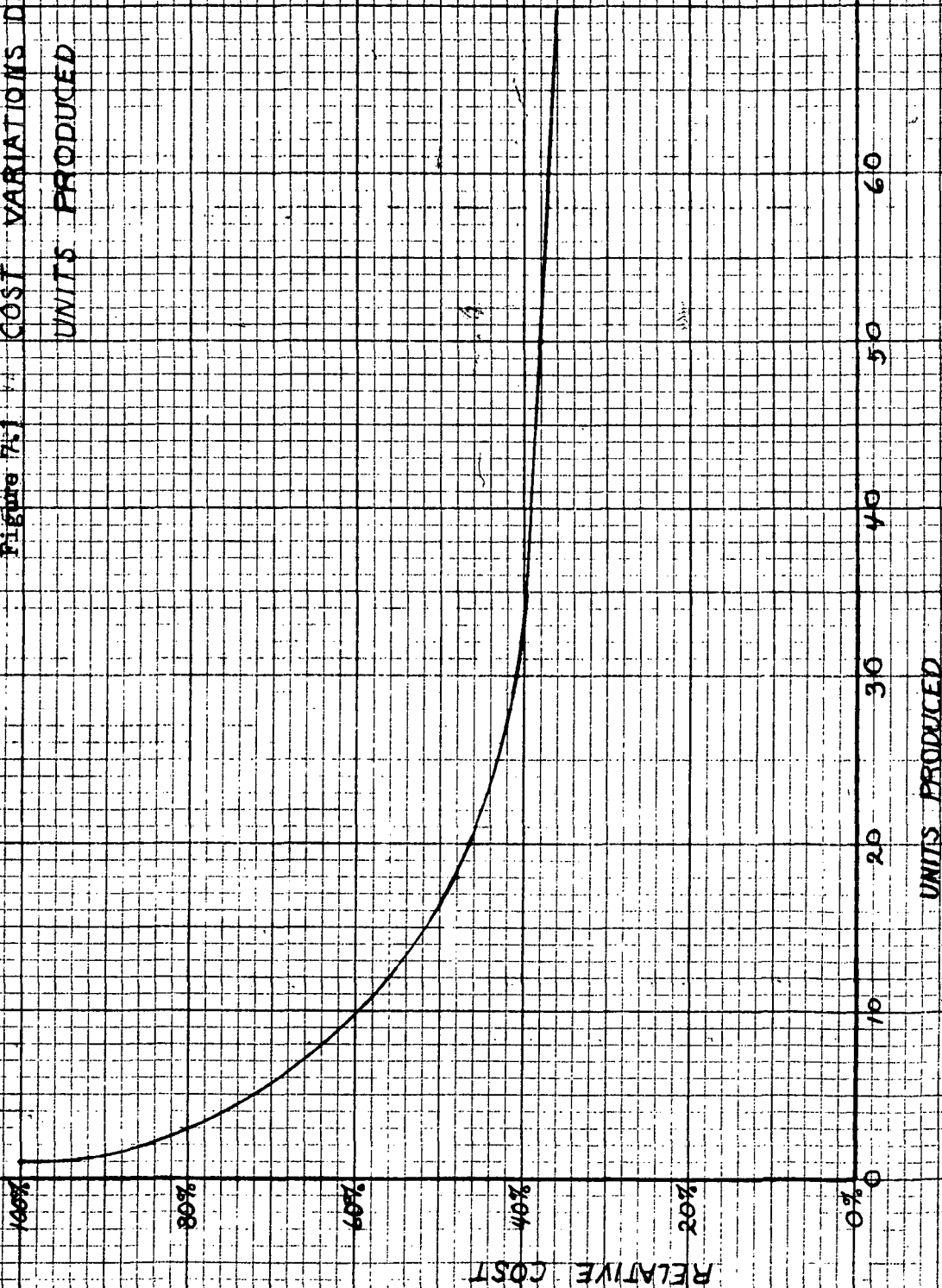
These cost factors will be applied when comparing the relative costs of the primary options. The unit cost estimates of each primary option and suboption will be developed from a total parts count. The completed assembly costs will be estimated for each part and thus a total unit cost determined from the parts count. Figure 7.2 is a list of the parts required for each design option. For the D suboption which will include spare word line switches additional hybrid circuits have been added. In an actual mechanization of this option additional switches would be added to each existing hybrid circuit rather than increasing the total number of hybrid circuits. The estimated cost of each component including amortized assembly, packaging, testing, printed circuit, fabrication, inspection and rework costs are:

transistors	$2.16
resistors	$1.39
capacitors	$1.49
integrated circuits	$13.90
diodes	$1.44
transformers	$19.38
chokes	$11.34
crystals	$16.34
hybrid digit switch	$38.96
hybrid word switch	$38.40
array costs	$ .54 per sq. cm

These cost figures are estimates based upon engineering opinion and do not represent actual memory costs. Actual costs would have to be based upon a detailed analysis of all cost sources with a known quantity to be manufactured. To develop actual cost data for the number of options being studied is beyond the scope of a trade study. The cost estimates are of sufficient accuracy to obtain relative cost merits between the various designs.

	IC's	Transistor	Resistor	Capacitor	Diode	Switch	Switch	Array Area
1Ax	121	2496	4901	1790	1059	3072	3456	65460
1Ay	93	1271	2738	1194	430	3072	3456	65460
1Bx	132	2510	4942	1815	1060	3072	3564	67500
1By	104	1285	2779	1219	431	3072	3564	67500
1Cx	176	2594	5188	1965	1066	3072	4212	79776
1Cy	148	1369	3025	1369	437	3072	4212	79776
1Dx	176	2594	5188	1965	1066	3456	4212	89748
1Dy	148	1369	3025	1369	437	3456	4212	89748
2Ax	94	1344	2885	1246	483	512	512	10910
2Ay	89	1093	2444	1122	340	512	512	10910
2Bx	105	1358	2926	1271	484	512	528	11250
2By	100	1107	2485	1147	341	512	528	11250
2Cx	149	1442	3172	1416	490	512	624	13296
2Cy	144	1191	2731	1292	347	512	624	13296
2Dx	149	1442	3172	1416	490	576	624	14958
2Dy	144	1191	2731	1292	347	576	624	14958
3Ax	87	1056	2381	1110	339	256	256	5455
3Ay	87	1056	2381	1110	339	256	256	5455
3Bx	98	1070	2422	1135	340	256	264	5625
3By	98	1070	2422	1135	340	256	264	5625
3Cx	142	1154	2668	1285	346	256	312	6648
3Cy	142	1154	2668	1285	346	256	312	6648
3Dx	142	1154	2668	1285	346	288	312	7479
3Dy	142	1154	2668	1285	346	288	312	7479

Figure 7.2   Parts Count for Trade Configurations

The cost per memory module is determined by summing the component costs over all of the components for each configuration. The results of this summation are shown in figure 7.3. Direct comparisons of the data is not meaningful since the bit capacity of the three primary options is different. Figure 7.4 shows the unadjusted costs required for each option in mechanizing a 10^8 bit memory. Figure 7.5 is the unadjusted cost per bit of each memory option. These cost values have not been adjusted for the difference in number of modules produced. The estimated component costs are based upon producing more than one item. Since it is assumed that the estimated cost figures are true for the average production costs of the first 10 units and ten 10^8 bit memorys are to be manufactured, then the option 2 costs should be reduced by 34.9% and the option 3 costs by 42.1%. Figure 7.6 and 7.7 give the adjusted average 10^8 bit memory costs and the per bit memory costs for the various options. These are the cost figures which should be used for relative comparisions assuming that the total number of 10^8 bit memories to be manufactured is near 10. Comparing these cost figures shows that costs are reduced by modularizing the 10^8 bit designs. Comparing figure 7.6 with figure 7.4 shows this cost reduction is due to a reduction in per unit costs with the number of units produced. Between the A, B, C and D suboptions the cost increases as additional memory features are added as would be expected. A contribution to cost which has not been included but which will influence the relative costs of the D suboption is yield. By employing word line spares correcting single bit failures or word line

	1	2	3
A	306.1	56.4	31.8
B	311.7	57.4	32.5
C	344.9	63.6	36.2
D	365.1	66.2	37.9

Suboption x

A	298.3	54.7	31.8
B	303.9	55.8	32.5
C	337.1	62.0	36.2
D	357.2	64.6	37.9

Suboption y

Figure 7.3 Memory Module Cost (K dollars)

A	306.1	338.4	381.6
B	311.7	344.4	390.0
C	344.9	381.6	434.4
D	365.1	397.2	454.8

Suboption x

A	298.3	328.2	381.6
B	303.9	334.8	390.0
C	337.1	372.0	434.4
D	357.2	287.6	454.8

Suboption y

Figure 7.4 10^8 Memory Cost (K dollars)

	1	2	3
A	.304	.336	.379
B	.310	.342	.387
C	.343	.379	.431
D	.363	.395	.452

Suboption x

	1	2	3
A	.296	.326	.379
B	.302	.333	.387
C	.335	.369	.431
D	.355	.385	.452

Suboption y

Figure 7.5 Memory cost per bit (cents)

	1	2	3
A	306.1	220.3	220.9
B	311.7	224.2	225.8
C	344.9	248.4	251.5
D	365.1	258.6	263.3

Suboption x

	1	2	3
A	298.3	213.7	220.9
B	303.9	218.0	225.8
C	337.1	242.2	251.5
D	357.2	252.3	263.3

Suboption y

Figure 7.6 Adjusted 10^8 bit memory costs (K dollars)

	1	2	3
A	.304	.219	.219
B	.310	.223	.224
C	.343	.247	.250
D	.363	.257	.262

Suboption x

	1	2	3
A	.296	.212	.219
B	.302	.216	.224
C	.335	.240	.250
D	.355	.250	.262

Suboption y

Figure 7.7   Adjusted cost per bit (cents)

failures during manufacturing would be greatly simplified. Thus
depending upon the yields experienced suboption D could show a lower
cost than other suboptions. Comparing the suboption x and y shows that
suboption y has the least cost.

7.2 Power

The importance of power as a trade factor is application dependent.
For a space application where power is an important trade factor several
minor design modifications can be mechanized to conserve total energy
drain upon the spacecraft power source. A major means of reducing the
power load is to take advantage of the memory duty cycle. In a normal
application a mass memory is used only for brief periods of time. Typically
a mass memory duty cycle may be below 1%. Unless special provisions are
made to shut off the power to the memory when it is not in use, it will
continue to use almost full power even without data being read from
or into the memory. Thus a 99% reduction in power can be achieved by
turning off the power to the memory when it is not in use. For the purposes
of this study, power will be assumed to be an important trade factor.
If it is not an important trade factor the total analysis of power as
a parameter is meaningless. The power requirements of each memory
functional element is discussed below.

Power Supply - The power used by the power supply is dependent upon
the output power which must be provided. Good power supply design
will result in efficiencies as high as 70% in a memory application.
Thus to account for power supply losses the total power requirements of
the remaining components will be multiplied by a factor of 1.3.

Interface Electronics - The interface electronics is mechanized using integrated circuits. It will be assumed that each integrated circuit requires 75mw power when operating. The total operating power requirements for the interface electronics is then

Option 1	3600 mw
Option 2	3525 mw
Option 3	3450 mw

Timing and Control Electronics - The timing and control electronics is mechanized using IC's yielding total operating power requirements of

Suboption A	900 mw
Suboption B	1200 mw
Suboption C	1575 mw
Suboption D	1575 mw

Data Register - The data register is composed by 16 IC's which require an operating power of 1200 mw.

Address Register - The address register is mechanized with IC's requiring an operating power of:

Option 1	825 mw
Option 2	750 mw
Option 3	675 mw

ECD Testing - The ECD testing logic is mechanized with IC's requiring an operating power of:

       Suboption A   0 mw

       Suboption B   0 mw

       Suboption C   1950 mw

       Suboption D   1950 mw

Parity Testing - Parity testing is mechanized with IC's requiring an operating power of:

       Suboption A   0

       Suboption B   300 mw

       Suboption C   375 mw

       Suboption D   375 mw

Sense Amplifiers - The sense amplifiers are mechanized using discrete components. Each amplifier has 9 transistors with an estimated average power drain of 65 mw per transistor. The total operating power drain for each suboption is:

       Suboption A   18720 mw

       Suboption B   19305 mw

       Suboption C   22815 mw

       Suboption D   22815 mw

ECD Generation - ECD generation is mechanized using 11 IC's resulting in a operating power drain of:

Suboption A	0 mw
Suboption B	0 mw
Suboption C	825 mw
Suboption D	825 mw

Parity Generation - Parity generation is mechanized using integrated circuits resulting in an operating power drain of:

Suboption A	0
Suboption B	225 mw
Suboption C	300 mw
Suboption D	300 mw

Digit Drivers - The digit drivers are mechanized from discrete components and must provide 31 ma in writing a one and 22 ma in writing a zero. This current is supplied to approximately 400 ohms including the output resistance of the circuitry. If it is assumed that as many ones as zeros are written and that the memory is used only half the time in the write mode (the other half of the time the memory being used in the read mode) then the average output power of the digit driver is 140 mw. In addition to the output power supplied, the digit

driver circuitry has five transistors which require an estimated 30 mw each. The average digit driver power is then 290 mw. The operating power for each suboption is then:

Suboption A	9280 mw
Suboption B	9570 mw
Suboption C	11310 mw
Suboption D	11310 mw

Digit Address Decode - The digit address decode logic is mechanized with integrated circuits having an operating power requirement for each option of:

Option 1	300 mw
Option 2	150 mw
Option 3	150 mw

Digit Logic Level Converters - The digit logic level converters are mechanized from discrete components with an average operating power requirements of 125 mw. The requirement for each option is then:

Option 1	7000 mw
Option 2	3000 mw
Option 3	2000 mw

Digit Line Switches - The majority of the circuitry with the digit line switch hybrid circuit packages is FET switching networks which do not require power supply connections. The power loss of these circuits is accounted for in the power requirements of the drive circuits. Each digit line switch hybrid circuit also includes a sense preamplifier which requires 37 mw of power. The total operating power requirement of the digit line switches for each option and suboption is:

Option 1A	127872 mw
Option 1B	131868 mw
Option 1C	155844 mw
Option 1D	155844 mw
Option 2A	18944 mw
Option 2B	19536 mw
Option 2C	23088 mw
Option 2D	23088 mw
Option 3A	9472 mw
Option 3B	9768 mw
Option 3C	11544 mw
Option 3D	11544 mw

Word Line Switches - The word line switch hybrid circuit packages do not require any directly supplied power from the power supply.

All power absorbed by these circuits is accounted for in those circuits which drive the word line switches.

Word Address Decode - The word address decode logic is mechanized with integrated circuits with a total operating power requirement of:

Option 1x	2250 mw
Option 2x	525 mw
Option 3x	150 mw
Option 1y	150 mw
Option 2y	150 mw
Option 3y	150 mw

Word Logic Level Converters - The word logic level converters are mechanized with discrete components with each converter requiring 125 mw. The total operating power requirement for each option is:

Option 1x	56000 mw
Option 2x	24000 mw
Option 3x	16000 mw
Option 1y	16000 mw
Option 2y	16000 mw
Option 3y	16000 mw

Word Oscillator - The word oscillator and its output current drivers are mechanized from discrete components. The operating power requirements of the oscillator is 325 mw. Each current driver must supply 1210 mw of word current power. The current driver requires 1535 mw to supply this power. The total operating power required by this circuitry for each option is

Option 1x	1860 mw
Option 2x	1860 mw
Option 3x	1860 mw
Option 1y	18745 mw
Option 2y	3395 mw
Option 3y	1860 mw

Figure 7.8 shows the accumulated operating power requirements for each option and suboption. There are several techniques available for reducing the average power requirements of the memory. A mass memory is not used continuously in a typical application. A conservative estimate of memory duty cycle would be 1%. By providing the ability to switch power on and off of the memory and taking advantage of the 1% duty cycle, the average power requirements of each module is a hundredth of that shown.
The modular designs of options 2 and 3 also allow for a reduction in total power requirements, By applying power to only the module under immediate use the operating power requirements of a 10^8 bit modular memory is the power required by a single module. Thus the average power of a 10^8 bit memory assuming a 1% duty cycle for each option is a hundredth of the values given.

	A	B	C
1	197	305	247
2	106	109	125
3	81	84	97

Suboption x

	A	B	C
1	164	172	314
2	97	100	116
3	81	84	97

Suboption y

Figure 7.8   Module Power Requirements (watts)

7.3 Reliability

In developing the reliability trades a basic simplyfing assuption is required. Any component failure, although affecting only a single bit, is counted as a memory failure. In practice , many such failures may be isolated and bypassed without seriously affecting the system. Observations of failures of electronics components show that the life of a typical electronic component can be divided into three periods. The first period is called the infant failure period which is characterized by high failure rates. It is during this period that those parts having manufacturing defects fail. The second period consists of random failures and the third period is where the useful component life has been exceeded and is characterized by increasing failure rates: Reliability analysis is concerned with the second or constant failure rate period. The first period is controlled through proper burn in and derating techniques. The third period can be controlled through adequate preventive maintance and marginal parts replacement. The reliability of a component having constant failure rate, λ , has a negative exponential distribution given by

$$R(t) = e^{-\lambda t} \tag{1}$$

Failure rate is expresses in units of failures per hour and time in hours. The probability of a component successfully completing i.e., not failing during a mission of T hours is

$$R(T) = e^{-\lambda T} \tag{2}$$

The probability of failure is then one minus the probability of success and expressed by:

$$Q(t) = 1 - R(t) = 1 - e^{-\lambda t} \tag{3}$$

Figure 7.9 gives the failure rates for common electronic components. Failure rates are dependent upon the operating environment of the component. Three failure rates are given for each component for the typical environments of a ground based environment, an aircraft avionics environment and a space system environment. The space environment failure rates are applicable to periods of missile launch only, during periods of unthrusting, i.e., zero g environments, the ground based figures apply. The failure rates applicable to any electronic system are dependent upon various controls applied during the manufacturing process. The failure rates are representative but are not necessarily the failure rates which would be obtained in the manufacture of a mass memory. For a particular application failure rates are derated according to expected electrical and mechanical stresses. Derating factors and reliability controls must be taken into account to obtain the actual failure rates applicable to the mass memory. The failure rates are used in developing relative failure probabilities between the defined mass memory options.

Part	Ground	Avionics	Space
ISC	1.06	2.65	9.01
Transistor	1.03	2.58	8.76
Resistor	.018	.036	.090
Capacitor	.157	.314	.785
Transformer	1.57	9.42	109.9
Diode	.051	.076	.133
Core/Spot	.00022	.00143	.0176
Correction	.0071	.071	1.56

Figure 7.9   Failure rates* of common electronic components for ground, airborne, and space environments expressed in units of failure per 10^8 hours

In order to develop the reliability values for a complete system the concepts of series and parallel arrangements must be developed. A series arrangement of n components is characterized by a system failure occurring if any single component failure occurs. In a parallel arrangement of n components all n components must fail before a system failure occurs. The reliability of a series arrangement of n components is given by the formula

$$R(t) = \prod_{i-1}^{n} e^{-\lambda_i t} = e^{-\left[\sum_{i=1}^{n} \lambda_i\right] t} \qquad (4)$$

*Failure rate values and environmental correlation factors taken from Univac Design Practices Manual.

From equation 4 it can be seen that for a series arrangement the system failure rate is the sum of the component failure rates.

For a parallel arrangement the reliability is given by the formula:

$$R(t) = 1 - \prod_{i=1}^{n} (1-e^{-\lambda_i t}) \qquad (5)$$

A measure of the mean time between failures (MTBF) is commonly used as a figure of merit for systems. The MTBF is found from the formula:

$$M_T = \int_0^{\infty} R(t)\, dt \qquad (6)$$

To obtain relative reliability comparisons between the trade options the probability of successfully completing a space mission will be determined for each option. The mission selected for comparison purposes will be a 201 hour space mission (approximately 8 days) in which 200 hours is spent in a zero-g environment and 1 hour is spent in combined launch and in orbit thrusting. The probability of successfully completing a specific mission is chosen as a percentage basis rather than mean time between failure. Probability of mission success is more easily obtained, and the results obtained will be the same as those obtained using mean time between failure. Each memory function will be evaluated spearately and then each memory module evaluated as a whole. For a series reliability arrangement where equation 4 is applicable the probability of mission success for the above defined mission can be written as:

$$R = e^{-\Sigma(200\lambda_{Gi} + \lambda_{Si})} \qquad (7)$$

where λ_{G1} is the ground based failure rates and λ_{S1} is the thrusting failure rates. An intermediate value is defined as:

$$p = \Sigma (200\lambda_{G1} + \lambda_{S1}) \tag{8}$$

giving:

$$R = e^{-p} \tag{9}$$

Values of p and R will be given for the memory functional elements.

1. <u>Power Supply</u> - For the purposes of reliability calculations the power supply is a series memory module element; i.e., a power supply failure results in a memory module failure. The power supply reliability values are:

$$p = 8840 \cdot 10^{-8}$$
$$R = .99991160$$

2. <u>Interface Electronics</u> - The interface electronics is a reliability series element having option dependent parameter values of:

Option	p	R
1	10608.10^{-8}	.999894
2	10387.10^{-8}	.999896
3	10166.10^{-8}	.999898

3. <u>Timing and Control Electronics</u> - The timing and control electronics is a reliability series element having suboption dependent parameter values of

Suboption	p	R
A	2652.10^{-8}	.9999735
B	3536.10^{-8}	.9999645
C	4641.10^{-8}	.9999536
D	4641.10^{-8}	.9999536

4. **Data Register** - The data register is a reliability series element having parameter values of:

$$p = 3536.10^{-8}$$

$$R = .999645$$

5. **Address Registers** - The address register is a reliability series element having option dependent parameter values of:

Option	p	R
1	2431.10^{-8}	.9999757
2	2210.10^{-8}	.9999779
3	1989.10^{-8}	.9999801

6. **Digit Selection, Read, Write and Storage Functions** - Because of the presence of error correction and detection codes as a suboption the total digit side of the memory must be considered as a single function with suboptions A, B, C and D considered independently. In each case the

memory is assumed to have failed if an error in either reading
or writing a single bit or multiple bits will result in erronous
memory outputs. Considering each memory suboption independently.

SUBOPTION A - The digit side of the memory for suboption A consists
of the sense amplifiers,the digit drivers, the digit address decode
logic, the digit logic level converters, the digit line switches,
the array digit lines and the thin film magnetic storage medium.
Since suboption A does not contain error correction detection a single
failure in any element will result in a memory module failure.
- Thus   these functions appear as series reliability elements and
their reliabilities can be determined independently. The reliability
values of each of these functions are:

Sense amplifiers - Suboption A contains 32 sense amplifiers which yield:

$$p = 102048.10^{-8}$$

$$R = .99898$$

Digit Drivers - Suboption A contains 32 digit drivers which yield:

$$p = 43904.10^{-8}$$

$$R = .999561$$

Digit Address Decode Logic - The digit address decode logic is primary
option dependent yielding parameter values of:

Option	p	R
1	884.10^{-8}	.99999116
2	442.10^{-8}	.99999558
3	442.10^{-8}	.99999558

Digit Logic Level Converters - The digit logic level converters are primary option dependent yielding parameter values of:

Option	p	R
1	53200.10^{-8}	.999468
2	22800.10^{-8}	.999772
3	15200.10^{-8}	.999848

Digit Line Switches - The number of digit line switches is primary option dependent yielding parameter values of:

Option	p	R
1	12686285.10^{-8}	.881
2	1879450.10^{-8}	.9814
3	939725.10^{-8}	.99060

Array Digit Lines - For the purposes of reliability calculations it will be assumed that each digit line has two solder connections. The number of digit lines is primary option dependent yielding reliability parameters values of:

Option	p	R
1	164782.10^{-8}	.99835
2	27464.10^{-8}	.999725
3	13732.10^{-8}	.999863

Thin Film Storage Medium - Each bit is stored in a small area of film at the digit and word line intersections. The failure rate of each film storage area is assumed to be $.062.10^{-8}$. For each primary option the reliability parameters are:

Option	p	R
1	7021265.10^{-8}	.9423
2	1170211.10^{-8}	.9884
3	585105.10^{-8}	.99415

Total Suboption A Digit Functions - Because the suboption A digit functions exhibit series reliability characteristics an overall p value can be computed as the sum of all the individual contributor p values. R is then computed in the normal manner as given by equation 9. The accumulated values for suboption A digit functions is then:

Option	p	R
1	20072368.10^{-8}	.818
2	3246319.10^{-8}	.9680
3	1700156.10^{-8}	.9831

SUBOPTION B - The digit function reliability computations for suboption B are performed in the same manner as used for suboption A.

Additional functions of parity generation and detection must be added and other functions increased in size such as the addition of one sense amplifier and additional digit lines. The reliability parameter values are:

Parity Testing

$$p = 884.10^{-8}$$

$$R = .99999116$$

Parity Generation

$$p = 663.10^{-8}$$

$$R = .99999337$$

Sense Amplifiers

$$p = 105237.10^{-8}$$

$$R = .99894$$

Digit Drivers

$$p = 45276.10^{-8}$$

$$R = .999547$$

Digit Address Decode Logic

Option	p	R
1	884.10^{-8}	.99999116
2	442.10^{-8}	.99999558
3	442.10^{-8}	.99999558

Digit Logic Level Converters

Option	p	R
1	53200.10^{-8}	.999468
2	22800.10^{-8}	.999772
3	15200.10^{-8}	.999848

Digit Line Switches

Option	p	R
1	1382731.10^{-8}	.877
2	1938182.10^{-8}	.9808
3	969091.10^{-8}	.99091

Array Digit Lines

Option	p	R
1	169932.10^{-8}	.99830
2	28322.10^{-8}	.999717
3	14161.10^{-8}	.999858

Thin Film Storage Medium

Option	p	R
1	7240679.10^{-8}	.9302
2	1206780.10^{-8}	.988
3	$603390.\ 10^{-8}$	.99397

Total Suboption B Digit Functions

Option	p	R
1	20699486.10^{-8}	.813
2	3348586.10^{-8}	.9671
3	1754344.10^{-8}	.9827

SUBOPTION C AND D - For the purposes of reliability computations, suboptions C and D are identical. The spare word lines added in suboption D are not used when the memory is operationally employed. The spare word lines are used during manufacturing and maintenance. Suboptions C and D both contain error correction/detection codes. The use of error correction/detection codes allows certain types of failures to occur without erroneous memory outputs. In order to evaluate the types of failures which do not produce memory errors each memory digit function must be considered. The memory digit functions are:

ECD test

Parity test

Sense Amplifiers

ECD generation

Parity generation

Digit drivers

Digit Address Decode Logic

Digit Logic Level Converters

Digit Line Switches

Digit Lines

Film storage media

First the Digit Address Decode Logic and Digit Logic Level Converters will be considered. A failure in either of these functions will result in the specification of the wrong memory address, thus these two functions exhibit series reliablity characteristics and produce values of:

Option	p	R
1	54084.10^{-8}	.999451
2	23242.10^{-8}	.999768
3	15642.10^{-8}	.999844

For the purpose of reliability analysis the remaining digit functions can be classified into four groups:

ECD logic

Sense and drive electronics

Digit line switches

Digit lines and storage

The ECD logic contains ECD testing, parity testing, ECD generation and Parity generation logic which is mechanized using a total of 46 IC's. The sense and drive electronics consists of the sense amplifiers and Digit drivers. Each bit position in the memory word requires a sense amplifier and a digit driver. The failure of either the sense amplifier or digit driver will result in the loss of the associated bit position in the word. The combined electronics requirements for a single sense amplifier and digit driver is

transistors	14
resistors	41
capacitor	25
diode	1
solder connection	196

The accumulated p value for this circuitry is $5461 \cdot 10^{-8}$.

Since the failure of a digit line or of any film bit storage area under the digit line both result in the inability for complete retrieval of the data stored along the digit line, these two items can be combined having an accumulated p value of $260 \cdot 10^{-8}$.

Each memory word consists of 39 bits including data, parity and ECD storage. Associated with each bit position is one sense amplifier, one digit driver, 1/39th of the digit line switches and 1/39th of the digit lines and storage. The number of each of these elements associated with each bit position for the primary options are:

OPTION	1	2	3
sense and drive electronics	1	1	1
digit line switches	108	16	8
digit lines and storage	864	144	72

The heart of generating a reliability model for the digit direction of the memory lies in the internal operation of the digit line switches. There are 9 digit lines attached to each first level digit line switch ; eight data lines and a dummy line. Failures within the digit line switch can cause either the loss of a single data line or the loss of all 8 data lines. The accumulated p value for the portion of the digit line switch which when failed, will cause the loss of its associated digit line only, is $p = 262 \cdot 10^{-8}$ and for that portion of the digit line switch which would cause the loss of all 8 data lines is $1579 \cdot 10^{-8}$. In order to discuss the failure modes with ECD, the term "level" will be used to distinguish between non-interacting failures. Each digit line associated with a bit position in the memory word is defined to be at a different level. Thus with 39 bits in each word there are 39 digit lines at each level. A memory failure due to digit line failures occurs only if more

than one digit line fails on the same level.

Several terms must be defined in order to simplify the reliability expressions to be developed. These are defined below.

The ECD logic is mechanized with 46 IC's in a manner that correct memory outputs will be formed even in the event of a single IC failure. Defining R_{EDC} as the mission reliability of a single IC and Q_{EDC} the failure probability of a single IC yields:

$$R_{EDC} = e^{-221.10^{-8}}$$

$$Q_{EDC} = 1-R_{EDC}$$

The reliability of a single combined sense amplifier and digit driver is:

$$R_{S} = e^{-4561.10^{-8}}$$

yielding:

$$Q_{S} = 1 - R_{S}$$

The mission reliability of the portion of the digit switches common to all 8 sense line inputs is defined as:

$$R_{dsc} = e^{-1579 \cdot 10^{-8}}$$

and:

$$Q_{dsc} = 1 - R_{dsc}$$

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The mission reliability of the portion of the digit switch associated with a single digit line is:

$$R_{dss} = e^{-262 \cdot 10^{-8}}$$

and:

$$Q_{dss} = 1 - R_{dss}$$

The mission reliability of a single digit line and its storage media is:

$$R_{dl} = e^{-262 \cdot 10^{-8}}$$

and:

$$Q_{dl} = 1 - R_{dl}$$

The reliability of the digit selection logic is dependent upon the primary option. Reliability formulas will be developed for each option independently. Since option 3 contains the least amount of hardware, its reliability formulas will be developed first.

Option 3 - First the ECD logic will be considered. Correct memory outputs can occur when the ECD has experienced no failures or a single failure. The probability of no ECD logic failures is:

$$R_{EDC}^{46}$$

and the probability of a single failure is:

$$46 R_{EDC}^{45} Q_{EDC}$$

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First under the condition of a single failure, all the read of the digit selection logic must perform in order for correct memory operation to occur. Thus the probability of the digit selection logic operating (excluding the digit addressing and level converters) with an EDC logic failure is:

$$R_1 = 46R_{EDC}^{45} \ Q_{EDC}^{39} \ R_S^{312} \ R_{dsc}^{2496} \ R_{dss}^{3808} \ R_{dl}$$

If no EDC logic failures occur, then failures in other components may be present without erroneous data output from the memory. Taking the sense amplifiers and digit drivers as the next elements in the digit selection logic string, proper memory operation can occur if all sense and driver electronics are functioning or if a single sense and driver electronics failure has occurred. The probability of each of these events under the conditions of the ECD logic operating is:

$$R_{EDC}^{46} \ R_S^{38}$$

for all sense and drive electronics operating and:

$$39R_{EDC}^{46} \ R_S^{38} \ Q_S$$

for a single sense and drive electronic failure.

If a single sense and drive electronics failure has occurred then all remaining digit selection logic must operate except for the digit

line switches and digit lines which act as inputs to the failed

sense and drive electronics. The probability of this

failure is:

$$R_2 = 39 R_{EDC}^{46} \ R_S^{38} \ Q_S \ R_{dsc}^{304} \ R_{dss}^{2432} \ R_{dl}^{2736}$$

With the EDC logic and all sense and drive electronics operating the

common portion of the digit line switches will be considered.

A dummy digit line is supplied to each digit line switch which must

also operate in order to have the common digit line switch electronics

working. There are 8 digit line switches associated with each section

of sense and drive electronics. Thus there are 8 levels of common

digit switch electronics. The probability of either no failure or

a single failure on each level occurring including the associated

dummy digit line is:

$$R_c = R_{dsc}^{39} \ R_{dl}^{39} + 39 \ R_{dsc}^{38} \ R_{dl}^{38} \ (1 - R_{dsc} \ R_{dl})$$

The equation for R_c given above is separated into two terms:

$$R_a = R_{dsc}^{39} \ R_{dl}^{39}$$

which is the probability of no common digit switch electronic failure

or dummy digit line failure on a single level and:

$$R_b = 39 \ R_{dsc}^{38} \ R_{dl}^{38} \ (1 - R_{dsc} \ R_{dl})$$

which is the probability of a single common digit switch and/or dummy line failure on a single level.

Each digit switch has 8 digit line inputs and associated digit line input circuitry which has a mission reliability of:

$$R_X = R_{dss} R_{dl}$$

and associated failure probability of:

$$Q_X = 1 - R_X$$

Thus 8 levels of digit lines exist for each digit switch. If the common digit switch electronics or dummy digit line has failed then all digit lines except those supplying the failed switches must operate. Thus the R_b term must be amended by multiplying by R_X^{38}. If all command digit switch electronics and dummy lines at a single level are operating then individual digit lines can fail as long as no more than a single failure occurs at any digit line level. Thus the R_a term must be ammended by multiplying by

$$(R_X^{39} + 38 R_X^{38} Q_X)^8$$

In light of the above discussion the total mission reliability of the digit selection logic (excluding the address decoding and logic level conversion) for option 3 is:

$$R = R_1 + R_a + R_{EDC}^{46} \; R_S^{39} \left[R_a (R_X^{39} + 39R_X^{38} \; Q_X)^8 + R_b R_X^{304} \right]^8$$

Option 2 - The reliability formula for option 2 can be generated by slight modifications of the development of the above reliability formula. Without discussion:

$$R_1 = 46 \; R_{EDC}^{45} \; Q_{EDC} \; R_S^{39} \; R_{dsc}^{642} \; R_{dss}^{4992} \; R_{dl}^{5616}$$

$$R_2 = 39 \; R_{EDC}^{46} \; R_S^{38} \; Q_S \; R_{dsc}^{608} \; R_{dss}^{4864} \; R_{dl}^{5472}$$

$$R = R_1 + R_2 + R_{EDC}^{46} \; R_S^{39} \left[R_a (R_X^{39} + 39R_X^{38} \; Q_X)^8 + R_b \; R_X^{304} \right]^{16}$$

Option 1 - For option 1 the same type of modifications required in generating the option 2 formulas must be incorporated plus terms to account for the second level of digit switching. The option 1 formulas are:

$$R_1 = 46 \; R_{EDC}^{45} \; Q_{EDC} \; R_S^{39} \; R_{dsc}^{4212} \; R_{dss}^{33696} \; R_{dl}^{33696}$$

$$R_2 = 39 \; R_{EDC}^{46} \; R_S^{38} \; Q_S \; R_{dsc}^{4101} \; R_{dss}^{32832} \; R_{dl}^{32832}$$

defining:

$$R_a = R_{dsc} \; R_{dss} \; R_{dl}$$

$$Q_a = 1 - R_a$$

$$R_b = R_{dl} \; R_{dss}$$

$$Q_b = 1 - R_b$$

then:

$$R = R_1 + R_2 + R_{EDC}^{46} \; R_S^{39} \left\{ R_{dsc}^{39} \left[R_a^{39} (R_b^{39} + 39R_b^{38} Q_b)^8 + 39R_a^{38} Q_a R_b^{304} \right]^8 \right.$$
$$\left. + 39R_{dsc}^{38} \; Q_{dsc} \; R_a^{304} R_b^{2432} \right\}^{12}$$

Evaluating the mission reliability for the three options yields values of:

Option 1

    R = .999058

Option 2

    R = .999880

Option 3

    R = .9999446

which results in equivalent p values of:

Option 1

    $p = 94227 \cdot 10^{-8}$

Option 2

    $p = 11951 \cdot 10^{-8}$

Option 3

    $p = 5543 \cdot 10^{-8}$

TOTAL SUBOPTION C AND D Digit Functions - The digit address decode
logic and digit logic level converter reliabilities must be joined
to the above figures in a series reliability functions to obtain
the complete digit functions for suboptions C and D. This results
in values for the three options of:

Option	p	R
1	$148311 \cdot 10^{-8}$	.99857
2	$35193 \cdot 10^{-8}$	.999648
3	$21185 \cdot 10^{-8}$	.999788

7. Word Line Switches - Each word line switch is connected to 16 word
lines. A failure in a word line switch will cause the loss of either
part or all of the 16 word lines which constitutes a memory failure.
Thus the word line switches act as a series reliability element.
Because of their close approximation with the word lines, the word lines
will be assumed part of the word line switches. The reliability and
p factor of each word line switch with its associate word lines is:

$$R = .9999501$$

$$p = 4991 \cdot 10^{-8}$$

The reliability values for all word line switches for each option is:

Option	p	R
1	$15332352 \cdot 10^{-8}$	.859
2	$2555392 \cdot 10^{-8}$	.9747
3	$1277696 \cdot 10^{-8}$	.9873

8. <u>Word Address Decode</u> - The word address decode logic acts as a series reliability function having mission reliability values for each option and suboption of:

Option	p	R
1x	$6630 \cdot 10^{-8}$	.9999337
2x	$1547 \cdot 10^{-8}$	.9999845
3x	$442 \cdot 10^{-8}$	.99999558
1y	$442 \cdot 10^{-8}$	.99999558
2y	$442 \cdot 10^{-8}$	.99999558
3y	$442 \cdot 10^{-8}$	.99999558

9. <u>Word Logic Level Converters</u> - The reliabilty values for each word logic level converter is

$$p = 1081 \cdot 10^{-8}$$

$$R = .9999892$$

The word logic level converters perform as a series reliability function having reliability mission values for each option of:

Option	p	R
1x	$484288 \cdot 10^{-8}$	.99516
2x	$207552 \cdot 10^{-8}$	.99792
3x	$138368 \cdot 10^{-8}$	.99862
1y	$138368 \cdot 10^{-8}$	.99862
2y	$138368 \cdot 10^{-8}$	.99862
3y	$138368 \cdot 10^{-8}$	.99862

10. <u>Word Oscillator</u> - Each word oscillator consists of a single oscillator circuit and one or more current drivers. The reliability values of the oscillator circuit is:

$$p = 1718 \cdot 10^{-8}$$

$$R = .9999828$$

and each current driver is:

$$p = 1374 \cdot 10^{-8}$$

$$R = .9999863$$

The series mission reliability values for each option is then:

Option	p	R
1x	$3092 \cdot 10^{-8}$	.9999691
2x	$3092 \cdot 10^{-8}$	.9999691
3x	$3092 \cdot 10^{-8}$	.9999691
1y	$18206 \cdot 10^{-8}$	.999818
2y	$4466 \cdot 10^{-8}$	.9999553
3y	$3092 \cdot 10^{-8}$	.9999691

The total mission reliability is then determined by combining the appropriate series functions for each option and suboption resulting in the module values given in figure 7.10.

Option	p	R
1Ax	.3592	.698
1Ay	.3559	.700
1Bx	.3655	.694
1By	.3622	.696
1Cx	.1600	.852
1Cy	.1567	.855
1Dx	.1600	.852
1Dy	.1567	.855
2Ax	.06041	.9414
2Ay	.05972	.9421
2Bx	.06144	.9404
2By	.60075	.9410
2Cx	.02832	.9721
2Cy	.02763	.9728
2Dx	.02832	.9721
2Dy	.02763	.9728
3Ax	.03147	.9689
3Ay	.03147	.9689
3Bx	.03202	.9684
3By	.03202	.9684
3Cx	.01470	.9854
3Cy	.01470	.9854
3Dx	.01470	.9854
3Dy	.01470	.9854

Figure 7.10   Comparison of Module Reliabilities

The reliability and p values for a 10^8 bit system are given in Figure 7.11

Option	p	R
1Ax	.359	.698
1Ay	.816	.700
1Bx	.809	.694
1By	.811	.696
1Cx	.160	.852
1Cy	.157	.855
1Dx	.166	.852
1Dy	.157	.855
2Ax	.362	.696
2Ay	.358	.699
2Bx	.369	.691
2By	.365	.694
2Cx	.170	.844
2Cy	.166	.847
2Dx	.170	.844
2Dy	.166	.847
3Ax	.378	.685
3Ay	.378	.685
3Bx	.384	.681
3By	.384	.681
3Cx	.176	.839
3Cy	.176	.839
3Dx	.176	.839
3Dy	.176	.839

Figure 7.11 Comparison of 10^8 bit System Reliabilities

7.4. Weight and Volume

In order to achieve accurate weight and volume estimates a layout of each circuit board and a mechanical design must be performed on each option. Producing designs of this detail is beyond the scope of this trade study. By basing estimates upon factors found in equipment presently being produced, weight and volume values can be obtained which will closely approximate the values achieved through detailed designs. The major assumptions made in estimating weight and volume are outlined below.

Printed Circuit Card Size - There are limitations on the size of a printed circuit card. If a printed circuit card is larger than 20 cm on a side flexure during vibration can result in adjacent cards touching with the possible result of electrical shorts. A connector must be mounted on one edge of the printed circuit card to provide means for connecting the card to an interconnect circuit board or to cabling. This connector extends the length of the printed circuit board by 2.5 cm in one direction. Thus the total printed circuit board area is 450 sq. cm of which 400 sq. cm is available for circuitry. The mounting distance between printed circuit cards is .6 cm resulting in the volume occupied by a single printed circuit board being 270 cu. cm. The 20 cm dimension is not critical and minor variations around this value will be used as dictated by the designs.

Component Areas - Each electrical component occupies an area of the
printed circuit board. An estimate of the areas required for the
different types of components is

transistor	1.5 sq. cm
resistor	1.4 sq. cm
diode	1.4 sq. cm
capacitor	1.4 sq. cm
integrated circuit	3 sq. cm
hybrid circuit	11.3 sq. cm

Weight - The density of packaged electronic systems never varies
significantly from 1 gram per cubic cm. This value will be used in
computing weight from estimated volume.

Packaging - The assembled electronics must be placed in a case. The
case will occupy approximately 1.2 cm. an all sides of the assembled
electronics.

Power Supplies - Comparing several power supply designs for avionics
systems shows an average power supply volume can be approximated by
applying a factor of 15 cu. cm per watt.

Using the above assumptions the volume and weight of each design option
will be estimated. In making these estimates the various major sections
of the memory will be considered separately. These major sections
are:

thin film arrays with word and digit switches

general electronics

power supply

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Figure 7.12 shows the physical layout which will be used in estimating module volume.

Thin Film Stack with Word and Digit Switches - The thin film stack area is dependent upon the suboption used. The dimensions for each suboption are:

Suboption	length	width
A	69.6 cm	78.2 cm
B	69.6 cm	40.8 cm
C	69.6 cm	95.5 cm
D	78.3 cm	95.5 cm

In constructing the memory these stacks are quartered and folded with a .6 cm separation.

After folding a width of .7 cm must be left around each side of the perimeter to allow for the word and digit line overlays to be looped from one folded level to the next without a crease. The folded dimensions for each suboption are thus:

Suboption	length	width	height
A	36.2 cm	40.6 cm	2.4 cm
B	36.2 cm	41.8 cm	2.4 cm
C	36.2 cm	49.2 cm	2.4 cm
D	40.6 cm	49.2 cm	2.4 cm

Electronics

Film Stack

Power Supply
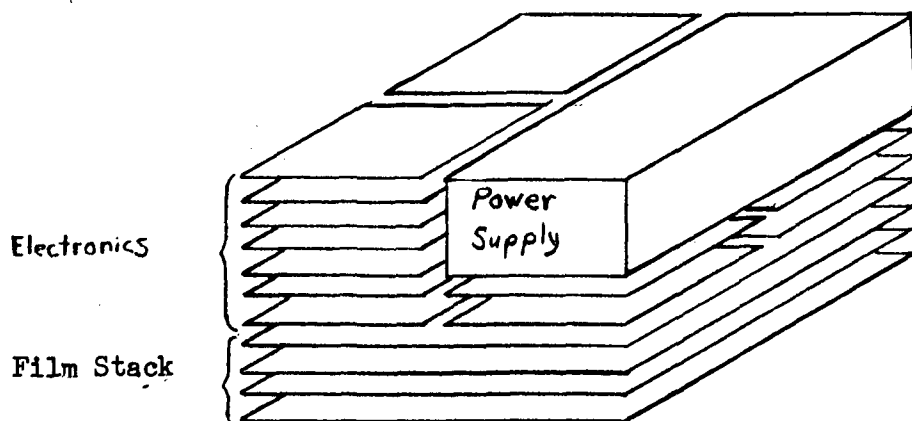
Figure 7.12   Physical Module Layout

The number of hybrid word switches required in each stack is 256.

These 256 word switches require a total circuit board area of 2893 sq. cm.

The word switches will be mounted on two printed circuit boards each having dimensions of 34.8 cm by 41.6 cm. Allowing for a bend radius on the word line overlay increases the dimension to 36.2 cm by 41.6 cm.

The number of hybrid digit switches is dependent upon the suboption and in the case of primary option 1, additional second level hybrid digit switches must be added. The number of hybrid digit switches and the required circuit board area is:

Option	number of switches	required area
1A	288	3255 sq. cm
1B	297	3356 sq. cm
1C and 1D	251	3966 sq. cm
2A and 3A	256	2893 sq. cm
2B and 3B	264	2983 sq. cm
2C,2D,3C, and 3D	312	3526 sq. cm

The maximum usable board area for digit switch circuit boards excluding a connector width along the board word direction for each suboption is:

Suboption	maximum board area
A	1321 sq. cm
B	1361 sq. cm
C	1610 sq. cm
D	1819 sq. cm

The number of boards required for each option and suboption is 2.5 except for options 2D and 3D where 2 boards are sufficient. Using a half board is allowable since the empty half board space can be used by the next array in the memory stack or by electronics circuit boards. The spacing between word and digit switch printer circuit boards is .6 cm. The total stack dimensions for each option and suboption is given below. These dimensions include the multiple arrays required in options 1 and 2. Those options marked with an asterisk (*) have a half board vacancy within the given dimensions.

Option	Length	width	height
1A	36.2 cm	41.6 cm	61.2 cm
1B	36.2 cm	41.8 cm	61.2 cm
1C	36.2 cm	49.2 cm	61.2 cm
1D	40.6 cm	49.2 cm	61.2 cm
2A	36.2 cm	41.6 cm	10.2 cm
2B	36.2 cm	41.8 cm	10.2 cm
2C	36.2 cm	49.2 cm	10.2 cm
2D	40.6 cm	49.2 cm	9.6 cm
3A*	36.2 cm	41.6 cm	5.4 cm
3B*	36.2 cm	41.8 cm	5.4 cm
3C*	36.2 cm	49.2 cm	5.4 cm
3D	40.6 cm	49.2 cm	4.8 cm

General Electronics - The array area is quartered

to allow four printed circuit boards to occupy each plane of the memory.

On one edge of each printed circuit board a connector of 2.5 cm
width must be allowed and a separation between adjacent board edges
of .6 cm is allowed. Using these values the available circuit board
area for each suboption is as given below

Suboption	usable area
A	341 sq. cm
B	343 sq. cm
C	409 sq. cm
D	460 sq. cm

Using the component area requirements given above in conjunction
with the parts count yields a total circuit board number
requirement as given below:

Option	Number of required circuit boards
1Ax	44
1Ay	25
1Bx	45
1By	25
1Cx	39
1Cy	23
1Dx	35
1Dy	21
2Ax	26
2Ay	22
2Bx	26
2By	22
2Cx	24
2Cy	21

Option (cont.)	Number of required circuit boards
2Dx	22
2Dy	19
3Ax	22
3Ay	22
3Bx	22
3By	22
3Cx	20
3Cy	20
3Dx	18
3Dy	18

The distance between boards is .6 cm. The arrangement of the boards is dependent upon the power supply size.

Power Supply - Using the figure of 15 cu. cm per watt for power supply volume gives the following total power supply volume requirements in cubic centimeters.

	A	B	C and D
1	4455	4575	5205
2	1590	1635	1875
3	1215	1260	1455

Suboption x

	A	B	C and D
1	3960	4080	4710
2	1455	1500	1749
3	1215	1560	1455

Suboption y

The power supply base area for each suboption is:

Suboption	Base area
A	740 sq. cm
B	744 sq. cm
C	875 sq. cm
D	984 sq. cm

Using this data the power supply volumes can be converted to the number of circuit board separations along its height. These values for each option are:

	A	B	C	D
1	10	11	10	9
2	4	4	4	4
3	3	3	3	3

Suboption x

	A	B	C	D
1	9	9	9	8
2	4	4	4	3
3	3	3	3	3

Suboption y

Using these values plus the number of circuit boards required for the electronics and a value of .6 cm separation distance between circuit boards results in the following values for the height of the power supply plus general electronics. For those options (i.e., 3A, 3B and 3C) which has remaining usable space in the array volume, this space has been filled before determining the electronics height.

	A	B	D	D
1	9.6 cm	10.2 cm	9.0 cm	8.4 cm
2	5.4 cm	5.4 cm	4.8 cm	4.8 cm
3	4.2 cm	4.2 cm	3.6 cm	3.6 cm

Suboption x

	A	B	C	D
1	6.6 cm	6.6 cm	6.6 cm	6.0 cm
2	4.8 cm	4.8 cm	4.8 cm	4.2 cm
3	4.2 cm	4.2 cm	3.6 cm	3.6 cm

Suboption y

Unpackaged Memory

The dimensions of the unpackaged memory for each suboption is then

Option	Length	Width	Height
1Ax	36.2 cm	41.6 cm	70.8 cm
1Ay	36.2 cm	41.6 cm	67.8 cm
1Bx	36.2 cm	41.8 cm	71.4 cm
1By	36.2 cm	41.8 cm	67.8 cm
1Cx	36.2 cm	49.2 cm	70.2 cm
1Cy	36.2 cm	49.2 cm	67.8 cm
1Dx	40,6 cm	49.2 cm	69.4 cm
1Dy	40.6 cm	49.2 cm	67.2 cm
2Ax	36.2 cm	41.6 cm	15.6 cm
2Ay	36.2 cm	41.6 cm	15.0 cm
2Bx	36.2 cm	41.8 cm	15.6 cm
2By	36.2 cm	41.8 cm	15.0 cm
2Cx	36.2 cm	49.2 cm	15.0 cm
2Cy	36.2 cm	49.2 cm	15.0 cm
2Dx	40,6 cm	49.2 cm	14.4 cm
2Dy	40.6 cm	49.2 cm	13.8 cm
3Ax	36.2 cm	41.6 cm	9.6 cm
3Ay	36.2 cm	41.6 cm	9.6 cm

Option	Length	Width	Height	(Cont.)
3Bx	36.2 cm	41.8 cm	9.6 cm	
3By	36.2 cm	41.8 cm	9.6 cm	
3Cx	36.2 cm	49.2 cm	9.0 cm	
3Cy	36.2 cm	49.2 cm	9.0 cm	
3Dx	40.6 cm	49.2 cm	8.4 cm	
3Dy	40.6 cm	49.2 cm	8.4 cm	

Packaging

The packaging adds 1.2 cm on each side, top and bottom of the unpackaged memory. The dimensions and volume of the packaged module is then:

Option	Length	Width	Height	Volume
1Ax	38.6 cm	44.0 cm	73.2 cm	124,323 cc (4.39 cu ft)
1Ay	38.6 cm	44.0 cm	70.2 cm	119,228 cc (4.21 cu ft)
1Bx	38.6 cm	44.2 cm	73.8 cm	125,912 cc (4.45 cu ft)
1By	38.6 cm	44.2 cm	70.2 cm	119,770 cc (4.23 cu ft)
1Cx	38.6 cm	53.6 cm	72.6 cm	150,206 cc (5.30 cu ft)
1Cy	38.6 cm	53.6 cm	70.2 cm	145,241 cc (5.14 cu ft)
1Dx	43.0 cm	53.6 cm	71.8 cm	165,485 cc (5.84 cu ft)
1Dy	43.0 cm	53.6 cm	69.6 cm	160,414 cc (5.66 cu ft)
2Ax	38.6 cm	44.0 cm	18.0 cm	30,571 cc (1.08 cu ft)
2Ay	38.6 cm	44.0 cm	17.4 cm	29,552 cc (1.04 cu ft)
2Bx	38.6 cm	44.2 cm	18.0 cm	30,710 cc (1.08 cu ft)
2By	38.6 cm	44.2 cm	17.4 cm	29,686 cc (1.05 cu ft)
2Cx	38.6 cm	53.6 cm	17.4 cm	36,000 cc (1.27 cu ft)
2Cy	38.6 cm	53.6 cm	17.4 cm	36,000 cc (1.27 cu ft)
2Dx	43.0 cm	53.6 cm	16.8 cm	38,821 cc (1.62 cu ft)

Option	Length	Width	Height	Volume (Cont.)
2Dy	43.0 cm	53.6 cm	16.2 cm	37.338 cc (1.32 cu ft)
3Ax	38.6 cm	44.0 cm	12.0 cm	20,381 cc (.72 cu ft)
3Ay	38.6 cm	44.0 cm	12.0 cm	20,381 cc (.72 cu ft)
3Bx	38.6 cm	44.2 cm	12.0 cm	20,473 cc (.72 cu ft)
3By	38.6 cm	44.2 cm	12.0 cm	20,473 cc (.72 cu ft)
3Cx	38.6 cm	53.6 cm	11.4 cm	23,586 cc (.83 cu ft)
3Cy	38.6 cm	53.6 cm	11.4 cm	23,586 cc (.83 cu ft)
3Dx	43.0 cm	53.6 cm	10.8 cm	24,892 cc (.88 cu ft)
3Dy	43.0 cm	53.6 cm	10.8 cm	24,896 cc (.88 cu ft)

Weight

Using a density of 1 gm per cc yields estimated module weights of

	1	2	3
A	124.3 kg (273 lbs)	30.6 kg (67 lbs)	20.4 kg (45 lbs)
B	125.9 kg (277 lbs)	30.7 kg (68 lbs)	20.5 kg (45 lbs)
C	150.2 kg (330 lbs)	36.0 kg (79 lbs)	23.6 kg (52 lbs)
D	165.5 kg (364 lbs)	38.8 kg (85 lbs)	24.9 kg (55 lbs)

Suboption x

A

	1	2	3
A	119.2 kg (262 lbs)	29.6 kg (65 lbs)	20.4 kg (45 lbs)
B	119.8 kg (264 lbs)	29.7 kg (65 lbs)	20.5 kg (45 lbs)
C	145.2 kg (319 lbs)	36.0 kg (79 lbs)	23.6 kg (52 lbs)
D	160.4 kg (353 lbs)	37.3 kg (82 lbs)	24.9 kg (55 lbs)

Suboption y

System Weight and Volume

Figure 7.13 shows the weight of the 10^8 bit memory system options and figure 7.14 their volume.

	1	2	3
A	124.3kg (273 lbs)	183.4kg (403 lbs)	244.6kg (538 lbs)
B	125.9kg (277 lbs)	184.3kg (405 lbs)	245.7kg (541 lbs)
C	150.2kg (330 lbs)	216.0kg (475 lbs)	283.0kg (623 lbs)
D	165.5kg (364 lbs)	232.9kg (512 lbs)	298.7kg (657 lbs)

Suboption x

	1	2	3
A	119.2kg (262 lbs)	177.3kg (390 lbs)	244.6kg (538 lbs)
B	119.8kg (264 lbs)	179.1kg (394 lbs)	245.7kg (541 lbs)
C	145.2kg (319 lbs)	216.0kg (475 lbs)	283.0kg (623 lbs)
D	160.4kg (353 lbs)	224.0kg (493 lbs)	298.7kg (657 lbs)

Suboption y

Figure 7.13 System Weight Comparisons

	1	2	3
A	124,232cc(4.38 cu ft)	183,426cc(6.84 cu ft)	244,572cc(8.64 cu ft)
B	125,912cc(4.45 cu ft)	184,260cc(6.51 cu ft)	245,676cc(8.68 cu ft)
C	150,206cc(5.30 cu ft)	216,000cc(7.63 cu ft)	283,032cc(10.00 cu ft)
D	165,485cc(5.84 cu ft)	232,926cc(8.23 cu ft)	298,704cc(10.55 cu ft)

Suboption x

	1	2	3
A	119,228cc(4.21 cu ft)	177,312cc(6.26 cu ft)	244,572cc(8.64 cu ft)
B	119,770cc(4.23 cu ft)	179,116cc(6.33 cu ft)	245,676cc(8.68 cu ft)
C	145,241cc(5.13 cu ft)	216,000cc(7.63 cu ft)	283,032cc(10.00 cu ft)
D	160,414cc(5.67 cu ft)	224,028cc(7.91 cu ft)	298,704cc(10.55 cu ft)

Suboption y

Figure 7.14 System Volume Comparisons

7.5 Maintenance

Maintenance can be divided into three phases, which are

1. Fault recognition and isolation

2. Line Replacable Unit (LRU) replacement

3. LRU repair

The relative merits of the various design options will be discussed with
relationship to these three maintenance phases. In each case an
LRU is defined as a single memory module.

Those options which contain parity or ECD have built-in capabilities
of detecting and isolating certain types of faults. In order to
determine the existance of multiple failures special tests must be
performed in which a series of test patterns are written into and
read from each memory location. The only notable difference between
options in the performance of these pattern tests affects the time
required to perform the tests. Those options employing multiple modules
to fulfill the 10^8 bit requirement can have each module tested simul-
taneously thus dividing the total testing time by the number of modules.
Assuming that the pattern test requires the reading and writing of
20 patterns in each memory word and that it takes 7.5 micro seconds for
the combined write/read memory cycle then the time required to perform
the pattern test for each option assuming simultaneous operation in
modular designs is:

Option	Test time
1	7.5 minutes
2	1.25 minutes
3	.625 minutes

Two primary factors contribute to a measurement of LRU replacement. These are the magnitude of the physical task of performing the replacement and the cost of maintaining a sufficient number of spares. Independent of the option, the replacement of an LRU requires that the unit must first be physically and electrically disconnected from the vehicle and then transported from its mounting position in the vehicle to a repair area. The reverse process must be performed on a functioning unit. The ease or difficulty with which this task is performed is dependent upon the weight of the LRU. If the weight of the LRU is less than 25 kilograms it can be fairly easily carried by one individual. Two men can fairly easily carry the unit if greater than 25 kilograms but less than 50 kilograms. If greater than 50 kilograms the unit must be lifted and transported by mechanical means. If the access to the LRU, as mounted in the vehicle, is constricted the limiting weights in the above ranges must be lowered. The weights of the various options show that option 1 configurations have modules weighing greater than 50 kilograms, option 2 modules weighing between 25 and 50 kilograms and option 3 modules weighing less than 25 kilograms. Thus option 3 is best and option 1 worst from the standpoint of replacement effort.

The cost of maintaining sufficient spares is dependent upon the cost per spare and the number of units which can be expected to be in the repair cycle at any one time. The number of units which can be expected to be in the repair cycle is dependent upon the total number of units in the field, the mean time between failure (MTBF) for each unit, and the mean time to repair (MTTR) for each unit. Expressed as a formula the total cost of spares is

$$\frac{MTTR}{MTBF} \cdot N \cdot C$$

where N is the number of modules in the field which must be operating and C is the cost per module. The MTBF value in the above formula differs from the MTBF value used in expressing mission reliability. MTBF for mission reliability is computed allowing certain types of failures to exist as long as correct data can be read from and written into the memory. For mission reliability computations incorporating redundancy, error detection and corrections functions in the memory enhance the reliability. In computing MTBF for use in determining the number of spares required, any detected failure requires repair, not just those failures which result in memory inoperation. Thus adding additional redundant electronics to enhance mission reliability reduces the MTBF value used in computing total cost of spares. The N·C factor in the above formula can be replaced by the number of 10^8 bit memories in the field times the cost per 10^8 bit memory. Since the number of 10^8 bit

memories in the field is independent of the option selected the above formula can be normalized by replacing N·C by the cost per 10^8 bit memory.

MTTR is one of the quantitative measurements resulting from an analysis of the third maintenance phase, LRU repair. The cost of effecting repairs is attributable to the labor cost, replacement parts costs and facilities costs. Facilities cost is independent of the option thus only the labor costs and replacement parts costs need be considered in order to compare the various options. The memories are composed of electronics and the thin film arrays overlayed with word and digit lines. The cost of repairing the electronics is independent of the selected option. Spare word lines are corporated in the suboption D designs for the purpose of easing the array repair task. There is no significant difference in repair costs or MTTR for the other options. The above discussion shows that there are numerous disimiliar requirements which must be considered in comparing the various options with relationship to maintenance. In an attempt to rate the options only the most significant parameters will be considered. The most significant parameters are the difficulties involved in replacing a failed unit on the vehicle due to the weight of the units and the repair costs. Assigning ratings of 1 through 6 to the various options with higher values indicating better maintainability performance yields the following for the various options.

Options	A	B	C	D
1	1	1	1	4
2	2	2	2	5
3	3	3	3	6

The suboptions of x and y exhibit no significant maintainability differences.

8.0 RECOMMENDED CEI DESIGN

8.1 Option Selection

The trade study parameters are presented in summary form in figure 8.1.
The values presented are for a 10^8 bit memory system, i.e., the data for
those options having modular construction is the total value for the number
of modules indicated as required to obtain 10^8 data bits. The option
exhibiting the best overall performance must be selected from the 24 options
presented.

First the separate word select and shared word select options will be
compared. Comparisons will be made only between identical modular con-
figurations and identical A, B, C and D suboptions. Thus the weight of the
basic memory plus parity 16 x 10^6 bit modular configuration with separate
word select (184kg) will only be compared with the weight of the basic memory
plus parity 16 x 10^6 bit modular configurations with shared word select (179kg)
etc. Making this comparison shows that the shared word select option is
better than or the same as the separate word select option in each instance.
Thus only the shared word select options will be considered.

The next step in selecting the best option will be to make a determination as
to whether parity, Error Correction/Detection and/or spare word lines are
desired. The major variation in the trade parameters occurs with the addition
of ECD. ECD was added to the memory in order to enhance the memory relia-
bility. The result is an increase in cost, power, weight and volume. The
percentage increases in these parameters over the basic memory values are:

Figure 8.1 Trade parameter summary for a 10^8 bit memory system.

	Module Capacity (bits)	Modules per 10^8 bits	Separate Word Select (X)				Shared Word Select (Y)			
			Basic Memory (A)	Plus Parity (B)	Plus ECD (C)	Plus Spares (D)	Basic Memory (A)	Plus Parity (B)	Plus ECD (C)	Plus Spares (D)
Cost (cents/bit)	10^8	1	.30	.31	.34	.36	.30	.30	.34	.36
	16×10^6	6	.22	.22	.25	.26	.21	.22	.24	.25
	8×10^6	12	.22	.22	.25	.26	.22	.22	.25	.26
Power (watts)	10^8	1	297	305	347	347	264	272	314	314
	16×10^6	6	106	109	125	125	97	100	116	116
	8×10^6	12	81	84	97	97	81	84	97	97
Reliability	10^8	1	.70	.69	.85	.85	.70	.70	.86	.86
	16×10^6	6	.70	.69	.84	.84	.70	.69	.85	.85
	8×10^6	12	.69	.68	.84	.84	.69	.68	.84	.84
Weight (Kg)	10^8	1	124	126	150	165	119	120	145	160
	16×10^6	6	183	184	216	233	177	179	216	224
	8×10^6	12	245	246	283	299	245	246	283	299
Volume (10^3 cc)	10^8	1	124	126	150	165	119	120	145	160
	16×10^6	6	183	184	216	233	177	179	216	224
	8×10^6	12	245	246	283	299	245	246	823	299
Maintenance (rated)	10^8	1	1	1	1	4	1	1	1	1
	16×10^6	6	2	2	2	5	2	2	2	5
	8×10^6	12	3	3	3	6	3	3	3	6

Cost	13% to 15%
Power	18% to 20%
Weight	11% to 23%
Volume	11% to 23%

These increases in cost, power, weight, and volume must be compared with the benefits in increased reliability. The reliability estimates for the defined space mission are inadequate for most space programs. As the oligatomic memory technology advances, significant improvements in reliability can be be expected through the increase in the capacity of a single memory plane and the mechanization of many of the discrete circuits into integrated circuits. Using the present technology status increased reliability can be achieved through redundancy. The following table demonstrates the reliabilities achieved with multiple redundancy for the various options with and without ECD.

Number of Redundant Units	Basic Memory			Memory with ECD		
	10^8 bit modules	16×10^6 bit modules	8×10^6 bit modules	10^8 bit modules	16×10^6 bit modules	8×10^6 bit modules
1	.700	.699	.685	.855	.847	.839
2	.910	.909	.901	.979	.977	.974
3	.973	.973	.969	.997	.996	.996
4	.992	.992	.990	.9996	.9995	.9993

Reliability can be best related to cost, weight, power and volume by assuming a desired mission reliability and comparing the cost, weight, power and volume

required to achieve the desired reliability through the use of redundancy.
Figure 8.2 makes this comparison for an assumed desired reliability of .99.
To achieve .99 mission reliability for the defined 201 hour space mission
requires quadruple redundancy if the basic memory units are used and triple
redundancy if ECD is added. The ECD mechanization exhibits better cost,
power, weight, and volume parameters by the following percentages.

Cost	16 - 18%
Power	28 - 30%
Weight	9 - 16%
Volume	9 - 16%

An option containing ECD will be selected.. The next question to be answered
is whether or not the option containing spare word lines should be selected.
The addition of spare word lines affects the trade parameters of cost, weight,
volume, and maintainability.   The affect upon cost is not necessarily as
indicated in figure 8.1, Spare word lines are added to the memory for the
purposes of increasing manufacturing yield and facilitating maintenance
of failed arrays. Since manufacturing yield is unknown the cost figures
shown   are based upon achieving no manufacturing cost advantage
from the employment of spare word lines.   The cost figures
indicate that the spare word lines increase memory cost by 4 to 5%. If
actual manufacturing yields exhibit a significant percentage of magnetic
substrates with a few local area faults, the cost of memories without spare
word lines can significantly increase. Thus the actual cost figures may

	Module Capacity (bits)	Basic Memory	Memory with EDC
Cost per redundant storage bit (cents)	10^8 16×10^6 8×10^6	1.18 .85 .88	1.0 .72 .75
Power (watts)	10^8 16×10^6 8×10^6	1056 388 324	816 300 252
Weight (Kg)	10^8 16×10^6 8×10^6	477 709 978	436 648 849
Volume (10^3cc)	10^8 16×10^6 8×10^6	477 709 978	436 648 849

Figure 8.2 Redundant mechanization parameters to
achieve .99 reliability.

show that the spare word line option has a very significant cost advantage

rather than the small cost disadvantage shown. Without spare word lines

maintenance costs and repair time are significantly increased for minor

substrate failures. Addition of spare word lines result in a 4 to 10%

weight and volume penalty. Since the oligatomic mass memory is an infant

technology, the inclusion of spare word lines offers insurance against cost

increases due to manufacturing and maintenance unknowns and thus should be

included.

Thus the spare word line option (D) and the shared word select (y) have

been selected, leaving a final selection to be made between the primary

option module size. In an avionics application electronic equip-

ment must be made to occupy volumes dictated by the placement of the vehicle

structures and skin. In most applications it would be difficult to obtain

a 160,000 CC volume with a predetermined form as would be required for the

10^8 bit option packaged in a single module. The two options having 10^8

bits configured from smaller modules will find wider application in meeting

available space constraints. The modular options are also more versatile

in their application to variations in capacity requirements. Memory capacities

can be achieved in 8×10^6 or 16×10^6 increments if the modular options are

selected. The 16×10^6 bit module is selected as a preferable because of the

trade parameters of cost, power, reliability, weight, volume and maintenance

8.2 Technology Improvements

The trade studies have considered state-of-the-art designs. Since

oligatomic memories are a new technology improvements in memory parameters

can be expected. Improvements in array bit density, operating margins and
electronic circuitry can be expected to offer significant improvements
in the memory specifications.Figure 8.3 shows the estimated memory para-
meters achievable with several variations in memory improvements. All of
the figures are based upon mechanizing a memory having $128 \times 10^6 (2^{27})$ bits
of data storage. A system of 128×10^6 bits is chosen because it is representable
as a power of 2, while 10^8 bits is not. The first column represents the
present "state-of-the-art" designs.   Three modular configurations
are shown with module sizes of 8×10^6 bits,32×10^6 bits,and 128×10^6 bits.
In each case extended Hamming code is employed, but no spare word lines are
used. The basic array size is 8×10^6 bits having 2808 digit lines, of which
2048 are data lines, 448 are used for Hamming code storage and 312 are used
as dummy reference lines, by 4096 word lines.

The second column represents the improvement achievable by doubling the
array bit density. Doubling the bit density is achieved by decreasing the
word and digit line spacings by a factor of .707. The number of bits in
the basic array is not changed and thus no changes are made in the memory
electronics. Percentage improvements achieved for each parameter(for the
128×10^6 bit module only)by doubling the density are:

Volume	21%
Power	0%
Weight	21%
Cost	6%
Reliability	0%

	Module Capacity (bits)	Modules per 2^{27} bits	Present Design	Double Density	Plus 40% Margins	Plus Minor Electronics	Plus Major Electronics	DD+ 180% Margins	Plus Minor Electronics	Plus Major Electronic
Volume (10^3 cc)	8×10^6	16	382	344	344	325	172	344	325	172
	32×10^6	4	225	187	139	129	81	139	129	81
	128×10^6	1	183	145	96	86	54	77	70	51
Power (watts)	8×10^6	16	97	97	97	93	57	97	93	57
	32×10^6	4	150	150	130	110	73	130	110	73
	128×10^6	1	370	370	230	170	120	170	140	96
Weight (Kg)	8×10^6	16	382	344	344	325	172	344	325	172
	32×10^6	4	225	187	139	129	81	139	129	81
	128×10^6	1	183	145	96	86	54	77	70	51
Cost (¢/bit)	8×10^6	16	.43	.40	.40	.34	.15	.40	.34	.15
	32×10^6	4	.34	.32	.17	.14	.07	.17	.14	.07
	128×10^6	1	.32	.30	.16	.13	.06	.10	.08	.04
Reliability (20/hr mission)	8×10^6	16	.79	.79	.79	.79	.98	.79	.79	.98
	32×10^6	4	.81	.81	.89	.89	.992	.89	.89	.992
	128×10^6	1	.81	.81	.90	.90	.995	.95	.95	.997

Figure 8.3 Estimated improvements in a 128×10^6 bit memory system with technology developments.

The third column represents an improvement in memory margins in addition to double density. Margins restrict the physical length of the word and digit lines. With double density the margins need be increased by a factor of 1.414 (approximately 40% increase) over their present capability to increase the basic array size to 5616 digit lines by 8192 word lines. Increasing the margins thus allows 32×10^6 data bits to be placed on a single array and thus reduces the electronics required in the larger module configurations. The 8×10^6 bit module is unaffected by increased margins. The percentage improvement over the double density improvements achieved by increasing margins by 40% for the 128×10^6 bit module is:

Volume	34%
Power	38%
Weight	34%
Cost	7%

Reliability improvement from .81 to 90

The next column shows the improvements obtainable through the minor electronic improvement of doubling the number of digit lines handled by a single hybrid circuit digit switch. The improved hybrid circuit design has been incorporated into the double density and improved margins configuration. The improvement is primarily a packaging improvement. The improvements in the 128×10^6 bit module are:

Volume   10%

Power   24%

Weight   10%

Cost   19%

Reliability   Insignificant

The next column shows the improvements achievable if all of the discrete

component circuits are replaced by special designed integrated circuits.

Cost values are based upon typical integrated circuit costs and not upon

special designs. The improvements achieved in the 128×10^6 bit module do to

integrated circuit implementation is

Volume   37%

Power   29%

Weight   37%

Cost   54%

Reliability improvement from .90 to .995

The remaining columns represent the improvements achievable by further

increases in margins. The margins have been increased to allow an array size

containing 11232 digit lines and 16384 word lines.

The above comparisons indicate that the most significant improvements are

achieved by improving margins and major electronic improvements. The major

electronics improvements are achievable through "state of the art" circuit

design funded for this purpose.

8.3   Extended Trade Parameters

During the trade study several paths of investigation were not pursued
because of anticipated minor significance in comparison to the variations
selected for study or because of the lack of specific requirements which
could be used in evaluating trade parameters. All configuration variations
which specifically affect memory speed were not investigated. The primary
factor governing speed is the word current frequency. With a 10 MHz word
current frequency the memory speed will be 2.5us to read and 5us to write.
The majority of the time required to read and write the memory is used in
providing the required number of word current cycles to perform the read or
write operation and to allow the digit and word switch switching transients
to decay. One method of achieving significant improvements in speed is to
raise the word current frequency. The present word current frequency of 10MHz
is selected because of frequency limitations of the FET switches used in the
memory circuits. To increase the word current frequency will require a change
in the switching device resulting in increased weight, power, cost and volume.
Since a specific application for the mass memory has not been specified the
requirements for increasing the speed above 2.5us read and 5us write do not
exist and thus to select a more costly and heavier design because of increased
speed capabilities is unwarranted.

Another method of increasing effective memory speed without a change in
switching devices is to increase the word length of the memory word. The
present design requires 2.5us to read and 5us to write a 32 bit data word.
If the number of data bits per memory word is doubled to 64, the effective
time required to read and write 32 bits would be 1.25us and 2.5us respectively.

A double word mechanization will increase the number of sense amplifiers from 39 to 72 and increase the complexity of the Hamming code and parity generation and testing circuitry. In order to obtain the increased speed, data must be written and read two words at a time.

The reliability estimates for the various configurations are less than is normally required for space or avionics applications. The reliability estimates are based upon the assumption that the loss of a single memory word results in the loss of the total mass memory system. For many applications the loss of a single word or even a small block of words can be bypassed by the computer system with little or no loss to the mission operation. The reliability analysis shows that the major source of failures is in the word lines and word switches. The failure of a single word line results in the loss of only 64 words of memory which is 1 part in 49152 of a 10^8 bit memory. A word switch has several failure modes resulting in the loss of different portions of memory varying from the loss of 64 words if a single FET switch fails open to the loss of 1/12 of the memory if a FET switch fails closed. For those applications where degraded operation in the event of failures is acceptable,the oligatomic mass memory has inherent characteristics making degraded operation achievable.

To conserve power it has been assumed that only the module being used will be turned on at any one time and when not in use, the power (to all memory modules)will be turned off. If the conservation of power is of major

consideration, the removal of power from all elements not under immediate usage can be extended to the memory internal circuitry. Major elements which are candidates for this approach are the sense amplifiers used only during read and the digit drivers used only during write operations. The $16x10^6$ bit memory module has two $8x10^6$ arrays driven in the word direction by a single oscillator and two current drivers. By adding another oscillator and driving each current driver from a separate oscillator,only one of the arrays need be supplied with word current at any one time,thus allowing power to be removed from one of the oscillators and word current drivers. Power switching has the disadvantage of requiring extra electronics to perform the switching and reduces memory speed. Each time power must be switched onto a needed circuit element approximately 10us is lost in awaiting power transients to decay.

In order to insure that proper addressing is occurring during the memory operation, a feature called virtual address encoding can be incorporated in the memory. Virtual address encoding requires a change in the Hamming code generation and testing logic. In generating the Hamming code, the data bits and address bits are combined. For a 10^8 bit memory of 32 bit words the address is 22 bits in length. The combined address and data word are thus 54 bits in length. An Extended Hamming code is generated for the total 54 bits. For 54 bits the Extended Hamming code requires 7 bits (which is the same length required by 32 bits). The 32 data bits plus 7 Extended Hamming code bits are then stored. Upon reading the memory the address register is combined with the read data bits in generating the testing

syndrome. If an error is indicated in the address bits it is known that an addressing error has occurred in the memory. It is not known if the error occurred during read or write. Note that the stored word length remains at 39 bits and that the actual address bits are not stored.

8. CEI Selection

The trade studies have been performed in parallel with the development
of a feasibility unit design. During the feasibility unit development two
significant advancements in stack mechanization have been identified.
These are an increase in maximum array size from 2808 digit lines by 4608
word lines to 2808 digit lines by 8272 word lines and a repackaging of the
hybrid digit switch. The repackaged hybrid circuit switch contains the
circuitry required by 16 digit data lines and 2 digit dummy lines. The
repackaged switch is approximately 30% larger than the previous design
while containing twice the circuitry resulting in an overall circuit area
reduction of 70%.

The configuration selected for detailed description in the CEI specification
is a modular design with the following characteristic

STACK
16,777,216 data bits
2808 digit lines
8272 word lines
.015 cm word line spacing
.031 cm digit line spacing

MODULE
2 stacks
33,554,432 data bits

FEATURES
Shared word select
32 bit data word
Extended Hamming Code
Virtual Address encoding
2.5 us read
5 us write

9.0 DEFINITIONS

Several terms have been used in this report which may require special
definitions:

ATR Case   - Standardized Air Transport Rack sized per ARINC 404.

Cycle Time - The time required between references to a memory module, due
to internal timing requirements.

FOFOFS   - Fail Operate, Fail Operate, Fail Safe. The ability of a system
to absorb two sequential component failures with no loss in
functional capability, and a third failure without causing a
mission failure.

LRU   - Line Replaceable Unit. The level of spare part available for
immediate replacement of a failed unit within the system.

LSI   - Large Scale Integration. A trend toward providing greater funct-
tional capability within one circuit device. System reliability
is increased through the reduced interconnection count obtained.

Multiple Redundant Mode -
The replication of components with similar functions, in order
to implement failure tolerant capabilities within a system.

Nominal (power) -
Power required based on normal environmental use of a memory
without failures operating at a frequency limited by the cycle
time.

NDRO   - Non-Destructive Readout. The capability of a storage element to
be sensed for its contents without removing the contents from
the element.

Non-Redundant Mode -
The operating mode which meets functional requirements, but
without redundancy allowing for potential failures.

Non-Volatile -
The ability of a storage media to maintain its contents without
applied power.

Oligatomic - "A few atoms" thick.   A characteristic description of the
          Univac thin film mass magnetic memory technology, which has a
          100 angstrom film thickness.

Random Access -
          The ability to access any word in memory on the next cycle time
          independent of the previous accessed word. (not true in sequential
          memories)

SEC/DED   - An on-line fault tolerant capability of Single Error Correction/
          Double Error Detection.

APPENDIX A

PX 6411-8 Program Plan -
Engineering Development Model,
Oligatomic Mass Memory Module

PRELIMINARY ISSUE

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PROGRAM PLAN - ENGINEERING DEVELOPMENT MODEL OLIGATOMIC MASS MEMORY MODULE

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August 1971

PREPARED FOR

NASA
GC Marshall Space Flight Center
Huntsville, Alabama

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PRELIMINARY ISSUE

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1. DOCUMENT NO.	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.
PX 6411-8		

4. TITLE AND SUBTITLE	5. REPORT DATE
PROGRAM PLAN - ENGINEERING DEVELOPMENT MODEL OLIGATOMIC MASS MEMORY MODULE PLAN	August 1971
	6. PERFORMING ORGANIZATION CODE: 6250

7. AUTHOR (S)	8. PERFORMING ORGANIZATION REPORT NO.
A. L. Recksiedler	

9. PERFORMING ORGANIZATION NAME AND ADDRESS	10. WORK UNIT NO.
Advanced Systems Requirements Department Defense Systems Division Univac Division of Sperry Rand Corporation St. Paul, Minnesota 55165	11. CONTRACT OR GRANT NO. NAS8-26670
	13. TYPE OF REPORT AND PERIOD COVERED

12. SPONSORING AGENCY NAME AND ADDRESS	
NASA GC Marshall Space Flight Center Huntsville, Alabama	Plan
	14. SPONSORING AGENCY CODE

15. SUPPLEMENTARY NOTES

Approved: *K. M. Hoglund*
K. M. Hoglund

16. ABSTRACT

A three phased plan is described to provide NASA with an Engineering Development Model of an Oligatomic Mass Memory Module in 18 months. Designed for spaceborne applications with a capacity of 33.5×10^6 bits, three modules provide a 10^8 bit memory capability.

17. KEY WORDS	18. DISTRIBUTION STATEMENT
Film Memories Mirror Memories Oligatomic Memories Space Shuttle Mass Memory	

19. SECURITY CLASSIF.(OF THIS REPORT)	20. SECURITY CLASSIF. (OF THIS PAGE)	21. NO. OF PAGES	22. PRICE
Unclassified	Unclassified		

UDI-2536-2 (REV. 5/69)

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DOCUMENT NO.
PX 6411-8

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1.0 INTRODUCTION

This program plan provides a three phased effort which provices NASA with a 33.5×10^6 bit oligatomic memory module suitable for spaceborne applications. Modules may be assembled into memory systems requiring 10^8 bits capacity.

The module delivered will be an Engineering Development Model. The Engineering Development Model is equivalent in form, fit and function to a production Contract End Item (CEI) prime equipment per NASA NPC 500-1. The CEI Specification Part I was developed on NASA Contract NAS8-26670. Part II, including detailed design, is to be accomplished within this plan.

The three phases included in this plan are summarized as follows:

    Phase I   Laboratory Breadboard
    Phase II   Engineering Development Model
    Phase III   Design Verification

Phase	Time Required	Summary	Engineering Requirements (mm)	Other Direct Costs
I	10 months	Build Breadboard Design for Environment Mil Spec Circuit Design Develop Test Plan Specify Software Determine MTBF Breadboard Tester	146	$ 66,500
II	6 months (can overlap phase I by 1 month)	Design Eng Dev Mod Build Eng Dev Mod Electronics Tester Memory Exerciser Diagnostic Software	387	$265,000
III	3 months	Perform Environmental Tests Final Report	44	$ 20,000

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2.0 PHASED DEVELOPMENT

This plan allows a development of the mass memory in three identifiable phases, leading to a deliverable Engineering Development Model.

The first phase develops a laboratory breadboard model utilizing the oligatomic memory technology. The laboratory breadboard efforts include utilizing the circuitry and array designs from the feasibility model developed on NASA contract NAS8-26670. This development investigates the mil-spec criteria as applied to the feasibility model designs. The laboratory breadboard thus addresses mil-spec design problems for an advanced memory technology.

The second phase is the design and build of an Engineering Development Model of the oligatomic memory module. This model is built to the CEI specified design, with an interface suitable for computer evaluation and diagnostics as well as a serial data bus. This model is then equivalent to the final configuration in form, fit and function. The quality assurance program of the CEI is investigated in this phase.

The third phase utilizes the Engineering Development Model in a series of environmental tests which verify the memory design.

A one month schedule overlap is possible between the first two phases. Otherwise the phases are independent developments.

The definition of the engineering development unit is given in the Preliminary CEI Part I Specification, PX-5714, "Performance/Design and Product Configuration Requirements, Oligatomic Mass Memory for Aeronautics and Space Applications". These requirements are summarized as follows:

Capacity; Module: 33.5×10^6 data bits
Speed: 2.5 microsecond cycle time read
5.0 micorsecond cycle time write

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Weight:	100 lbs.
Power:	113 watts
Volume:	1.6 cu. ft.
Word Length:	39 bits
	32 bit data word
	6 bit Hamming code
	1 bit parity
Access:	Random access to the word
Interface:	a) Bit Serial for data bus
	b) Word Parallel for computer application

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3.0 PHASE I, LABORATORY BREADBOARD

3.1 <u>System Engineering Tasks</u> - The system engineering tasks in the first development phase consist of

- Control Project
- Study Applications
- Develop Specifications
- Develop Reliability Plan

Work performed under each task is described below.

Task 1 - Control Project
- Communicate with all participating groups
- Maintain report inputs
- Maintain schedules
- Disseminate customer directives
- Generate monthly status reports
- Maintain periodic customer contact

Task 2 - Study Applications

- Review existing NASA documentation on potential activity
  - Aeronautic missions
  - Orbital missions
  - Planetary landings
  - Deep Space missions

- Evaluate mass memory requirements per mission
- Recommend specific mission oriented configurations.

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Task 3 - Develop Specifications

- Maintain functional specification on laboratory breadboard
- Develop specification for associated diagnostic software
- Develop test plan for next phases including:

    . Component test requirements

    . Film and array test requirements

    . Card and circuit test requirements

    . Module test requirements

    . Exerciser test requirements

- Develop tester specifications
- Revise CEI Specification

    . Additions to Part I

    . Incorporate Part II

- Develop specifications for Engineering Development Model

Task 4 - Develop Reliability Plan

- Calculate MTBF
- Develop Error Detection and Correction Algorithm
- Recommend partitioning of Engineering Development Model
- Determine available degraded modes.

3.2 <u>Engineering Design Tasks</u> - The   engineering design tasks in the first development phase consist of:

    . Develop Circuits

    . Develop Central Stack

    . Assemble and Evaluate Breadboard.

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These tasks lend to the operation of a laboratory breadboard model of an oligatomic memory which includes the environmental considerations. Work performed under each task is described below.

Task 5 - Develop Circuits

- Evaluate vendor components
- Design Mil Spec circuits
- Analyze circuit models
- Design logic of laboratory breadboard
- Fabricate circuits
- Assemble circuits
- Test circuits
- Fabricate breadboard
- Assemble breadboard
- Test breadboard

Task 6 - Develop Central Stack

- Develop test packets
- Provide layout drawings
- Fabricate Central Stack
- Assemble Central Stack
- Test Central Stack

Task 7 - Assemble and Evaluate Breadboard

- Assemble Stack to Breadboard
- Test Connections
- Verify operation with power on
- Generate plots of drive current variation.

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4.0 PHASE II, ENGINEERING DEVELOPMENT MODEL

4.1 <u>System Engineering Tasks</u> - The system engineering tasks in the second development phase consist of:

- Control Project
- Develop Specifications
- Develop Quality Assurance Plan

Work performed within each task is described below.

Task 8 - **Control** Project
- Communicate with all participating groups
- Maintain report inputs
- Maintain schedules
- Disseminate customer directives
- Generate monthly status reports
- Maintain periodic customer contact.

Task 9 - Develop Specifications
- Maintain specifications developed on first phase

- Develop environmental test plan
- Develop acceptance specifications, Engineering Development Model.

Task 10 - Develop Quality Assurance Plan
- Determine vendor quality capability
- Determine incoming inspection requirements
- Determine Lot Identity Requirements
- Determine Traceability Requirements
- Determine Clean Room Requirements
- Determine Packaging and Handling Requirements
- Determine Equipment Calibration Requirements.

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4.2 <u>Memory Stack Development Tasks</u> - The memory stack development tasks are performed simultaneously with the circuitry and packaging tasks, so that a completed module can be assembled as the developments are integrated. These tasks consist of:

- Design Stack
- Develop Tester
- Fabricate Stacks
- Assemble and Test Stacks

Work performed within each task is described below:

Task 11 - Design Stack
- Design Hybrid Electronics
- Design Centerboards and Overlays
- Develop Fabrication Procedures
- Develop Fabrication Fixtures.

Task 12 - Develop Tester

- Specify circuit tolerances
- Design and fabricate test fixtures
- Write automated test procedures.

Task 13 - Fabricate Stacks

- Fabricate electronic packages
- Assemble and test electronics
- Fabricate and test central stacks
- Test sample arrays
- Fabricate arrays.

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Task 14 - Assemble and Test Stacks

- Assemble electronics and central stacks
- Perform operational tests.

4.3 <u>Circuitry and Packaging Tasks</u> - The circuitry and packaging tasks are performed to develop the logic and stack environment of the Engineering Development Model. These tasks include incorporating the developed stacks into the final assembly (memory module). These tasks consist of:

- Design module
- Design and build card tester
- Fabricate module
- Design and build exerciser
- Assemble and test module
- Evaluate and accept module

Work performed within each task is described below:

Task 15 - Design module

- Define logic requirements
- Design circuits external to stack
- Design logic
- Design mechanical assemblies
- Design thermal system
- Design power system
- Design electrical system
- Design and map pc card set

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Task 16 - Design and Build Card Tester

- Specify tester and adapter capability
- Design tester, mechanical
- Design tester, electrical
- Build tester
- Checkout and debug tester
- Provide tester documentation

Task 17 - Fabricate module

- Purchase components
- Build Major subassemblies
- Build printed circuit cards
- Wire subassemblies

Task 18 - Design and Build Exerciser

- Define exerciser capability
- Design interfaces
- Build exerciser
- Checkout and debug exerciser

Task 19 - Assemble and Test Module

- Assemble subassemblies
- Perform power on checkout
- Checkout all stacks

Task 20 - Evaluate and accept module

- Evaluate of nominal voltages
- Establish drive current variation limits
- Perform acceptance tests
- Deliver module.

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4.4 <u>Develop Diagnostic Software</u> - The software is developed to provide a
factory acceptance test and a user confidence test. The diagnostics provide
software fault isolation, partitioning, and reconfiguration ability for
a using system. The software development has two tasks:

- Develop Factory Acceptance (FACT) Software
- Develop Diagnostic Program

Work involved in each task is described below:

Task 21 - Develop Factory Acceptance Software

- Analyze design data
- Specify functional tests
- Write flowcharts
- Code program
- Compile and debug program
- Document program
- Accept program

Task 22 - Develop Diagnostic Program

- Define isolation procedures
- Specify fault printouts
- Write flow charts
- Code program
- Compile and debug program
- Formalize documentation
- Accept program

5.0 PHASE III, DESIGN VERIFICATION

5.1 <u>System Engineering Tasks</u> - The system engineering task in the verification phase consists of:

- Control Project
- Write Final Report.

The work performed within each task is described below.

Task 23 - Control Project

- Communicate with all participating groups
- Maintain report inputs
- Maintain schedules
- Disseminate customer directives
- Maintain monthly status reports
- Maintain periodic customer contact.

Task 24 - Write Final Report

- Collect existing documentation
- Index and summarize
- Write report - with conclusions and recommendations.

5.2 <u>Environmental Tests</u> - These tests are performed on the memory module to verify meeting the design requirements. These tasks consist of:

- Scheduling tests and facilities
- Perform and evaluate tests
- Document test results.

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Work performed within each task is described below.

Task 25 - Scheduling Tests and facilities

Task 26 - Perform and evaluate tests

- Perform temperature/altitude test
- Perform vibration test
- Perform shock test
- Perform humidity cycle tests
- Perform EMI tests
- Perform radiation tests.

Task 27 - Document test results

- Collect test evaluations
- Summarize conclusions
- Write summary test report

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APPENDIX B

PX 5714 Preliminary
Contract End Item Detail
Specification, Performance
Design and Product Configuration
Requirements, Oligatomic
Mass Memory for Aeronautics
And Space Application.

PRELIMINARY

CONTRACT END ITEM DETAIL SPECIFICATION

- PRIME EQUIPMENT -

PERFORMANCE/DESIGN

AND

PRODUCT CONFIGURATION

REQUIREMENTS

OLIGATOMIC MASS MEMORY

FOR

AERONAUTICS & SPACE APPLICATIONS

Approved by _____   Approved by _____
          UNIVAC   NASA

Approval Date _____   Approval Date _____

Contract Number NAS 8-26670

Release Date:

1. SCOPE

This Part I Contract End Item (CEI) specification establishes the requirements for performance, design, test and qualification of an advanced memory device identified as Oligatomic Mass Memory CEI number PX-5714. This CEI depicts capabilities that will be required for future NASA Aeronautics and Space Applications.

2. APPLICABLE DOCUMENTS

The following documents, of exact issue shown, form a part of this specification to the extent specified herein. In the event of conflict between documents referenced herein and other detail content of Sections 3, 4, 5, and 10, the detail requirements of sections 3, 4, 5 and 10 shall be considered a superseding requirement.

PROJECT DOCUMENTS

TBD

SPECIFICATIONS

TBD

STANDARDS

TBD

DRAWINGS

TBD

BULLETINS

TBD

OTHER PUBLICATIONS

TBD

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Release Date:

3. REQUIREMENTS

3.1 Performance

The oligatomic mass memory will be designed to operate in an aeronautics/space environment. It will be capable of accepting and providing data in either a serial or a parallel mode of operation.

This CEI specification describes a single oligatomic mass memory module. This module may also be utilized in multiple-module configurations. These configurations shall include the three-module configuration that will exhibit a total capacity of 10^8 bits.

3.1.1 Functional Characteristics

3.1.1.1 Primary Performance Characteristics

3.1.1.1.1 Memory Capacity

The oligatomic memory shall have a total capacity of approximately 46,258,992 bits. This capacity shall include approximately 33,554,432 (2^{25}) data bits, 7,340,032 associated extended Hamming code bits, 224,640 spare bits, and 5,139,888 dummy bits.

3.1.1.1.2 Addressable Word Length

The 33,554,432 memory data bits shall be divided into 1,048,576 (2^{20}) 32-bit data words. Each data word shall be directly addressable.

3.1.1.1.3 Extended Word Length

In addition to the 32 data bits, each word shall contain an extended Hamming Code consisting of 6 error correction/selection bits and 1 parity bit.

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3.1.1.1.4 DRO/NDRO Characteristic

The oligatomic mass memory will operate as an NDRO memory device; ie, a read oper-
ation will not change the state of the associated magnetic vectors.

3.1.1.1.5 Access Time

The memory access time for the oligmatic mass memory shall not exceeed TBD nano-
seconds.

3.1.1.1.6 Memory Cycle & Read/Write Times

The oligatomic mass memory will have a basic memory cycle time of 2.5 μsec. The
read operation will be accomplished during a single memory cycle time. The write
operation will require two memory cycle times.

3.1.1.1.7 Random Addressability

The oligatomic mass memory shall have the capability to randomly address each of
the 1,043,576 (2^{20}) 32-bit data words.

3.1.1.1.8 Volatility

The oligatomic mass memory shall provide a non-volatile storage medium. A power
sensing/switching capability shall also be provided to assure a non-volatile operation
during power-off and power-transient conditions.

3.1.1.1.9 Interface

The interface electronics associated with the oligatomic mass memory shall be capable
of receiving data on either a serial or a parallel mode of operation. Priority logic
will be utilized as required to resolve conflicting requests.

Release Date:

The memory serial channel signal lines shall provide clock signals, synchronization, mode control, addresses, and data as required. The channel shall exhibit a minimum pulse repetition rate of 1.1 MHz. Logic levels shall range between +2 & +5 volts for a binary "1" and +1 & -2 volts for a binary "0", or other suitable levels determined by application or peripheral equipment.

The memory parallel channel signal lines shall provide mode control, addresses, and data as required. The channel shall exhibit a maximum transfer rate of 200 KHz. Logic levels shall range between +2 & +5 volts for a binary "1" and +1 $ -2 volts for a binary "0", or other suitable levels determined by application or peripheral equipment.

3.1.1.2 Secondary Performance Requirements

3.1.1.2.1 Power Transient Protection

Power transient protection will be provided within the oligatomic mass memory of automatically sequencing the memory off upon detection of a lower limit primary supply voltage. This sequencing action will be accomplished immediately after completion of the memory cycle that is in process when the detection occurs.

3.1.1.2.2 Self Checking Features

The oligatomic mass memory will utilize self-checking schemes to assure that the program being executed is error free. These schemes shall include: Hamming Code utilization over data and address fields and parity bit summation checks.

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3.1.1.2.3 Degraded Modes

The oligatomic mass memory shall be capable of a degraded mode of operation when installed within an operating system. In the single-module configuration, this capability can be achieved through utilization of adaptive software to bypass the portion of the memory found to be defective as a result of a self-test or diagnostic routine. In the multiple-module configurations, module switching schemes controlled by external logic may also be utilized.

3.1.2 Operability

3.1.2.1 Reliability

3.1.2.1.1 MTBF

The calculated MTBF associated with the oligatomic mass memory shall be in excess of TBD hours.

3.1.2.2 Maintainability

3.1.2.2.1 Maintainability Features

The oligatomic mass memory shall be designed to facilitate a high level of maintainability. This level of maintainability will be achieved through use of an optimum combination of fault recognition/isolation techniques and modular hardware replacement procedures.

3.1.2.2.2 MTTR

The MTTR of the oligatomic mass memory after fault detection/isolation shall not exceed TBD minutes.

Release Date:

3.1.2.2.3 Maintenance/Repair Cycles

TBD

3.1.2.3 Useful Life

3.1.2.3.1 Shelf Life

The Oligatomic Mass Memory shall be designed with a shelf life in excess of 10 years.

3.1.2.3.2 Operating Life

The oligatomic Mass Memory shall be designed with an operating life in excess of 10 years when repair activities are authorized. When repair activities are not authorized, the Oligatomic Mass Memory shall be designed to operate in a full or degraded mode for a minimum of TBD years.

3.1.2.4 Natural Environment

The Oligatomic Mass Memory shall be designed to operate within an environment consistent with typical aeronautics and space requirements. Launch and mission environmental requirements shall be as indicated in Tables 1 & 2, respectively.

3.1.2.5 Transportability

3.1.2.5.1 Design Considerations

The oligatomic mass memory shall be designed to facilitate ease of packaging for shipment.

3.1.2.5.2 Packaging Requirements for Shipment

TBD.

Release Date:

Vibration Levels:

Sinusoidal

5 to 33 Hz at 0.36 cm DA[+] displacement

33 to 140 Hz at 8g peak

140 to 240 Hz at 0.0204 cm DA displacement

240 to 2000 Hz at 24g peak

Random

20 to 200 Hz at 2dB per octave

200 to 700 Hz at $0.64g^2 \text{ Hz}^{-1}$

700 to 890 Hz at -18 dB per octave

890 to 2000 Hz at $0.15g^2 \text{ Hz}^{-1}$

Overall sound pressure level: 153.5 dB

Temperature in boost flight: $21 \pm 5.5^{\circ}\text{C}$

Acceleration maximum: first cutoff* 6.99 ms^{-2}

second cutoff** 15.24 ms^{-2}

Altitude maximum: 287 km

+ Double amplitude
* Launch into Earth orbit
** Injection into Earth-escape path

Table 1. Typical Payload Launch Environment

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Release Date:

Primary Radiation Belts

Inner Zone (~1000 to ~8000 km)

Composition: mainly electrons and protons
($\lesssim 10^{10}$ particles cm^{-2} s^{-1} ster^{-1}, $\lesssim$ 40 MeV)

Slight variations with solar activity.

Outer Zone (~13000 to ~80000 km)

Composition: mainly electrons and protons
($\lesssim 5 \times 10^{8}$ particles cm^{-2} s^{-1} ster^{-1}, $\lesssim$ 5 MeV)

Extreme variation with solar activity.

Solar High Energy Particle Radiation

Composition: protons with 1-2% alpha particles

Once every few years (~4.5 years) an extremely
high energy (~15 GeV) flux occurs.

Galactic Cosmic Radiation

Isotropic distribution of particles with intensity
variations during the solar cycle. High energies
($\lesssim$ 20 GeV) and about 2.5 particles cm^{-2} s^{-1}

Solar Wind Particles

Small numbers ($\lesssim 10^{4}$ cm^{-3}) of low energy ($\lesssim$ 40 keV)
electrons and protons.

Solar X-Radiation

$\lesssim$ 1 μW cm^{-2} of soft x-rays during periods of solar
activity.

Table 2. Typical Payload Mission Environment

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SPECIFICATION SYMBOL
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3.1.2.6 Human Performance

Not Applicable

3.1.2.7 Safety

3.1.2.7.1 Personnel

The oligatomic mass memory shall be designed to minimize any danger to operating or maintenance personnel. Techniques utilized shall include: bevelled edges, power-off interlocks; hazard signs, etc.

3.1.2.7.2 Equipment

The oligatomic mass memory shall be designed such that it will accommodate power transients without any detrimental effect to the equipment. In addition, it shall have the capability to sense any temperature in excess of (TBD) and to condition the input power as required.

3.1.2.8 Induced Environment

Not Applicable.

3.2 CEI Definition

3.2.1 Interface Requirements

3.2.1.1 Schematic Arrangement

The interface for the Oligatomic Mass Memory shall be designed consistent with the functional requirements associated with a specific application. Candidate applications include: 1) utilization as a main memory, and 2) utilization as a peripheral device with a parallel interface, and 3) utilization as a peripheral device with a serial interface. These candidate applications would result in typical interface signal requirements as shown in Figures 1, 2 & 3.

Release Date:


```
Memory
Module
```

- 32 Address/Data Lines
- Memory Request
- Requester Hold
- Data Ready
- Read Command
- Write Command
- Master Clear
- Stop
- Power Indicator
- Low Overtemp. Indicator
- High Overtemp
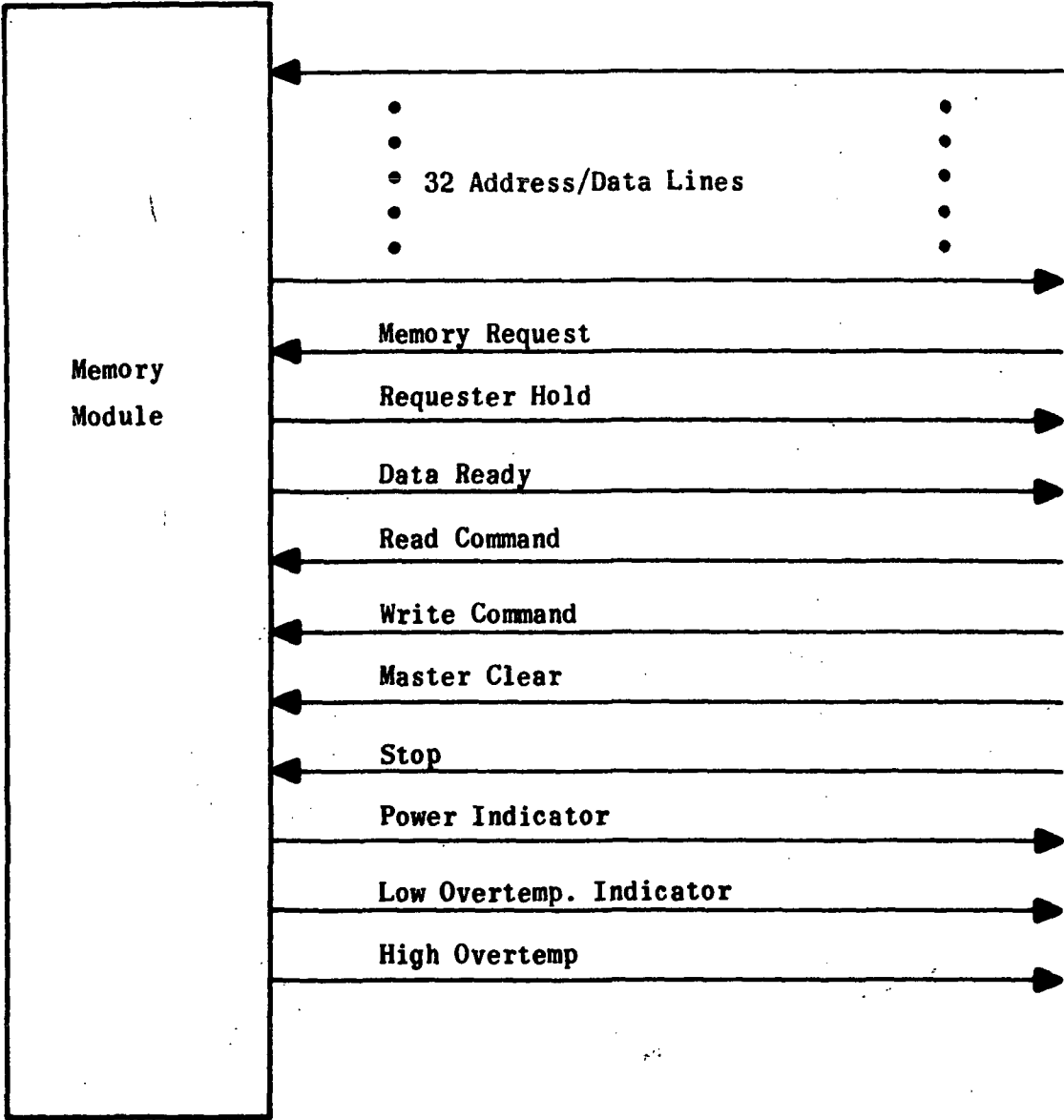
Figure 1. Typical Memory Module Interface
- Main Memory Application -

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Release Date:

Computer   Peripheral

External Function Request

External Function Acknowledge

Output
Channel

Input
Channel

Output Data Request

Output Data Acknowledge

Output
Data
Lines
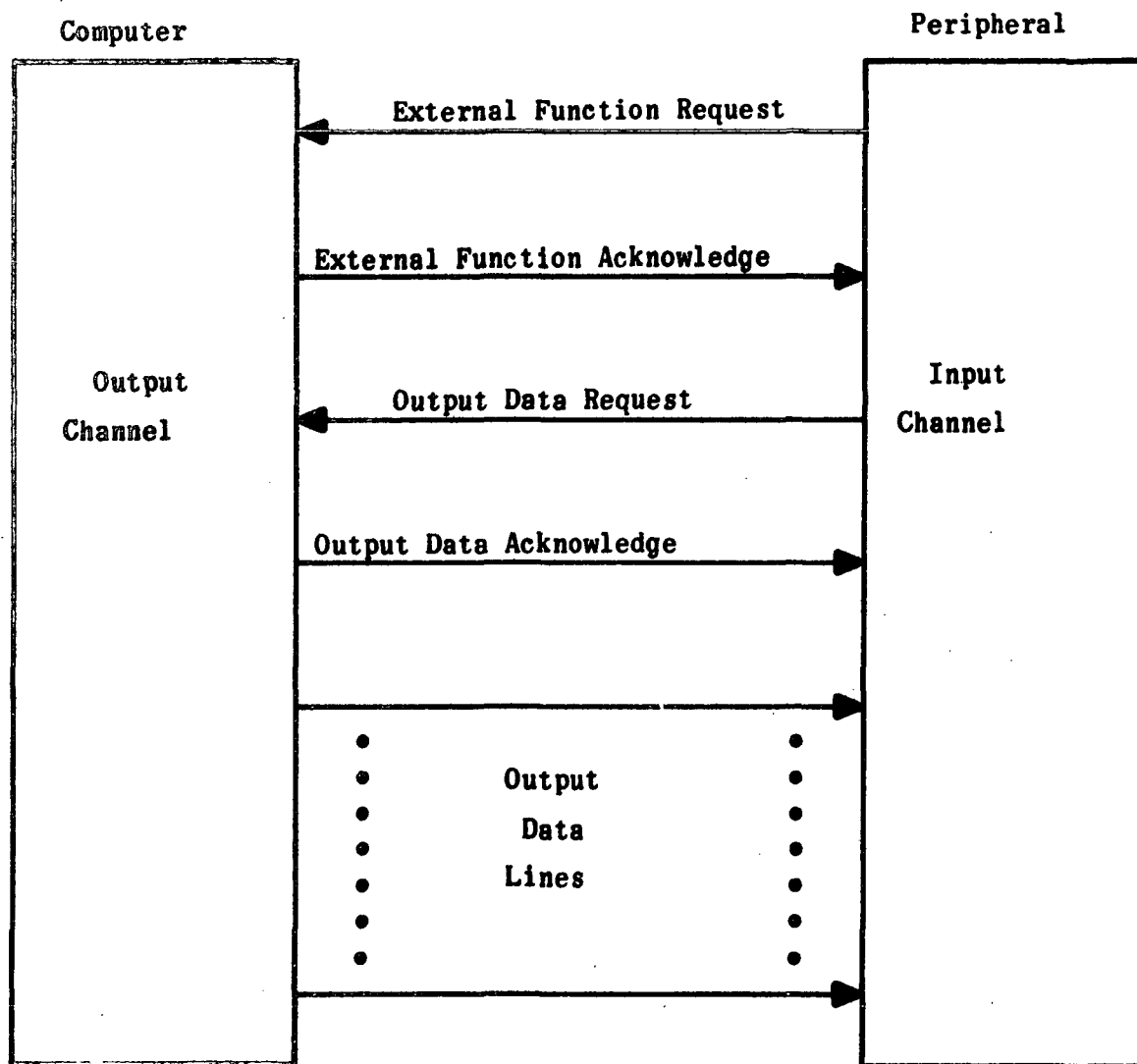
Figure 2.   Typical Memory Module Parallel Interface
- Peripheral Applications -

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SPECIFICATION SHEET

| SHEET I-12 | REVISION |

SPECIFICATION SYMBOL
PX-5714
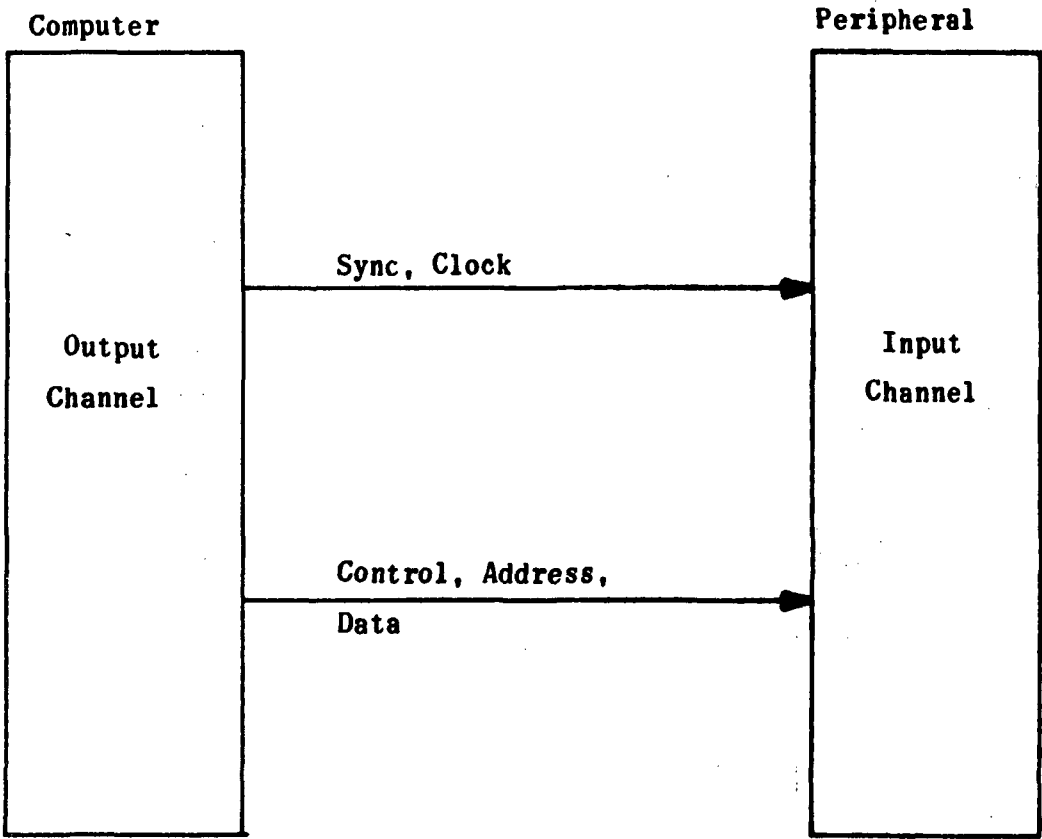
Release Date:

Figure 3.   Typical Memory Module Serial Interface
-Peripheral Applications-

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Release Date:

3.2.1.2 Detailed Interface Definition

TBD

3.2.2 Component Identification

3.2.2.1 Government Furnished Property List

Not Applicable.

3.2.2.2 Engineering Critical Components List

TBD.

3.2.2.3 Logistics Critical Components List

TBD.

3.2.3 Technical Manuals

3.2.3.1 Operating/Maintenance Manual

Univac shall develop an Operating/Maintenance Manual for the Oligatomic Mass Memory.
This manual shall be developed in accordance with requirements as stated within
NASA Specification TBD. This technical manual shall contain information including:
theory of operation, installational instructions, general description, trouble
shooting charts, drawings, and wire tabs.

3.3 Design & Construction

3.3.1 General Design Features

3.3.1.1 General Design Requirements

The Oligatomic Mass Memory shall be designed in accordance with NASA Specification
TBD.

Release Date:

3.3.2 Physical Characteristics

3.3.2.1 Form Factor

The Oligatomic Mass Memory shall have external dimensions as follows: width TBD, height TBD, depth TBD.

3.3.2.2 Weight

The weight of the Oligatomic Mass Memory shall not exceed 45.3 kg (100 lbs.).

3.3.2.3 Volume

The volume associated with the Oligatomic Mass Memory shall not exceed 0.045 cu. m. (1.6 cu ft.).

3.3.2.4 Power

The primary power required by the Oligatomic Mass Memory shall be 113 watts nominally.

3.3.2.5 Selection of Specifications and Standards

TBD

3.3.3 Materials, Parts, and Processes

The materials, parts, and processes utilized within the Oligatomic Mass Memory shall conform to requirements stated within NASA Specifications TBD.

3.3.4 Standard and Commercial Parts

Standard and commercial parts will be utilized in the Oligatomic Mass Memory to a maximum extent consistent with good design practices.

3.3.5 Moisture and Fungus Resistance

The Oligatomic Mass Memory shall be designed to comply with moisture and fungus prevention requirements stated within NASA Specification TBD.

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3.3.6 Corrosion of Metal Parts

The Oligatomic Mass Memory shall be designed to comply with corrosion prevention requirements stated within NASA Specification TBD.

3.3.7 Interchangeability & Replaceability

The Oligatomic Mass Memory shall be designed to achieve a maximum level of parts interchangeability/replaceability consistent with good design practices. The design shall comply with the interchangeability/replaceability requirements stated within NASA Specification TBD.

3.3.8 Workmanship

The Oligatomic Mass Memory shall be fabricated in accordance with workmanship requirements stated within NASA Specification TBD.

3.3.9 Electromagnetic Interference

The Oligatomic Mass Memory shall be designed to comply with electromagnetic interference prevention requirements stated within NASA Specification TBD.

3.3.10 Identification and Marking

The Oligatomic Mass Memory shall be designed with identifications and markings consistent with requirements stated within NASA Specification TBD.

3.3.11 Storage

Not Applicable

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Release Date:

4. QUALITY ASSURANCE PROVISIONS

4.1 Phase I Test/Verification

4.1.1 Engineering Test and Evaluation

The Oligatomic Mass Memory shall be tested/evaluated to assure compliance with requirements as stated within Section 3 of this CEI Specification. The test/ evaluation activities shall include: inspection of the CEI, review of analytical data, demonstrations, and test & review of test data. These activities shall relate to specific requirements as shown on the Performance Requirements vs Test/Verification Activities Matrix for Engineering Test & Evaluation (See Table 3).

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Release Date:

4. QUALITY ASSURANCE PROVISIONS

1.1 Phase I Test/Verification

1.1.1 Engineering Test and Evaluation

The Oligatomic Mass Memory shall be tested/evaluated to assure compliance with requirements as stated within Section 3 of this CEI Specification. The test/ evaluation activities shall include: inspection of the CEI, review of analytical data, demonstrations, and test & review of test data. These activities shall relate to specific requirements as shown on the Performance Requirements vs Test/Verification Activities Matrix for Engineering Test & Evaluation (See Table 3).

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Release Date:

Requirements \ Activities	Inspection of CEI	Review of Analytical Data	Demonstration	Test & Review of Test Data
3.1.1.1.1			X	
3.1.1.1.2			X	
3.1.1.1.3			X	
3.1.1.1.4				X
3.1.1.1.5				X
3.1.1.1.6				X
3.1.1.1.7			X	
3.1.1.1.8			X	
3.1.1.1.9			X	
3.1.1.2.1				X
3.1.1.2.2			X	
3.1.1.2.3			X	
3.1.2.1.1		X		
3.1.2.2.2			X	
3.1.2.5.1	X			
3.1.2.5.2				X
3.1.2.7.1	X			
3.1.2.7.2				X
3.3.9				X

Table 3. Performance Requirements Vs. Verification Activity Matrix
-Engineering Test and Evaluation -

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Release Date:

4.1.2 Preliminary Qualification Tests

Not Applicable

4.1.3 Formal Qualification Test

The Oligatomic Mass Memory shall be subjected to a formal qualification test to demonstrate and/or verify that each requirement established in Section 3 of this CEI Specification has been satisfied. These activities shall relate to the specific performance requirements as shown on the Performance Requirements Vs Test/Verification Activities Matrix for the Formal Qualification Test (See Table 4).

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Requirements \ Activities	Inspection of CEI	Review of Analytical Data	Demonstration	Test & Review of Test Data
3.1.1				X
3.1.2.2		X		X
3.1.2.2.1	X			
3.1.2.2.3		X	X	X
3.1.2.3				
3.1.2.4	X			X
3.1.2.7.1			X	
3.1.2.7.2				
3.1.2.5	X			
3.2.1.1	X			X
3.2.1.1				X
3.3.2.1	X			X
3.3.2.2	X			X
3.3.2.3				
3.3.2.4				
3.3.3		X		
3.3.4		X		
3.3.5				
3.3.6	X			
3.3.7	X			
3.3.8				
3.3.9				
3.3.10	X			X

Table 4. Performance Requirements Vs. Test/Verification Matrix
-Formal Qualification Test-

Release Date:

4.1.4 Reliability Test and Analyses

TBD

4.1.5 Engineering Critical Component Qualification

TBD

4.2 Phase II Integrated Test Requirements

TBD

5. PREPARATION FOR DELIVERY

Not Applicable.

6. NOTES

6.1 Supplemental Information

TBD

6.2 Alternate Source Qualification

TBD

10. Appendix

TBD