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RESEARCH ON VARIABLE THRESHOLD TRANSISTOR STORAGE SYSTEMS

by

H.A.R. Wegener, R.E. Oleksiak and E.T. Lewis

FINAL REPORT – PHASE II
Contract No. NAS 12–686
April 1970

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Prepared for

ELECTRONICS RESEARCH CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
CAMBRIDGE, MASSACHUSETTS

SPERRY RAND RESEARCH CENTER
SUDBURY, MASSACHUSETTS 01776

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RESEARCH ON VARIABLE-THRESHOLD TRANSISTOR STORAGE SYSTEMS

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H. A. R. Wegener, R. E. Oleksiak, and E. T. Lewis

SECTION I

OBJECTIVE

The objective of this program was to develop a fully integrated, electrically alterable, nonvolatile, nondestructive readout control memory using as storage elements metal-nitride-silicon variable threshold transistors. As determined during the course of investigation pursued under Contract No. NAS 12-686, an optimum approach to such a memory was one in which a three-dimensional selection technique was used, both for read and write operations. Electrical isolation of writing and memory circuits was best obtained by means of separate memory and write circuit chips. This method provided better protection from voltage breakdowns, increased circuit flexibility, and greater ease of testing of interim and final circuit elements.

The memory proposed for this effort has 128 words, each consisting of 64 bits. It therefore consists of 64 memory chips, with each chip containing part of the required decoding circuitry. There are 14 input lines and 4 output lines per memory chip. The 14 input lines are decoded by circuits off the memory chip to allow selection of one out of 32 bit positions for reading and writing. Current flow (high or low) at the four output points of each memory chip indicates the contents of the selected bit position. The design goal for read cycle time was 250 nsec.

SECTION II

SUMMARY OF RESULTS

The design and construction of the proposed control memory was successfully completed. This entailed the design and fabrication of 128-bit integrated memory circuit chips and their incorporation into a complete memory system, which also required design and construction.

The memory consists of sixty-four 128-bit memory chips. These are arranged in groups of 16 on four printed circuit cards. Each card output consists of 16 bits each, giving a total of 64 bits. The memory array is interfaced with 16 input drivers, a gated substrate supply, and 64 sense amplifiers and write inhibit drivers. The 16 input drivers are controlled by the outputs of decode circuits that are in turn controlled by a 7-bit address and timing and control circuits. Under operating conditions the read cycle time is 250 nsec.

The successful operation of this control memory is, in itself, a demonstration of the performance of the 128-bit memory chips. During this contract period the design and fabrication of 128-bit memory chips was accomplished. This entailed the circuit design, its topological translation into a planar circuit, mask design and process implementation. During this phase of the program a number of process improvements were made so that we were able to accumulate a significant inventory of operating chips hermetically sealed in 24-lead flatpacks. For the 128-bit chip a preliminary calculation indicated that the read-out delay should be approximately 25 nsec. The measured read-out delay was 50 nsec. The read cycle time quoted earlier for the control memory is longer because of existence of system noise and the presence of "zero-level" feed throughs. The overall memory characteristics agree with those of single memory transistors.

The complete testing of these 128-bit chips was accomplished using equipment that was constructed during this contract period. This test equipment allowed for a simple and rapid evaluation procedure.

SECTION III

DEVELOPMENT OF INTEGRATED MEMORY CIRCUIT

A. Proposed Organization of Control Memory

The original plan was to use a 1 x 128 bit memory chip as the basic building block of the control memory. In this approach, there was only one output (D) per chip, there were eight VG (variable gate) inputs, four GG (gating gate) inputs, and four LG (large gate) inputs.

Considerations arising from the exact layout of the integrated circuit form led to the adoption of a 4 x 32 bit organization. In this approach, the original four LG inputs have been consolidated into one, while instead of 128 bits fed into one D output, there are four groups of 32 bits, each feeding into a separate D output. This results in the advantage that during rewriting, only four 64 bit words have to be stored temporarily, rather than sixteen 64-bit words.

The block diagram of the proposed memory system consisting of 4 x 32 bit subunits is shown in Fig. 1. The 7-bit address is decoded as three separate groups: Two bits are decoded into 1 of 4 LG lines; two other bits are decoded into 1 of 4 GG lines; and the three remaining bits are decoded into 1 of 8 VG lines. These three groups uniquely select 1 of 128 words. Each of the 4 groups of 13 drivers is used to drive a row of 16 memory chips. The outputs of the 4-bit lines (points D) in a column are tied together and connected to the sense amplifier and bit drivers.

B. Description of the Integrated 4 x 32-Bit Memory Circuit

The basic building block of the memory is an integrated circuit containing 128 bits and 32 control gates on the same chip. The organization within the chip consists of 32 words of 4 bits each.

Addressing is accomplished through three sets of gates (designated VG, LG, and GG) which give the memory its three dimensional topology. Figure 2 shows the circuitry which represents one quarter of the 4-bit x 32-word chip: It is a 1-bit x 32-word configuration. The lines VG1 to VG8, GG1 to GG4, G and LG1 are common to the four sections of the chip. Four independent D lines are brought out of the chip.

Writing is initiated by applying +50 V to all VG gates and ground to all other contacts. This procedure shifts the threshold voltages of all locations to their most positive extreme. Transistors storing the extreme negative V_T are then individually selected. To write this threshold voltage into memory location 111, D_1 is set to zero volts, G is set to -40 V, VG1, LG1, GG2, GG3, and GG4 are set to -50 V. Opening the columns controlled by GG2, GG3, and GG4 places all channels of the memory transistors <u>not</u> to be written into at

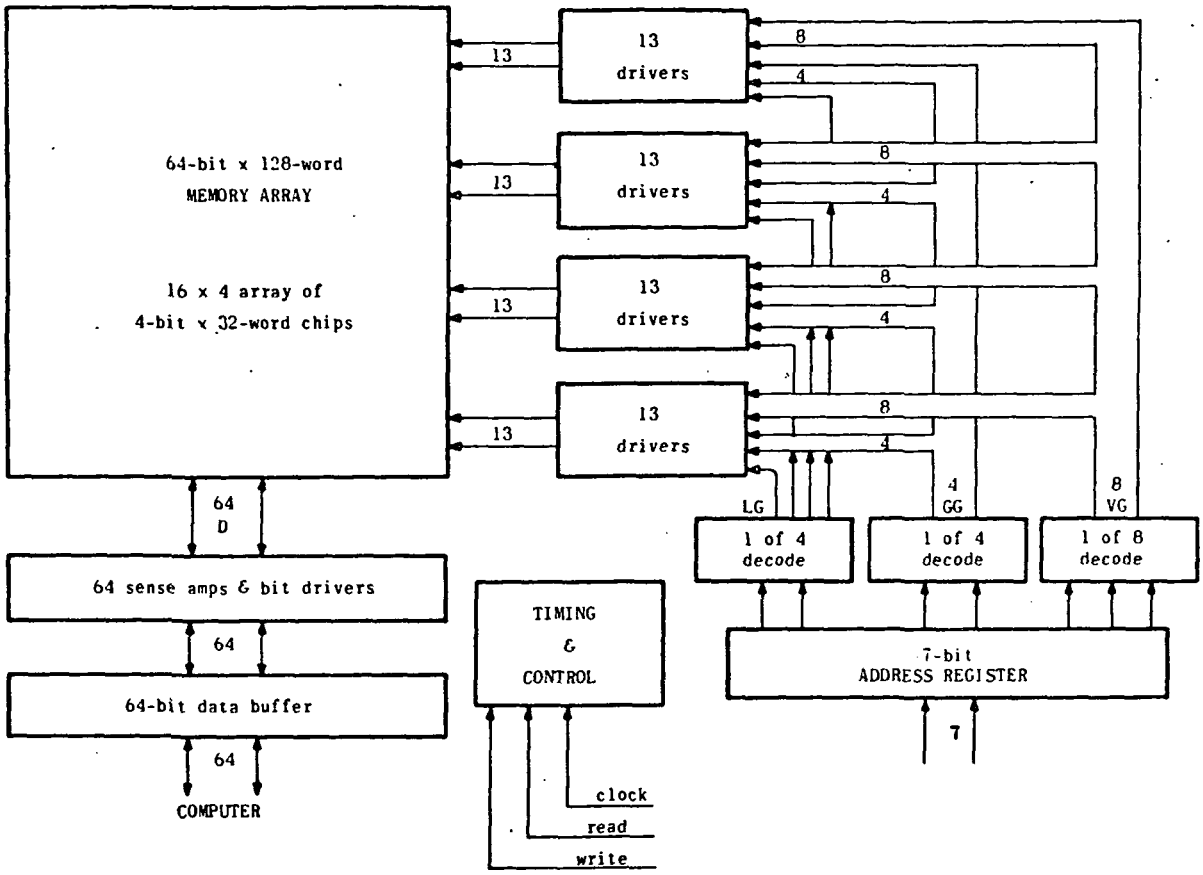


FIG. 1 Block diagram of proposed control memory.

-40 V, since the resistance of the LG transistor is designed to be much larger than that of the devices in series with it. Thus the memory gate dielectrics in these three columns (112, 113, 114) which also are exposed to the -50 V of VG1, see only a potential difference of -10 V, which is not enough to cause a change in the stored information. In contrast, the channels of the transistors controlled by GG1 remain at zero volts, the full potential of -50 V is developed across the dielectric of location 111, and the negative threshold voltage extreme is written into location 111.

Reading is somewhat more straightforward. Now G functions as the input, D functions as the output of the bit line, and addressing is achieved by opening all the gates in the line. To read memory location 111, -2 V are applied at G, -7 V at GG1, VG1, and LG1. If the V_T at 111 is more negative than -7 V, D_1 will see zero volts; if it is more positive, D_1 will see the fraction of the voltage determined by the division of the input voltage across the resistance of the three transistors controlled by GG1, VG1, and LG1.

A 500:1 scale drawing of one bit line in its integrated circuit form is shown in Fig. 3. The labeling of the lines reveals that the layout is strikingly similar to the schematic shown in Fig. 2. By using four of these sub-units, the 128-bit circuit shown in Fig. 4 is built up.

C. Prediction of Read-Out Delay

As the definitive layout of the circuit pattern is completed, a more detailed analysis of the read-out delay of the circuit can be made. The circuit elements involved are outlined in Fig. 5. On the left of that figure the resistive elements of the read-out circuits are outlined, and on the right the capacitance elements are indicated. The resistive elements are represented by the resistances R of the diffused regions between G and D and the reciprocal conductances 1/G of the three transistors GG, VG, and LG in each current path. The capacitances are given by the junction capacitances C_{ji} of the diffused areas and the MIS capacitance C_{Mi} of the metalized interconnections and, particularly, the output contact. The value of these circuit elements can be calculated from the formulas given in Table I. Substituting representative values in these formulas gives the resistance and capacitance values listed in Table II. It is clear that the series resistances due to the diffused conductors are not important, and the inverse conductances of the transistors are dominant. The largest capacitance is associated with the D output pad.

In order to analyze this circuit the differential equations of a three-tier RC ladder must be solved. For fixed resistances and capacitances the solution is basically simple, indicating that the behavior of this network can be approximated by the sum of the three constants:

$$(R_1 + 1/G_1)\, C_{j1} + (R_1 + 1/G_1 + R_2 + 1/G_2) C_{j2}$$

$$+ (R_1 + 1/G_1 + R_2 + 1/G_2 + R_3 + 1/G_3)\, (C_{j3} + C_M) \quad .$$

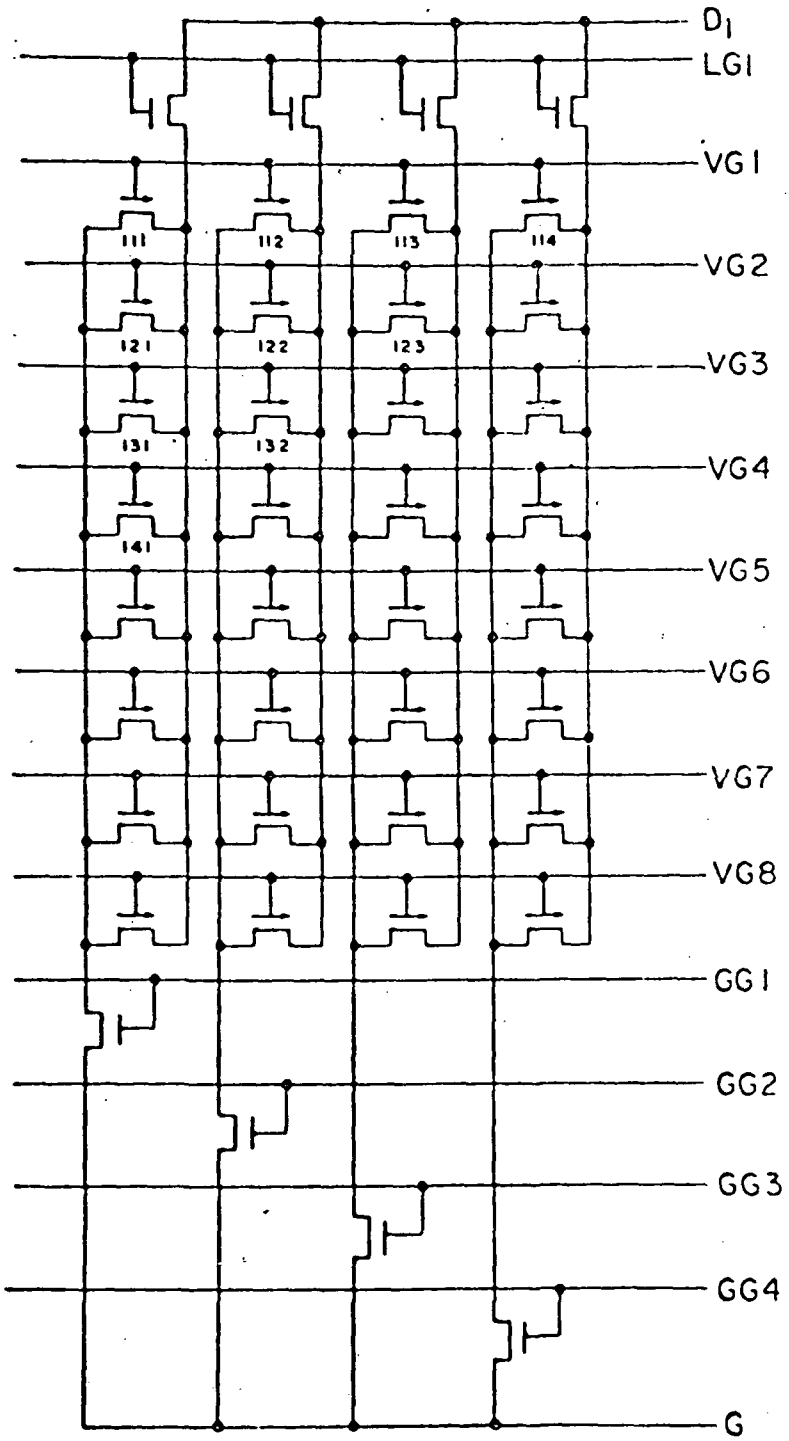


FIG. 2 Representative section of integrated memory circuit.

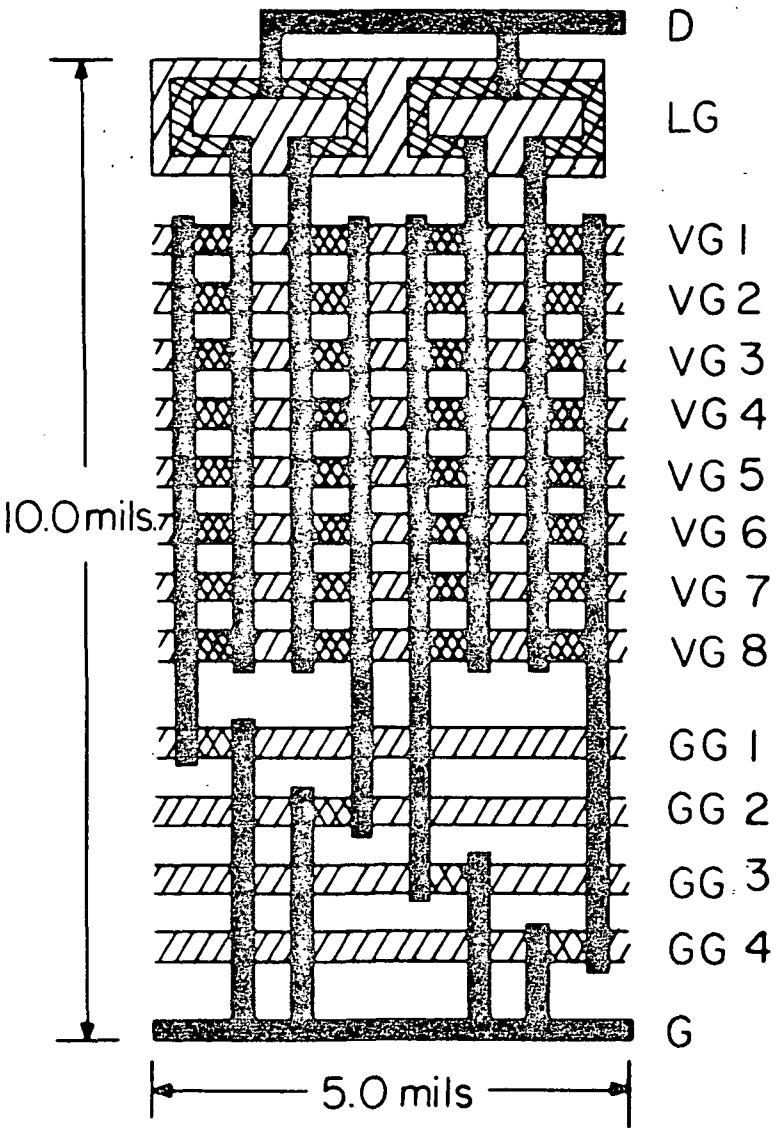


FIG. 3 Circuit pattern of 1 x 32 bit memory section.

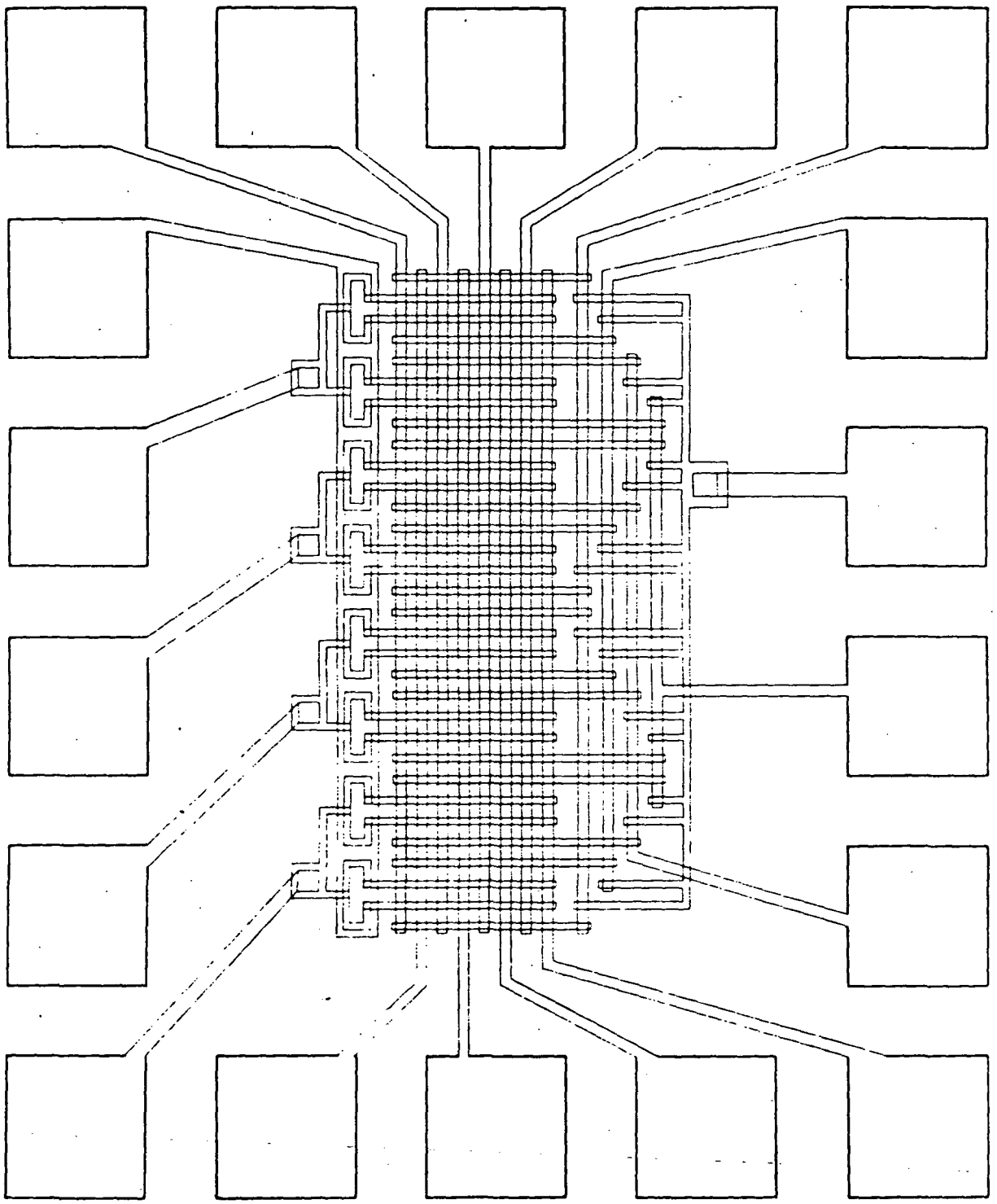


FIG. 4 Composite of mask drawings of 128-bit memory circuit.

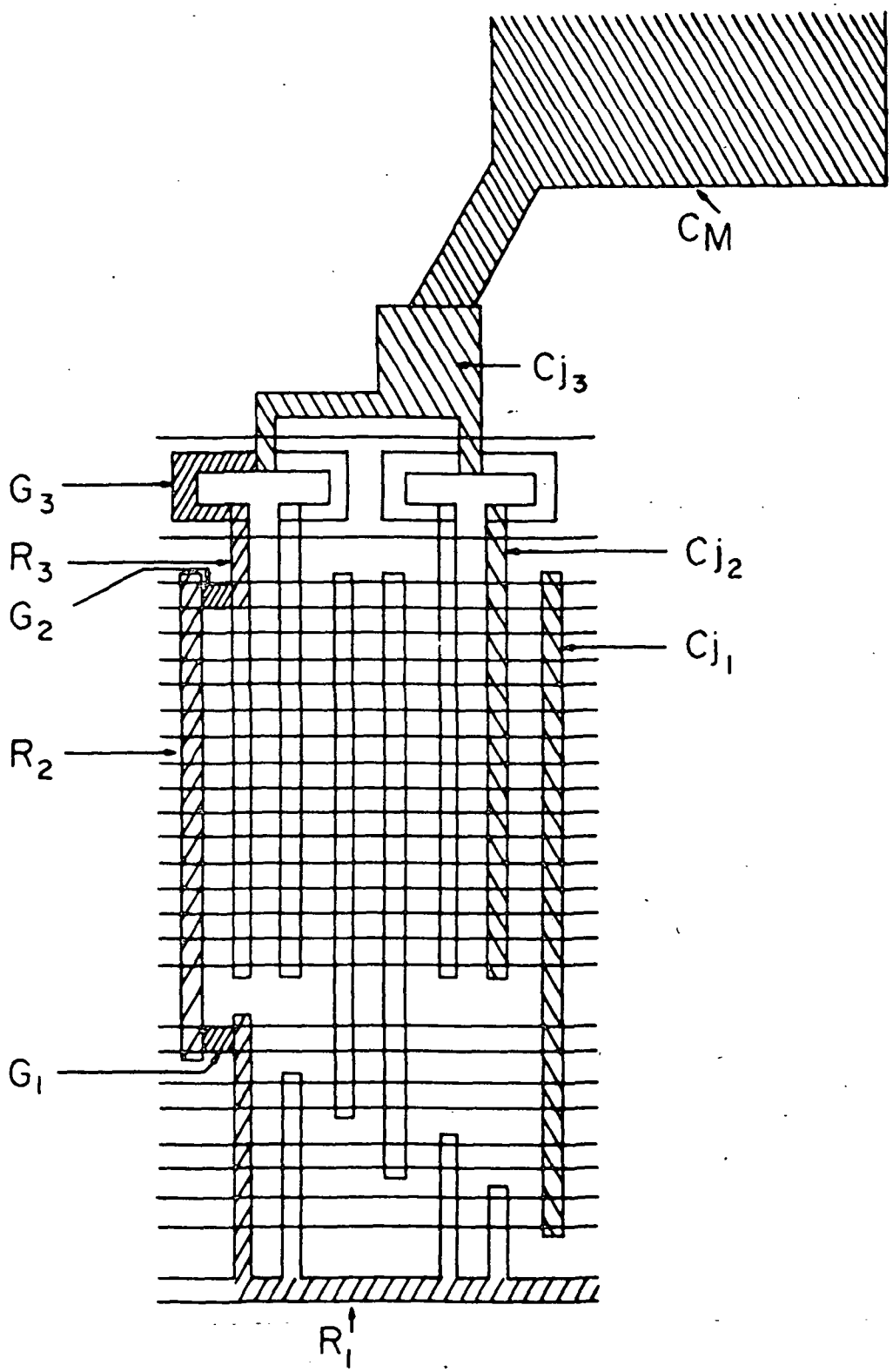


FIG. 5 Identification of resistive and capacitive circuit elements.

TABLE I

FORMULAS

1. Series resistance of diffused areas R_i:

$$R_i = \frac{L}{Z} \rho_s$$

2. On-resistance of IGFET $1/G_i$:

$$1/G_i = \frac{1}{gm} = \left(\frac{L}{Z}\right) \frac{x_o}{\epsilon_I \bar{\mu} \ (Vg-Vt)}$$

3. Junction capacitance Cji:

$$Cji = LZ\left(\frac{\epsilon_{Si}}{\rho_n (V+V_D)}\right)^{1/2}$$

4. Metallization capacitance C_M:

$$C_M = \frac{\text{Area } \epsilon_I}{x}$$

TABLE II

VALUES OF RESISTANCES AND CAPACITANCES

$R_1 = 332\ \Omega$

$R_2 = 192\ \Omega$

$R_3 = 30\ \Omega$

$R_4 = 40\ \Omega$

$1/G_1 = 12{,}500\ \Omega\ (V_G - V_T = 5\ V)$

$1/G_2 = 12{,}500\ \Omega\ (V_G - V_T = 5\ V)$

$1/G_3 = 113{,}000\ \Omega\ (V_G - V_T = 5\ V)$

$C_{j1} = 0.26\ pF$

$C_{j2} = 0.17\ pF$

$C_{j3} = 0.20\ pF$

$C_M = 1.36\ pF$

Unfortunately, neither the conductances of the transistors, nor the junction capacitances are constant with voltage, so that the values calculated from this sum of RC constants are only an approximation. Since C_M is so large, shorting it with a low impedance (R_D) sense amplifier should improve read-out speed. The results of these considerations are shown in Table III. They indicate that for logic level output ($R_D \gg \Sigma R$ circuit), a read-out delay of the order of 300 nsec can be expected, while for current sensing ($R_D \ll \Sigma R$ circuit) an order of magnitude improvement should be discernible.

The writing speed is at present determined by the rate of charge injection into the memory gate. With the accepted value of one millisecond for present structures, the circuit parameters would in no way limit the writing speed. When in single devices the writing speed approaches 0.02 μsec, the speed limitations will be represented by RC constants of the circuit typical of the reading speeds discussed above.

D. Description of Process Steps and Masks

The processing of the 128-bit memory circuit is done by the following steps: A 1-Ωcm n-type slice is covered with an 1850 Å layer of silicon nitride. By standard photoresist procedures, source and drain diffusion windows are etched through the silicon nitride down to the bare silicon. This is followed by the actual p-type diffusion, performed by a Pt box deposition of B_2O_3 at 850°C, and a separate drive-in step at 1200°C. Next, the patterns of the fixed threshold gate areas, the variable threshold gate areas, and the contacts, are etched. Then the variable gate structure, an oxide and a nitride layer, is formed over all bare silicon areas. The following step is a photoresist-etch procedure to bare the silicon in the fixed gate and ohmic contact areas. This is followed by the deposit of a fixed gate nitride. The next photoresist etch step bares the ohmic contact areas once more, and it also decreases the thickness of the silicon nitride over the variable gate. The processing is concluded with aluminum evaporation, definition of the metalization pattern by a final photoresist etch procedure, and a sintering step.

A summary of the process is given in Table IV. It reveals that there are three nitride deposition steps and five photoresist maskings involved. The five masks necessary for the process steps described are shown in Fig. 6.

E. Results of the First Slices Processed

Using the process and the masks described in the previous section, several slices were started on their fabrication run. Within two weeks, the first of these had been completed. This slice was then probed for gate short circuits. Of the roughly 480 dice of 44 × 50 mil^2 area obtainable from 1¼" diameter slice of silicon, 60 exhibited no shorts under the conditions of the measurements. This is roughly a 12% gate yield per slice. These 60 dice were then mounted in 24-lead flatpacks, and 1.5 mil gold wire bonds were made between circuit pads and package leads. Only seven devices survived this step. Since it is normal to expect a 50% survival rate, the failed devices were inspected under the microscope to determine the cause of failure. It was found that

TABLE III

CIRCUIT RESPONSE DURING READ-OUT

1. Maximum output voltage ($R_D \gg \Sigma R$ circuit): logic level = 2 V

2. Maximum output current ($R_D \ll \Sigma R$ circuit)

$$= \frac{2\ V}{48.2\ k\Omega} = 42\ \mu A$$

3. Estimated time delay for 60% of maximum voltage ($R_D \gg \Sigma R$ circuit) in logic level output

$$(R_1 + 1/G_1)\ C_{j1} + (R_1 + 1/G_1 + R_2 + 1/G_2)\ (C_{j2}) + (R_1 + 1/G_1 + R_2 + 1/G_2 + R_3 + 1/G_3)\ (C_{j3} + C_M) = 0.08\ \mu sec$$

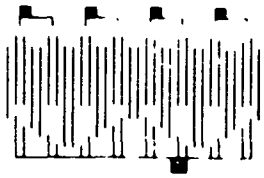
4. Estimated time delay for 60% of maximum current output ($R_D \ll \Sigma R$ circuit) into bipolar sense amplifier

$$(R_1 + 1/G_1)\ C_{j1} + (R_1 + 1/G_1 + R_2 + 1/G_2)\ (C_{j2}) = 0.008\ \mu sec$$

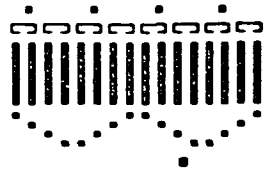
TABLE IV

PROCESSING STEPS

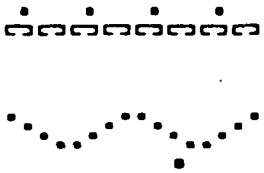
1. Deposition: Diffusion mask silicon nitride
2. Photoresist-etch: Source and drain area mask
3. Diffusion: B_2O_3 deposit
4. Diffusion: Drive-in
5. Photoresist etch: Fixed and variable gate, and ohmic contact mask
6. Deposition: Variable gate silicon nitride
7. Photoresist-etch: Fixed gate and ohmic contact area mask
8. Deposition: Fixed gate silicon nitride
9. Photoresist-etch: Ohmic contact and variable gate area mask
10. Aluminum evaporation
11. Photoresist-etch: Metallization mask
12. Sintering of ohmic contacts.



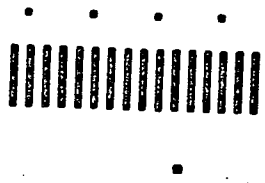
Source and Drain Diffusion



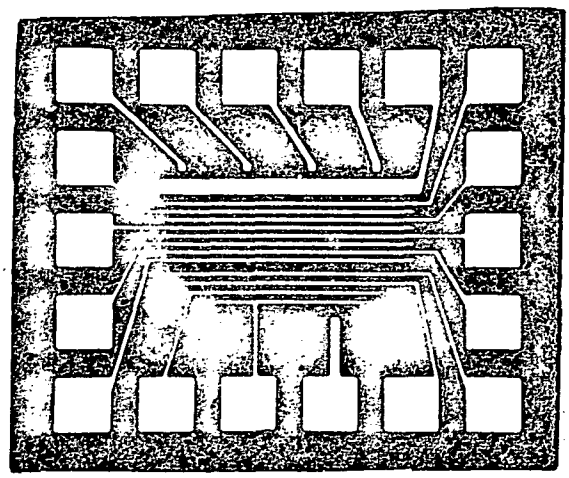
All Gates and Contacts



Fixed Gates and Contacts



Variable Gates and Contact



Metallization

FIG. 6 Photographic masks for 128-bit memory.

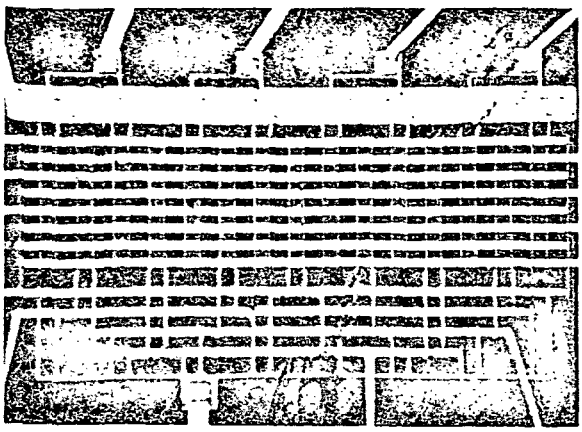
about 80% of the devices failed because of damaged metalization: one-half of this was probably due to scratches caused by improper handling, the other half appear to have been destroyed by electrostatic charges. In order to eliminate the former damages, mounting procedures have been streamlined so that each die is picked up only once. Also the vacuum pencil used is now carefully inspected to insure the absence of uneven surface and burrs. In addition, great pains have been taken to ground all parts making contact with the die. Photographs of the circuit at various magnifications are shown in Fig. 7. The highest magnification (Fig. 7a) shows how closely the circuit pattern follows the schematic shown in Fig. 2. The next highest magnification (Fig. 7b) indicates that the size of the dice is controlled by the number of contacts, requiring a 6 mil center-to-center spacing, rather than by the active circuit area. This indicates that a larger circuit should ultimately be more economical. The photograph of the complete chip (Fig. 7c) shows how small a fraction of the complete silicon chip is occupied by the active circuit, and finally, the last picture (Fig. 7d), how small a fraction of the package space is really occupied by the chip.

F. Performance of First Circuit

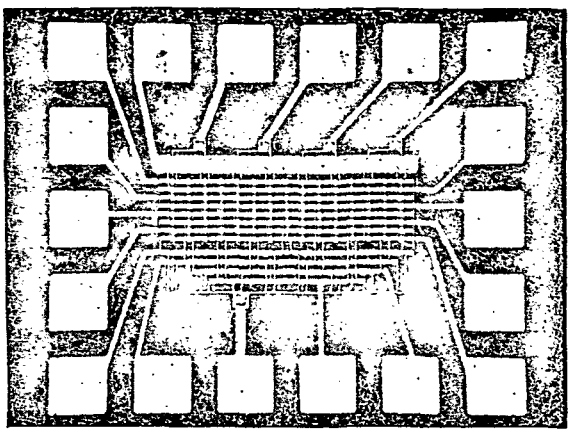
Initially, the writing characteristics of the circuits were tested by grounding all contacts, and by applying the writing voltage to the substrate of the circuit. In this way the threshold voltages of all memory cells were shifted simultaneously. The threshold voltages of the three types of transistors (LG, VG, and GG) were tested by connecting a -10 V supply to contact G, -20 V to all gates not under test, and the scope to a D-line. Then the voltage applied to the gate under test was slowly made more negative, until a 10 μA output was discernible on the scope. In this case it was determined that the threshold voltage in the GG and LG gates were -3 V, and that the threshold voltage extremes in the memory gates were -7 and -18 V for writing voltages of $\pm$60 V.

The read-out delay was determined using the sense amplifier sketched in Fig. 8a. The 2N964 transistors shown have an f_t of 300 MHz, and a beta of 40. Using -10 V on the GG and LG gates, and -10 V on the G contacts, an interrogation voltage of -10 V was placed on a VG gate with a -7 volt V_T The scope indicated a read-out delay of 100 nsec. This value is roughly a factor of four larger than that calculated. It was felt that improving both sense amplifier and measurement circuit should bring the measured value closer to the predicted one. This was accomplished later on with the help of the circuit shown in Fig. 8b. The read-out characteristics obtained in this configuration are shown in Fig. 8c. It is clear that in one packaged memory circuit, the access time was of the order of 50 nsec and the read cycle was about 100 nsec.

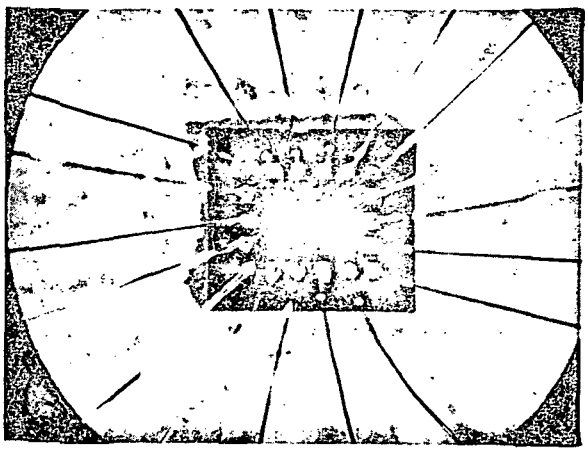
When it was found that the circuit performed reasonably well in its write-in and read-out characteristics, it was examined in greater detail. Particularly, the selective writing of the memory was investigated. For an initially unaccountable reason, the shift in threshold voltage was drastically curtailed under selective writing conditions. A typical set of data is shown in Table V.



(a)
Magnification 195 x



(b)
Magnification 91 x



(c)
Magnification 27 x

FIG. 7 128-bit memory circuit.

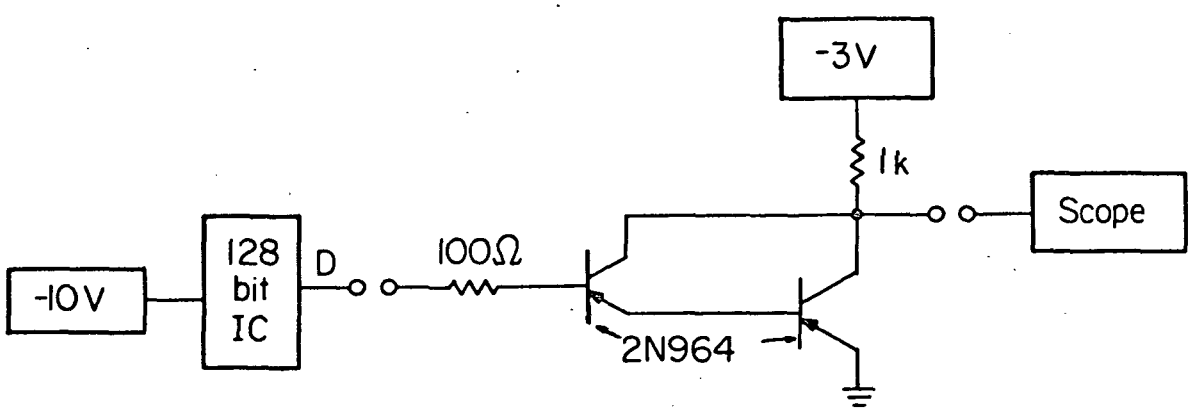


FIG. 8a Schematic of sense amplifier.

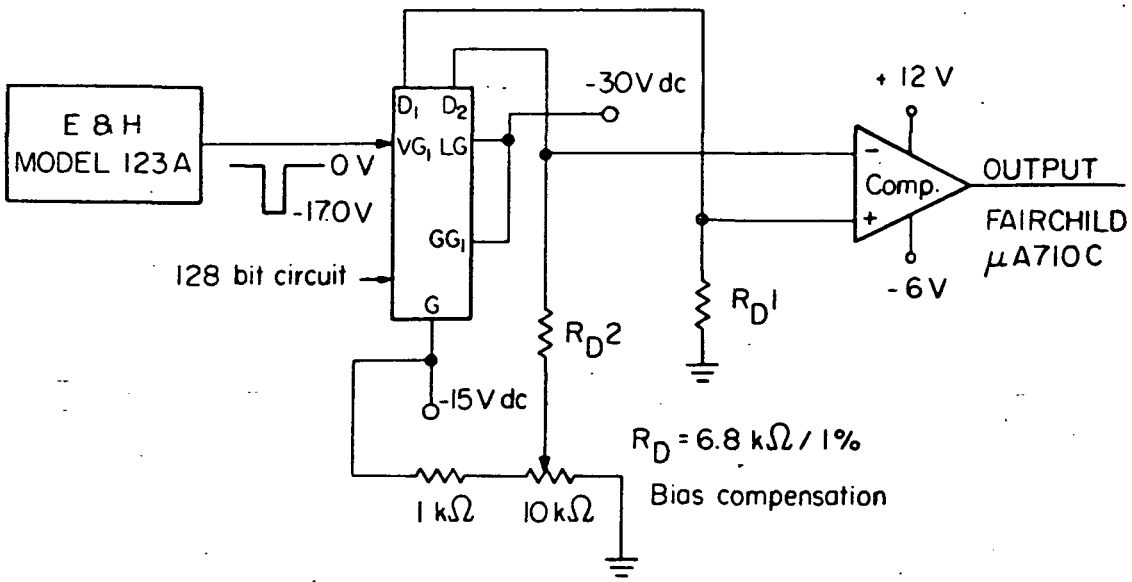


FIG. 8b Improved Read circuit.

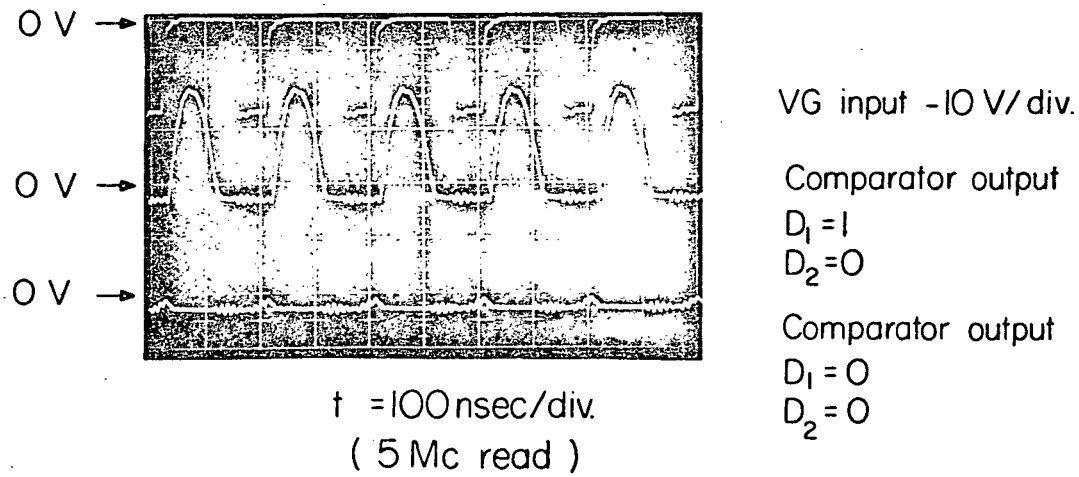


FIG. 8c Read input-output waveforms.

TABLE V

WRITING DATA OF FIRST 128-BIT CIRCUIT

Nonselective Writing		Selective Writing	
$V_{applied}$	ΔV_T	$V_{applied}$	ΔV_T
±20	0	±20	0
±30	0	±30	0
±40	4	±40	0
±50	8	±50	0
±60	10	±60	2

After repeated testing it became clear that somehow the inhibiting condition affected writing potential across a selected memory transistor. A leakage between neighboring columns of memory transistors controlled by different GG gates was postulated. A possible explanation for this leakage could be the inversion of the n-type surface between the drains and sources of neighboring but unrelated memory transistors by the writing voltage of -50 V on a particular VG line. The turn-on of this parasitic transistor would then connect the inhibit voltage from the G-power supply to the line of the transistor to be written into, thus inhibiting this line also. In order to test that hypothesis, -10 V were placed on one D contact, a scope at a heighboring one, and then the negative voltage across the LG gate was slowly increased. When the scope indicated a 10 μA output, an LG voltage of -35 V was noted down. This meant that the parasitic transistor was turned on any time the voltage on a VG line exceeded -35 V. Since, however, the effective resistance of this parasitic transistor was an estimated factor of two larger than that of the GG transistor, only about a third of the inhibit voltage was leaked, so that some writing could occur at -60 V.

It was clear then that the process specifications of the circuit had to be changed in such a way as to increase the threshold voltage of the regions not diffused and not acting as transistor gates, to a value above that of the writing voltage. This would be accomplished by increasing the thickness of the silicon nitride deposited over those regions.

G. Present Status of Circuit Fabrication

Following the preceding work, more slices of the 128-bit integrated memory were completed. Initial tests on the slice indicated that the problem of parasitic turn-on between bit lines has been eliminated.

Packaging of devices from the two completed wafers has been completed. In view of a high gate yield predicted by an on-slice spot check, dice were screened for mounting on a visual basis only. Initially, they had been mounted and bonded, and then checked electrically before capping. Losses incurred by static charge buildup and subsequent gate insulator breakdown during capping forced a postponement of electrical testing until after capping.

One hundred and seventeen dice from one wafer were packaged, and of these, forty-four were found to be fully operative on all 128 bits. This is the first slice that yielded devices that could be selectively written into. The second slice yielded fourteen fully operating devices out of seventy-six that were packaged. Extensive use of the automatic test set described in the following section was made in screening the devices for operability.

Typical device characteristics are shown in Table VI. The parasitic turn-on voltage has been increased to 45 V, which makes selective writing possible. It can be seen that a pulse width of 1 msec at ±45 V is required to obtain a reasonable shift of the memory devices (14 V). Persistency was checked by setting a checkerboard pattern into the memory (i.e., each bit set at one state and surrounded by bits of the opposite state) and then interrogating the memory at -8 V, 10 μsec, 30 kHz for 10 hours. A relaxation of -2 V

TABLE VI

DEVICE CHARACTERISTICS

Junction Breakdown Voltages

(@ 10 μA)

	High	Typical	Low
"G" to Bulk:	-66 V	-60 V	-45 V
"D" to Bulk:	-70 V	-66 V	-58 V
Drain to Source: (*memory*)	-70 V	-66 V	-58 V

Threshold Voltages V_T

(@ 1 μA)

Fixed	High	Typical	Low
"LG"	-4.4 V	-3.5 V	-3.0 V
"GG"	-3.5 V	-2.5 V	-2.2 V
Parasitics:	-48 V	-45 V	-28 V
Variable			
"VG" (initial)	-8.0 V	-7.5 V	-7.0 V

Memory Characteristics

Shift Pulse	V_T	Shift Pulse	V_T
+45 V @ 10 ms:	-5 V	+45 V @ 50 μs:	-14 V
-45 " " " ":	-20 V	-45 " " " ":	-16 V
+45 V @ 1 ms:	-6 V		
-45 " " 1 ms:	-20 V		

for the positive set V_T and +2 V relaxation of the negative set V_T resulted, leaving a reasonable 10 V difference. Operating conditions under which these circuits function are shown in Table VII.

More wafers have been completed including on-slice testing. The device characteristics are the same as for the wafers described above, except that the parasitic turn-on voltage on one has been increased to 75 V, by further increasing nitride thickness between word lines.

H. Test Equipment

Initial work in the evaluation of the circuit made it clear that a more rapid method of acceptance testing the 128-bit circuit was necessary. By techniques adapted from single transistor testing, it took several hours to evaluate a single circuit. The complete evaluation of each slice containing hundreds of circuits could have taken weeks. For this purpose, the Automatic 128-Bit Memory Circuit Reader was designed, built, and put into operation.

Its circuit schematic is shown in Fig. 9. It permits simultaneous writing of either ones or zeros into a single 32-bit section of the memory circuitry, and an automatic and serial read-out of each cell. A 32-light bulb display permits the location of memory cells that show a "one" when it should have been a "zero", or vice versa. A photograph of this equipment is shown in Fig. 10.

This test set is capable of providing an impressive amount of detailed information. This can be obtained with the help of controls that adjust the input voltages during read out, and the amplitude and duration of the writing pulses. Both individual and average writing time and storage time data can be obtained with this equipment, and it has been used in this capacity in the evaluation of the 128-bit circuits just completed.

TABLE VII

OPERATING CONDITIONS - 128-BIT MEMORY

Terminal		I Clear	II Read:M123	III Write:M123 only	IV Write: All VG1	V Write: M_{1n1} n = 1,2,3...8
D	1	GND	Current Amplifier	GND	GND	GND
	2	"	GND	-35 V @ 1 ms	"	"
	3	"	"	"	"	"
	4	"	"	"	"	"
LG	1	-15 V dc	-15 V dc	-35 V @ 1 ms	-15 V dc	-15 V dc
VG	1	+45 V @ 1 ms	GND	GND	-45 V @ 1 ms	-45 V @ 1 ms
	2	"	-10 V @ any read cycle	-45 V @ 1 ms	GND	"
	3	"	GND	GND	"	"
	4	"	"	"	"	"
	5	"	"	"	"	"
	6	"	"	"	"	"
	7	"	"	"	"	"
	8	"	"	"	"	"
GG	1	GND	GND	-45 V @ 1 ms	GND	GND
	2	"	"	"	"	-45 V @ 1 ms
	3	"	same as VG2	GND	"	"
	4	"	GND	-45 V @ 1 ms	"	"
G	-	-3 V dc	-3 V dc	-35 V @ 1 ms	-3 V dc	-3 V @ 1 ms

(Substrate is at GND at all times)

I. The Clear condition will set all memory devices to the least negative V_T.

II. This column indicates how one bit (M_{123}) can be interrogated.

III. This column indicates how one bit (M_{123}) can be set to its most negative V_T, while holding all other bits in the memory to a less negative V_T than the read voltage (keeping the balance at a V_T that will allow the read voltage to turn them on).

IV. This is a write condition that will set bit #1 in all 16 words, i.e., M_{111}-M_{114}; $M_{211-214}$; $M_{311-314}$, $M_{411-414}$. (Word lines run vertical).

V. This write condition demonstrates the use of the "GG" gates to select a word line. If the "D" lines are not used to inhibit, word line one from each "D" section will be set negative, i.e., each word line connected to GG1 in this case.

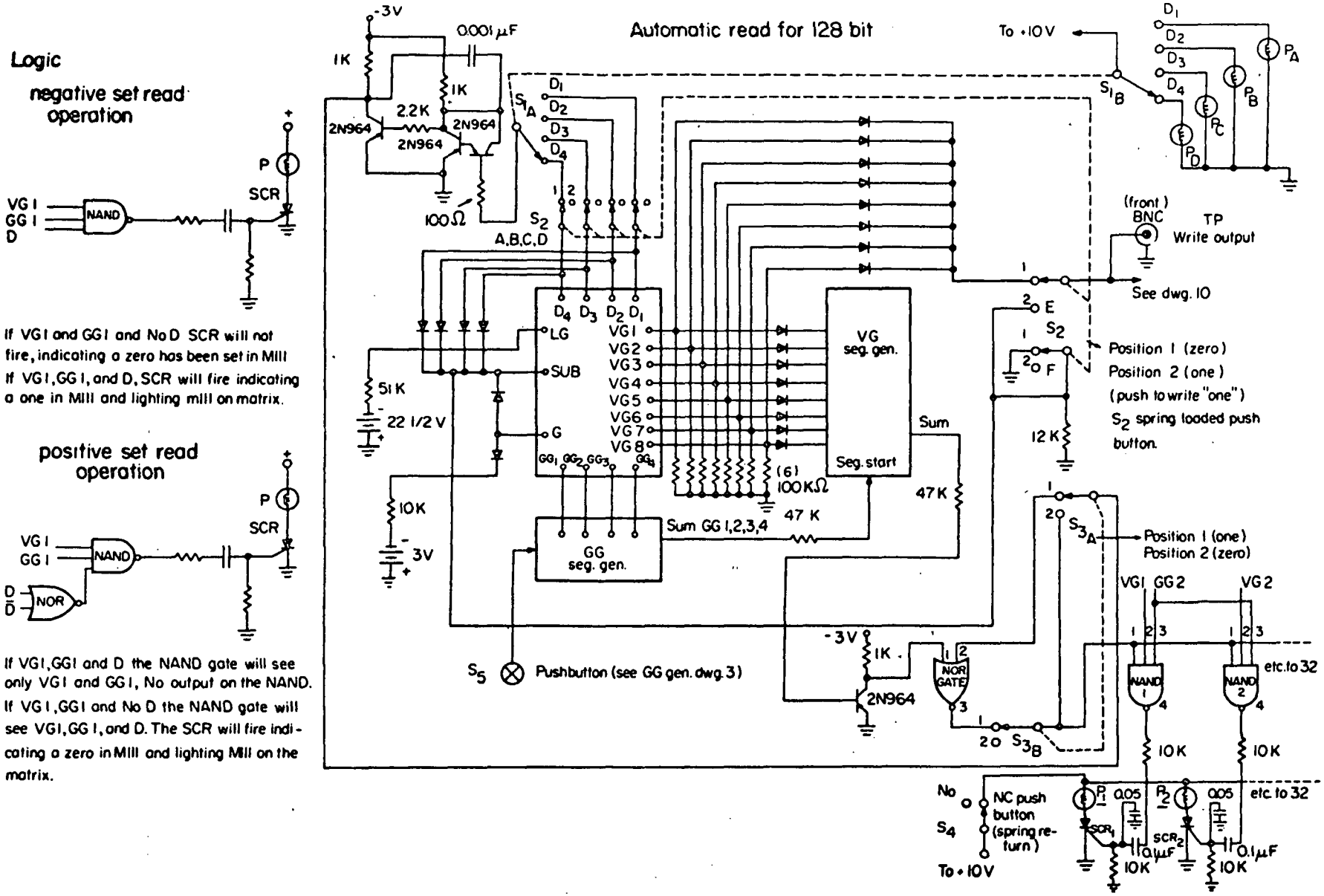


FIG. 9 Circuit schematic of 128-bit memory circuit reader.

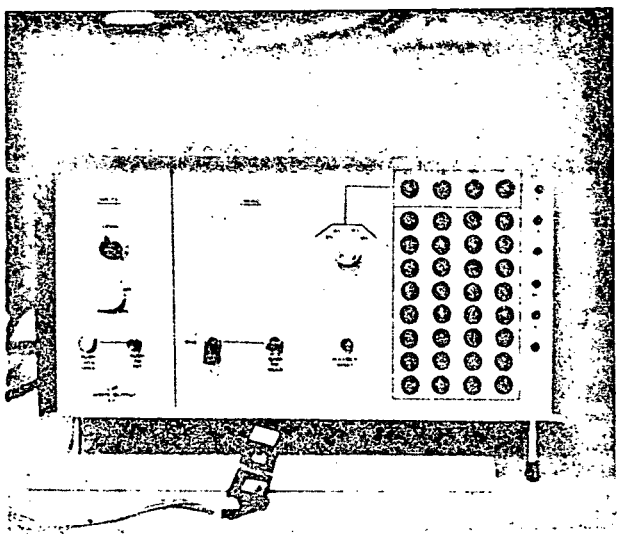


FIG. 10 Memory circuit reader.

SECTION IV

CONTROL MEMORY SYSTEM

A. System Organization

The 8192-bit memory is organized into 128 words of 64 bits each. The memory operates in a random-access word-organized mode during read or write operation and in a block-organized mode during erase (clear) operation. The data is read nondestructively as a 64-bit word in parallel. Data is stored by first clearing a block of 16 words. The desired data is then stored in the 64 bits of the desired word in parallel. The 16 words of the block can be written in a random order.

The interface to the system consists of 64 data input lines, 64 data output lines, 7 address lines and 4 control lines. A block diagram of this system is shown in Fig. 11. The data input lines are TTL level inputs, a +5 V level causing a zero to be written during set mode. The data output lines have 5 V swings but are referenced to +20 V. Capacitive coupling can be used to restore the voltages to TTL levels. Strobing of the outputs should be done no sooner than 250 nsec after the initialization of the read cycle. The 7 input lines are normal TTL levels. The clear blocks are specified by the 3 high order bits.

B. Hardware Implementation

The memory is contained on five printed circuit cards. One printed circuit card contains the address decode, power drivers, and the LG, VG and GG drivers. The four other cards are identical, each containing 16 memory chips organized into a 128 word by 16 bit memory, 16 sense amplifiers and 16 write inhibit drivers. The VG, LG and GG inputs of these four cards are connected in parallel to organize the memory into a 128 word x 64 bit memory.

Driver Card. The circuitry contained on the driver card is shown in Figs. 12 and 13. Photographs of the actual driver card are shown in Figs. 14 and 15. The address decode is straightforward. The 7 bit address is split into groups of 2 bits, 2 bits and 3 bits each. The two lowest order bits, 2^0, 2^1, are decoded into one of four GG lines. The 2^2 and 2^3 bits are decoded into one of four LG lines. The three highest order bits, 2^4, 2^5, 2^6 are decoded into one of eight VG lines. The GG and VG lines have different modes of operation during READ, CLEAR, and WRITE (SET) mode. During READ mode, the selected state of the desired GG, LG and VG driver is GND. VG is the only signal that has any effect during CLEAR mode, the selected state being a positive voltage and the unselected state being GND. This change in selection mode is accomplished by gating the inverted output of the decoder to drive the VG drivers. During WRITE mode, LG drivers and VG drivers operate in a normal manner while the selected GG driver is at a positive voltage with the other GG drivers at GND.

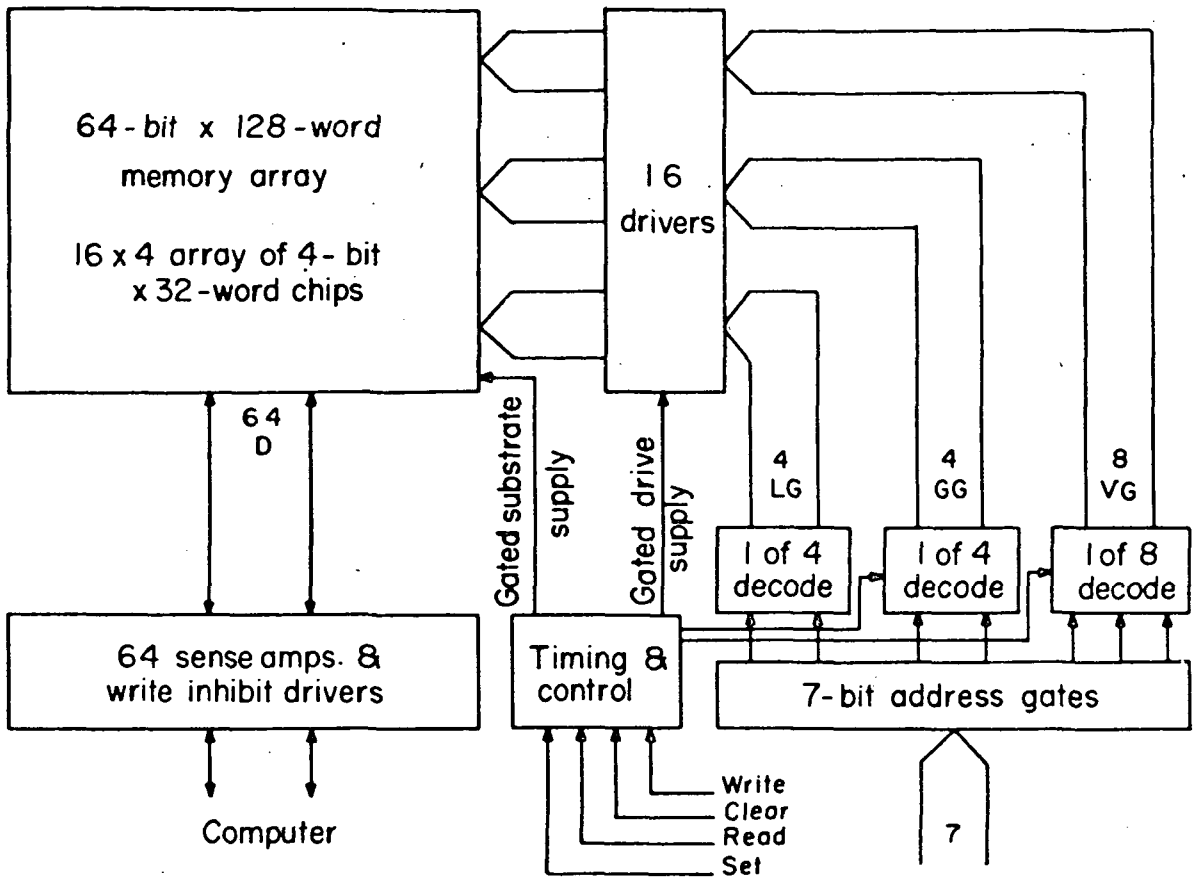


FIG. 11 Block diagram of control memory.

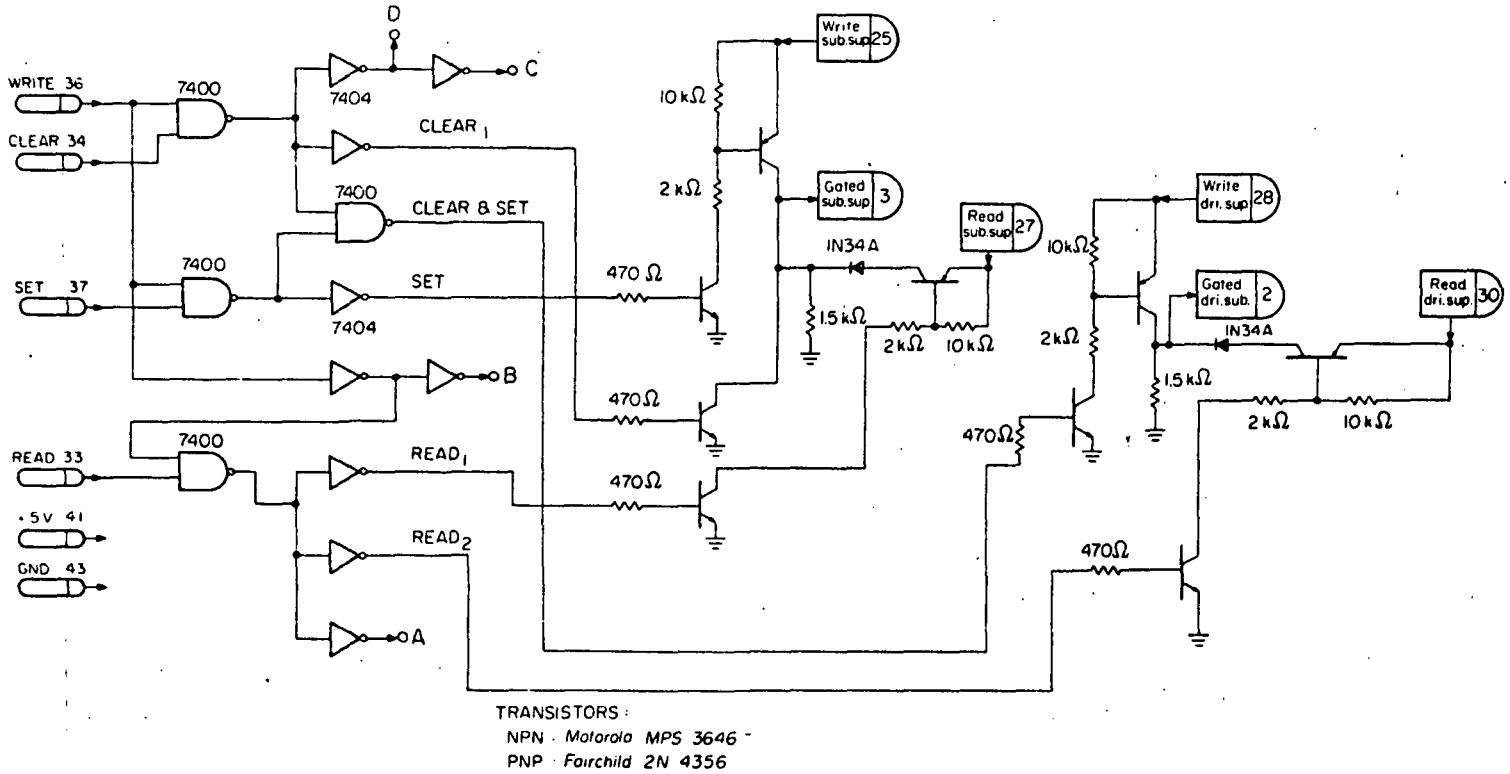


FIG. 12 Timing and control circuits.

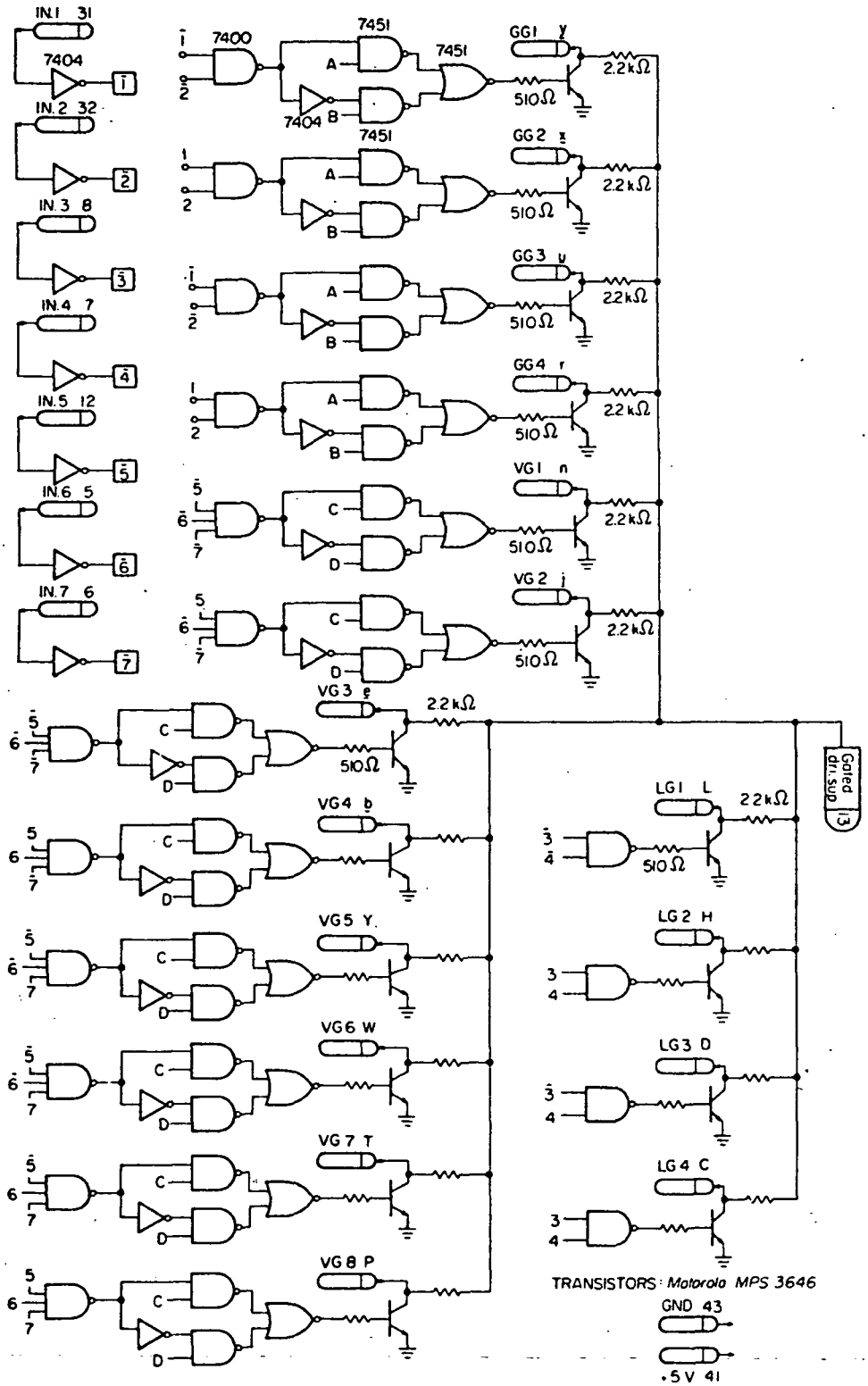


FIG. 13 Decode and driver circuits.

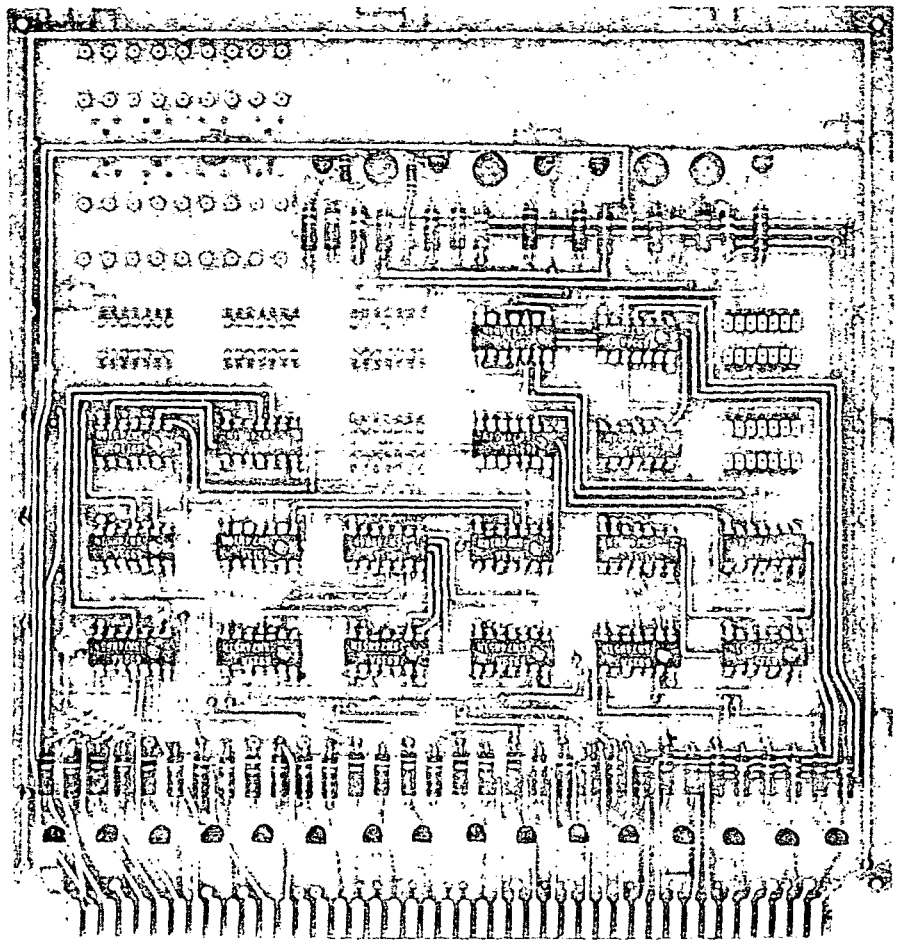


FIG. 14 Front view of fully wired driver card for control memory.

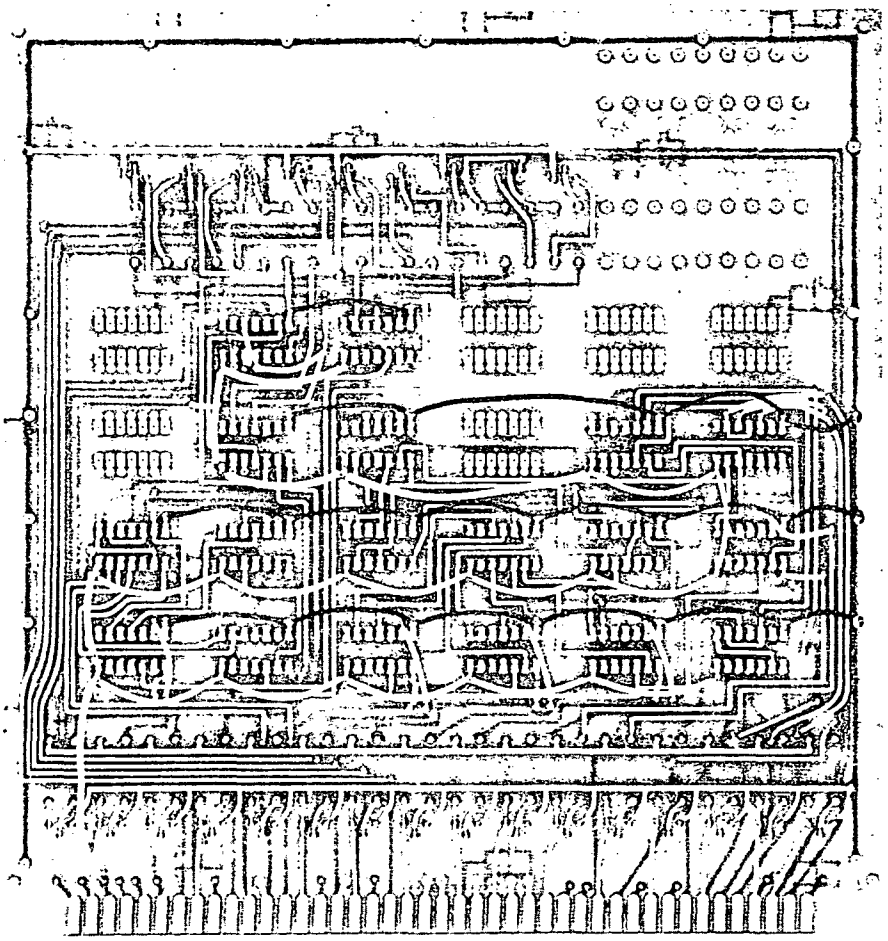


FIG. 15 Back view of fully wired driver card for control memory.

The other signals generated on the driver card are the Gated Substrate Supply (GSS) and the Gated Driver Supply (GDS). The GSS has the following three voltage levels: +40 V during WRITE mode, +20 V during READ mode and GND during CLEAR mode. The GDS is at +40 V during WRITE and CLEAR modes and at +20 V during READ mode. The timing of the signals on the driver card is shown in Fig. 16.

C. Memory Card

The circuitry of the 128 x 16 memory card is shown in Fig. 17. Photographs of the actual memory card are shown in Figs. 18 and 19. The card contains 16 inhibit drivers (Motorola MPS3646 and Texas Instruments SN7400 logic gates), 16 integrated circuit sense amplifiers (Fairchild μL 710 comparator) and 16 packaged memory chips. The memory chips operate in the manner described for the individual memory chips. The manner in which the chips are tied together can best be understood with the simpler circuit shown in Fig. 20. The lines from four different chips, each chip having a different LG line, are tied to a common bus through 1 KΩ resistors. The resistors are used primarily as a debugging aid to help locate shorted units. During READ mode, the inhibit transistor is turned off and does not effect circuit operation. Continuity between G and D through the path selected by VG, LG and GG will cause current to flow through the memory. This current causes the inverted input of the Fairchild μL 710 comparator to be pulled more negative than the common reference threshold (positive input) and the output of the comparator to change state indicating a ONE. During WRITE mode after the memory has been cleared to the ONE state, the substrate voltage is at +40 V. The selected bit is set at ZERO when the inhibit driver is not turned on and the D line is returned to +40 V through the 20 K resistor. The diode is reverse biased at this time to decouple the 710 comparator and allow the +40 V swing. If the inhibit driver is on during the WRITE mode, the D line is held at approximately +12 V and write VG line at GND; the memory transistor is not set to ZERO.

D. System Performance

About half a year after the start of the contract, when the 128-bit chips had already been designed and fabricated, modification of the performance goal for the control memory was suggested by the contractor. This modification was the availability of an access time of only 100 nsec during the read cycle. Since the original specification had left this performance characteristic open, the integrated circuit had been designed without this added constraint in mind. It remained therefore only to attempt to meet this requirement by manipulation of the circuitry external to the memory chip. The system described in this report represents our attempt to accomplish this. The attempt to obtain a 100 nsec access time led to design decisions which resulted in a sacrifice of operating margins in order to gain speed. The 100 nsec were in reality at most 80 nsec because one flip-flop delay was incurred before the address was available to the decoder, and the output data were required 10 nsec early because of the set-up time of the data register. The three logic stages in the decoder required an excess of 20 nsec even with high speed logic. This allowed less than 60 nsec total delay

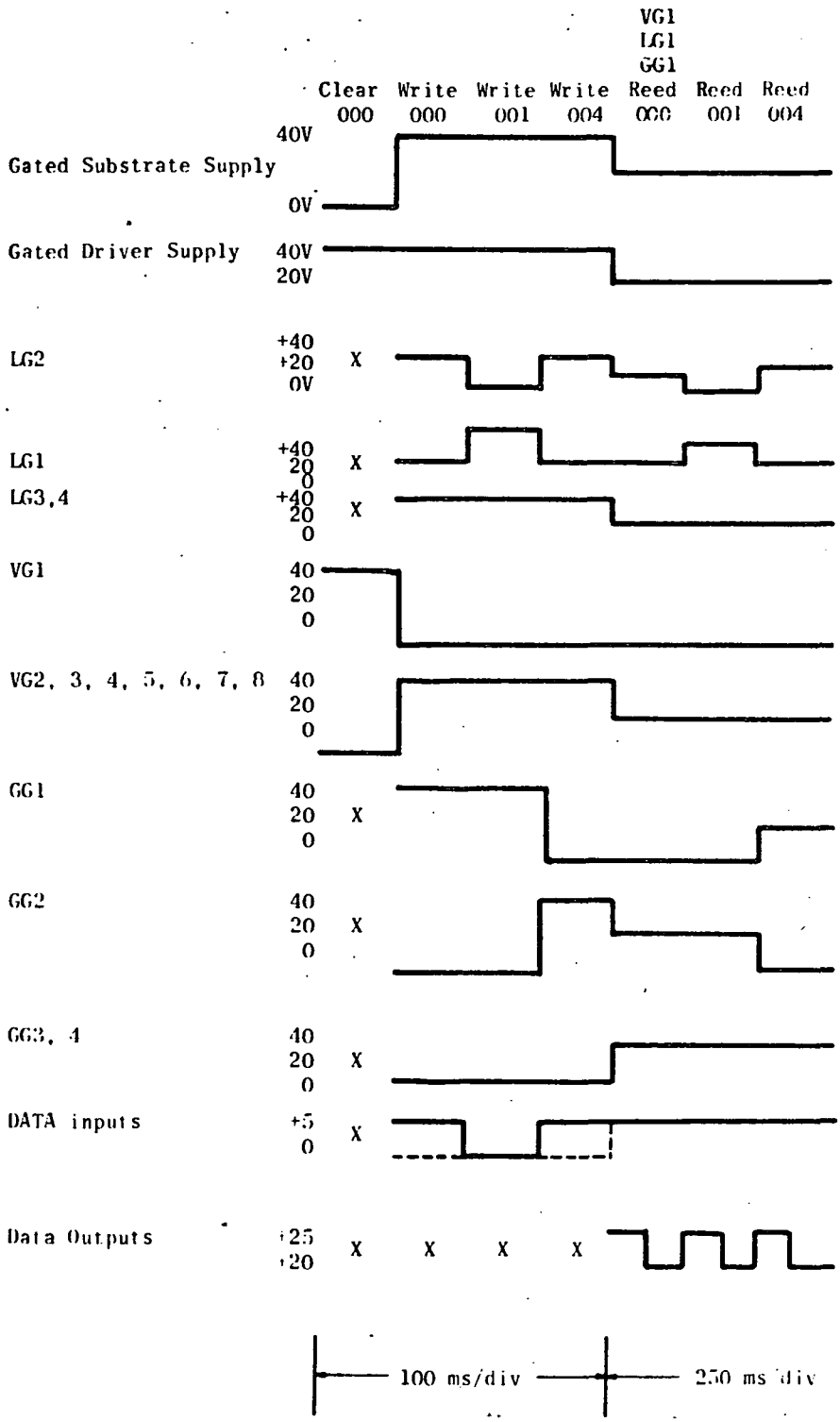


FIG. 16 Timing signals.

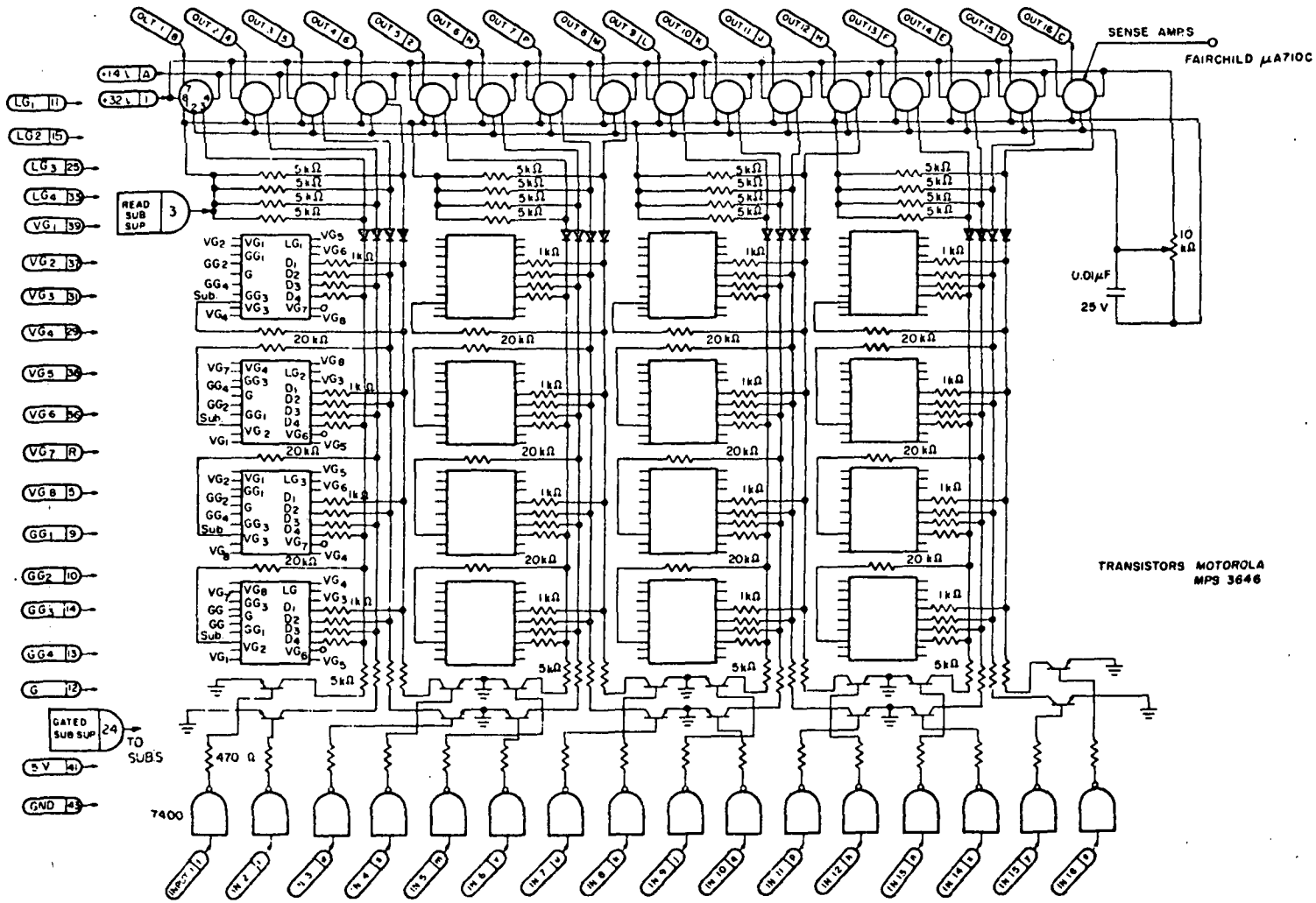


FIG. 17 128 x 16 memory card circuits.

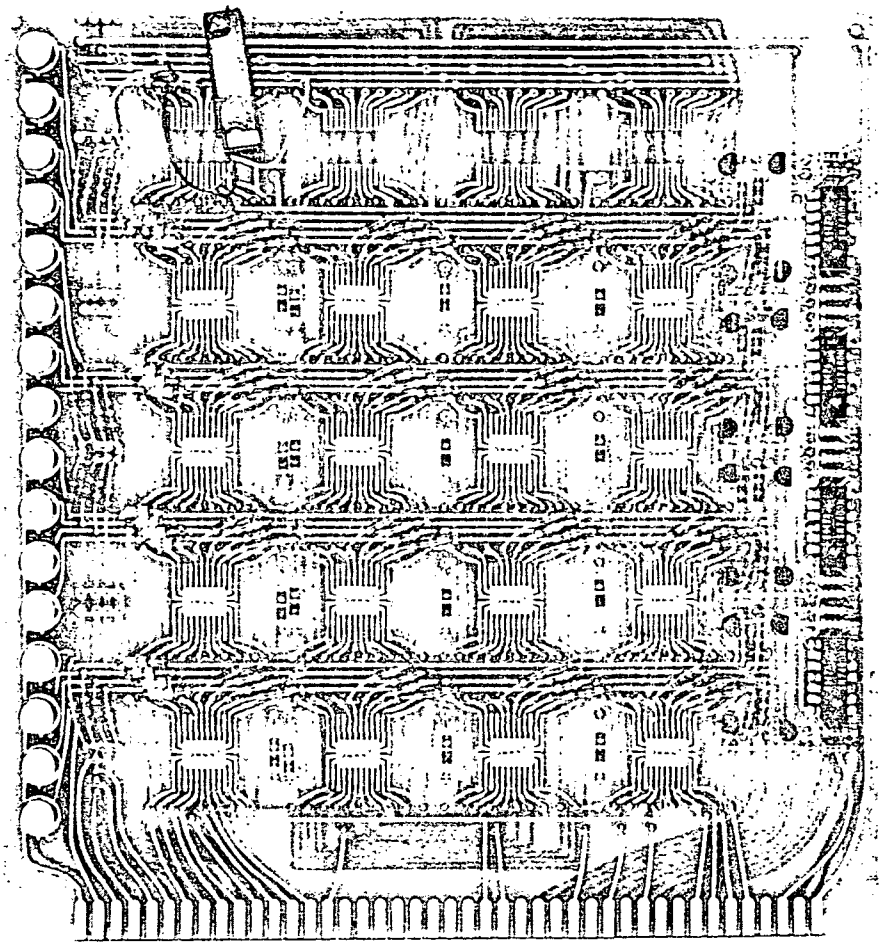


FIG. 18 Front view of 128 × 16 fully wired memory card.

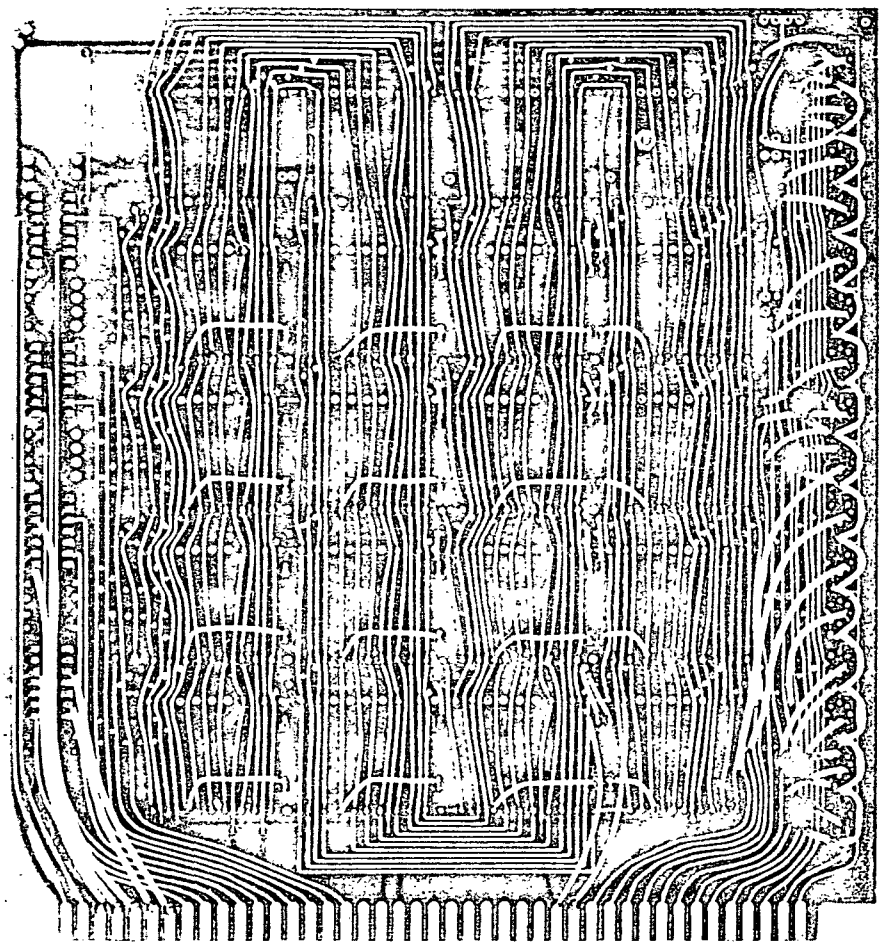


FIG. 19 Back view of 128 × 16 fully wired memory card.

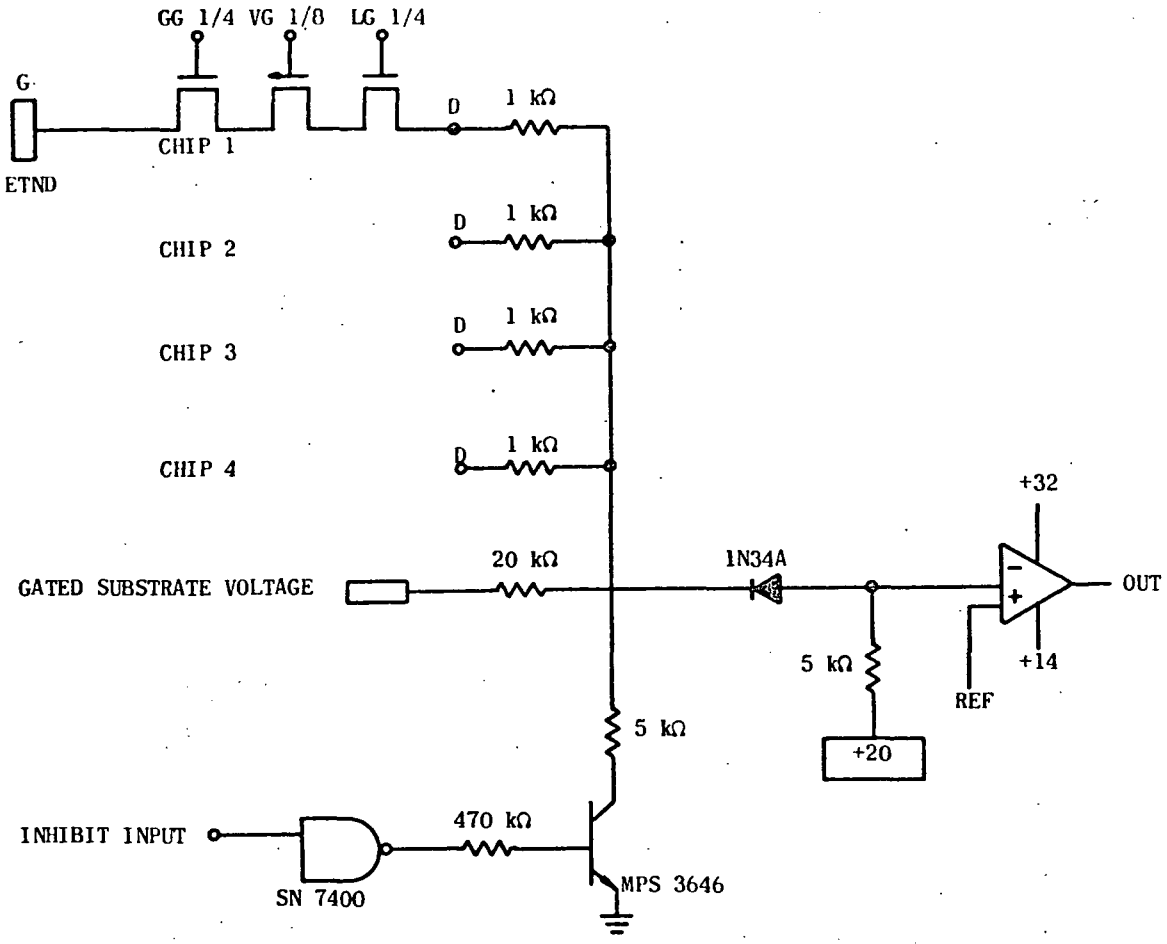


FIG. 20 Simplified circuit diagram of output signal sensing.

for the drivers, memory and sense amplifiers. The circuit of the 128 bit memory chip with its high internal resistance was, however, not quite capable of these speeds in a system where it must drive external lines.

The only possible way of achieving the access time goal was to attempt to overdrive the memory and to sense on the leading edge of the output signal. Two approaches were taken in the attempt to make it possible to sense on the leading edge. The first was to run the drive lines and the sense lines on opposite sides of the printed circuit card at 90^0 to each other to minimize coupling. Four extra memory chips were put on the card which would be set to ZERO and be driven in the same manner as the regular memory chips. It was hoped that the device on the sense lines of these four units would be proportional to the noise on the signal lines and these lines could feed the threshold inputs of the comparator to subtract the noise from the signal lines. Unfortunately, the variation of noise patterns on the signal line and dummy line was too great to make this approach useful.

Several methods of coupling the D line to the sense amplifier were also attempted. The need for this arose from the problem of protecting the D line junctions from becoming forward biased (drain to substrate). At the same time the input voltage of the comparator must be limited to prevent damaging the comparator. Various capacitive coupling techniques together with diode clamping were tried. The baseline shift with different pulse trains made this unworkable. It was decided that signal restoration to true ground should be established after the sense amplifiers. The low impedances would allow a capacitive coupling scheme to be used.

The wave forms of the ONE-ZERO signals are shown in Figs. 21 and 22. The input signal has approximately 100 mV separation between the ONE and ZERO after the initial noise pulse. This is enough to saturate the sense amplifier output and obtain logic level outputs. The sense amplifier output was obtained using a dc threshold level. The output goes high at the beginning of the read cycle due to the noise pulse on the input. The output is valid 200 nsec after the initialization of a read cycle. More complex threshold waveforms did result in faster access times due to the variations in input noise. The noise level could be reduced to some extent but it always remained much larger than the input signal. The operating margin of the system could, however, be increased by the use of a stage of gain before the comparator.

Had the memory been designed for an access time of 200 nsec from the start, good operating margins could have been obtained. The level transitions between TTL to MOS to low level output to TTL could have been designed for wide operating margins rather than speed. The use of switched voltages which are positive to system ground to be used as memory ground is a stiff penalty to pay in order to obtain speed. The memory could have also been operated in a grounded source mode rather than a source follower mode. This would have made the polarity of the noise opposite that of the signal and simple threshold sensing would give a distinct ONE output signal. The sense amplifiers could have been a slower but higher gain circuit, which would have increased the operating margins. The output waveforms during a cyclical read

is shown in Fig. 23. The scope triggering was adjusted so that "one - zero" overlap would occur. Prior to the initialization of the read cycling a random pattern was stored in the memory. The figure indicates where, in time, the output sensing should be accomplished.

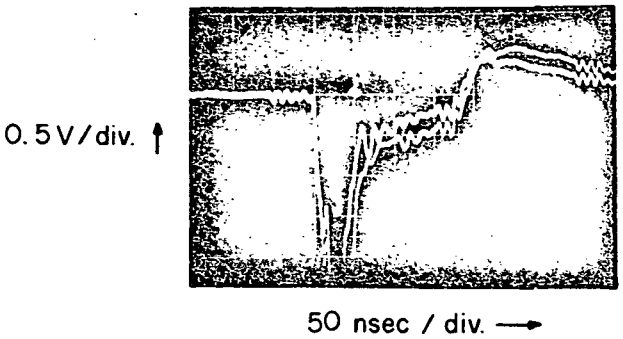


FIG. 21 "D" - line output before comparator.

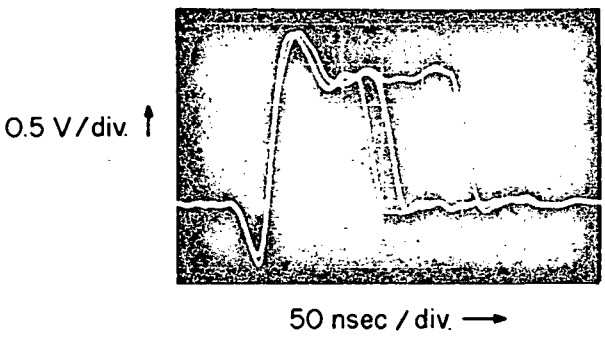


FIG. 22 "D" - line output after comparator.

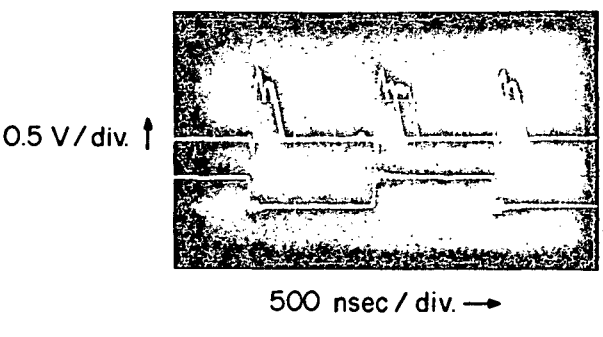


FIG. 23 Output waveform during a cyclical read operation.

SECTION V

NEW TECHNOLOGY APPENDIX

Pursuant to the "Reporting of New Technology" clause of the subject contract, no "reportable items" were conceived or first actually reduced to practice in performance of the subject contract except for the following:

Item I - Subject Invention: Three Dimensional (3D) Selection Technique

Inventor: Robert E. Oleksiak

Item II - Subject Invention: Solid State Memory Array Using Variable Threshold Field Effect Transistors

Inventor: T. Williams