https://ntrs.nasa.gov/search.jsp?R=19790021262 2020-03-11T19:15:12+00:00Z

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

Produced by the NASA Center for Aerospace Information (CASI)

ACCELERATED LIFE TESTING EFFECTS ON CMOS MICROCIRCUIT CHARACTERISTICS

Phase IV Report

November 1977 to April 1979

JUNE 1979

(NASA-CR-161282) ACCELERATED LIFE TESTING EFFECTS ON CMOS MICROCIRCUIT CHARACTERISTICS Technical Report, Nov. 1977 - Apr. 1979 (RCA Solid State Div., Somerville, N.J.) 16 p HC A02/MF A01 CSCL 09C G3/33

N79-29433

Unclas

31738

Prepared By

RCA, SOLID STATE DIVISION

Somerville, New Jersey

Prepared for

GEORGE C. MARSHALL SPACE FLIGHT CENTER

MARSHALL SPACE FLIGHT CENTER

ALABAMA 35812

TABLE OF CONTENTS

Section		Page
I	INTRODUCTION	1
II	OBJECTIVES	1
III	THE PROCESS	2
IV	DEVICE SELECTION	2
V	DEVICE FABRICATION	5
VI	TEST AND EVALUATION	5
VII	TEST RESULTS	10
VIII	CONCLUSION	13

LIST OF ILLUSTRATIONS

Figure		Page
1	Deposition of layers on p-channel transistor.	3
2	CMOS dual complementary pair plus inverter, CD4007A. . . .	4
3	Experimental cell matrix.	6
4	Burn-in pin connections.	8
5	Testing and evaluation of each cell.	9

LIST OF TABLES

Table		Page
I	Test Results of Cells No. 1 Through 8, Number of Out-of-Specification Devices	11
II	Test Results of Cells No. 10 and 11	14

ACCELERATED LIFE TESTING EFFECTS ON
CMOS MICROCIRCUIT CHARACTERISTICS

PHASE IV REPORT

CONTRACT NAS8-31905

I. INTRODUCTION

The results of Phase I and Phase II of this contract (250°C and 200°C accelerated tests) as well as work done by RCA's various activities in the field of reliability improvement suggest that reduced longevity of the CMOS microcircuits under high-temperature accelerated testing is primarily due to contaminants external to the chip. The presence of small amounts of moisture enhances the mobility of the contaminant ions, thereby contributing to increased leakage currents and changes in other device characteristics, such as threshold and output voltage, under the high-temperature accelerated testing. Phase IV introduces modifications and additions to the present process of making CMOS microcircuits which are designed to provide protective layers on the chip to guard against moisture and contaminants.

II. OBJECTIVES

Phase IV of this contract has the following objectives:

1. The improvement of the Class A CMOS microcircuit high-temperature accelerated-test characteristics through deposition of silicon nitride protect layers.
2. The selection of the optimum process for further evaluation under high-temperature accelerated-test conditions.

III. THE PROCESS

The standard wafer-manufacturing process was modified by the introduction of two distinctly different silicon nitride (Si_3N_4) protect layers. These two kinds of Si_3N_4 layers are distinguished by the method of deposition and, therefore, resultant characteristics.

The high-temperature Si_3N_4 layer is deposited in a furnace at 800°C. This method of deposition results in a dense layer which is impervious to contaminants, has a slow etch rate, and which provides a good barrier to sodium. The deposition of the layer over the field oxide presents few problems. When the layer is deposited over the channel oxide, its thickness must be minimized (175 - 200Å) to prevent the formation of a metal-to-channel oxide interface and the possibility of accumulation of undesirable charges. Fig. 1(c) shows the location of this layer.

The low temperature Si_3N_4 layer is plasma deposited after the metallization, at 310°C, a temperature low enough to prevent alloying of aluminum metal into the silicon. This type of deposition results in a less dense layer with a higher etch rate. The layer is deposited over the entire chip and is made relatively thick (3kÅ to 10kÅ) in an attempt to make it impervious to contaminants, Figs. 1(b) and (c). The PSG (phosphorous silica glass) layer standard in current RCA processing is retained with the idea that it may still serve the useful function of gettering for those contaminants that might be trapped under the protect layer.

VI. DEVICE SELECTION

The simplicity of the CD4007A device type was the compelling reason for choosing it as the vehicle for this experiment. A wealth of life-test information is also available for this device type. The schematic diagram of Fig. 2 shows the internal connections of the CD4007A; the easy accessability to individual transistors should greatly facilitate the analysis of failures resulting from subsequent testing and evaluation.

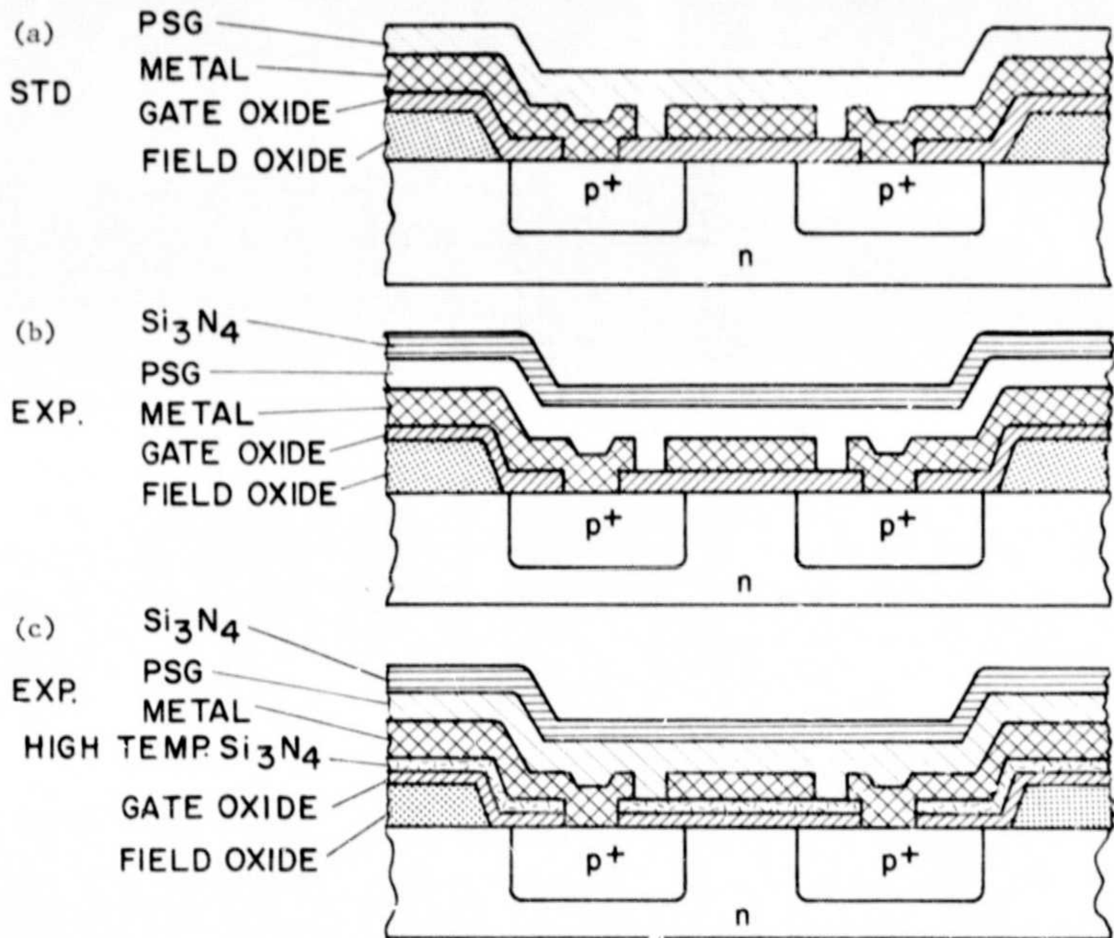

Fig. 1 - Deposition of layers on p-channel transistor.

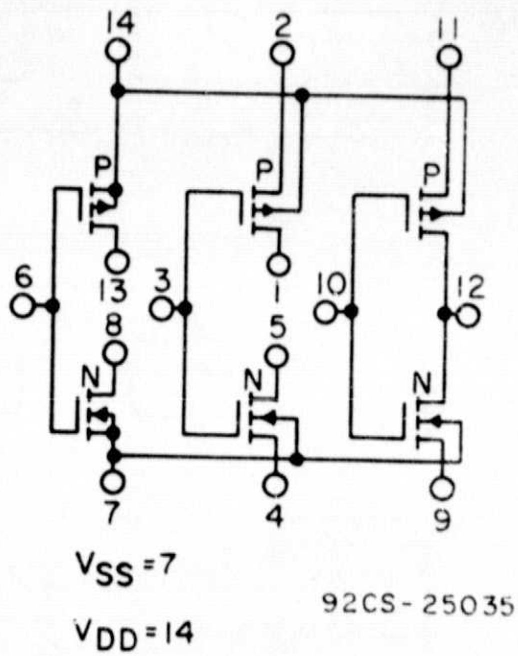

Fig. 2 - CMOS dual complementary pair plus inverter, CD4007A.

V. DEVICE FABRICATION

The experimental cell matrix was developed as shown in Fig. 3. Twenty-four wafers were processed by means of the standard RCA process for fabricating commercial CMOS IC's through channel-oxide deposition. At this point, the lot was split as shown on the matrix of Fig. 3, into one control cell (No. 1) and seven (Nos. 2 through 8) test cells. The seven test cells represent the low-temperature deposition of Si_3N_4 to various thicknesses in combination with (Group I) the high-temperature Si_3N_4 layer or without (Group II) the high-temperature Si_3N_4 layer.

The wafers were circuit probed with high resultant yields, which is a good indicator of the manufacturability of the process. For comparison, the circuit probe yields for the CD4007A were:

For the 1977 year, 80 to 85%
For the Si_3N_4 experiment, 82%

The control cell (No. 1) and the test cells (Nos. 2 through 8) were assembled in standard plastic dual-in-line packages. The pellets were mounted with epoxy used in the RCA CD4000 commercial series. The Novolac plastic package is thought to accentuate problems that might be encountered in subsequent testing, thereby reducing the duration of tests. The assembled devices were screened to commercial specifications to net 60 good devices per cell for further evaluation.

The devices in test cells Nos. 9, 10 and 11 were to be eutectically mounted in ceramic (DIC) packages so that they could be tested under high-temperature accelerated-test conditions. These three cells represent those test cells appearing as the last line in the experiment matrix of Fig. 3.

VI. TEST AND EVALUATION

The evaluation of the effectiveness of the Si_3N_4 protect layers as the barriers to contaminants required the type of testing that provides sufficient

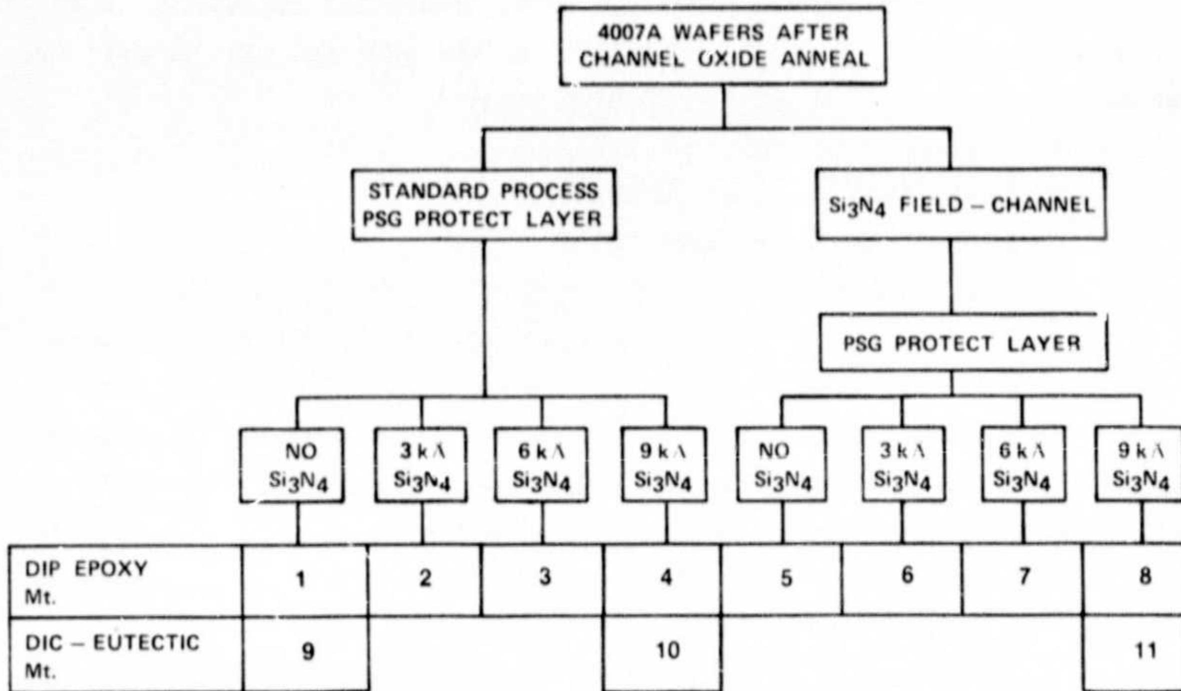

Fig. 3 - Experimental cell matrix.

stressing, particularly in two areas: the high-temperature and high-humidity environment. Three tests were used to achieve this type of stress:

1. 200°C bias/temperature test
2. 150°C bias/temperature test
3. 85°C/85% relative-humidity, bias/humidity test.

All tests were conducted at 12.5 V dc. The circuit bias arrangement used was the standard burn-in bias configuration shown in Fig. 4. Each test cell from No. 1 to No. 8 was tested in accordance with the schedule of Fig. 5. The electrical measurements were taken initially and at each down-time as indicated for tests 1, 2, and 3. The anticipated end-of-test time for each test is also shown in Fig. 5 as the last down-time.

It was thought, from experience, that all test cells would have generated a sufficient number of out-of-specification devices at each end-of-test time to provide the basis for comparison among the test cells. However, it was found during the actual testing that the longevity of the test devices was underestimated. Neither 240 hours at 200°C nor 1152 hours at 150°C were producing enough out-of-specification devices for conclusive evaluation. Because of time and equipment limitations it was then decided to continue beyond the anticipated end-of-test time with the 200°C bias-temperature test only. The 200°C test in actuality had to be extended to 500 hours and eventually to 768 hours before a conclusive evaluation could be done.

The test parameters and the limits used were those of the standard commercial device specifications. The use of specifications more relaxed than those of the MIL-M-38510 commercial specifications was dictated by the need to detect gross differences among the test cells rather than differences resulting from subtle process variations.

One group of devices was evaluated in an entirely different way. These devices were assembled in ceramic packages with eutectic mounts and tested with a 200°C bias/temperature test. These devices were represented by the

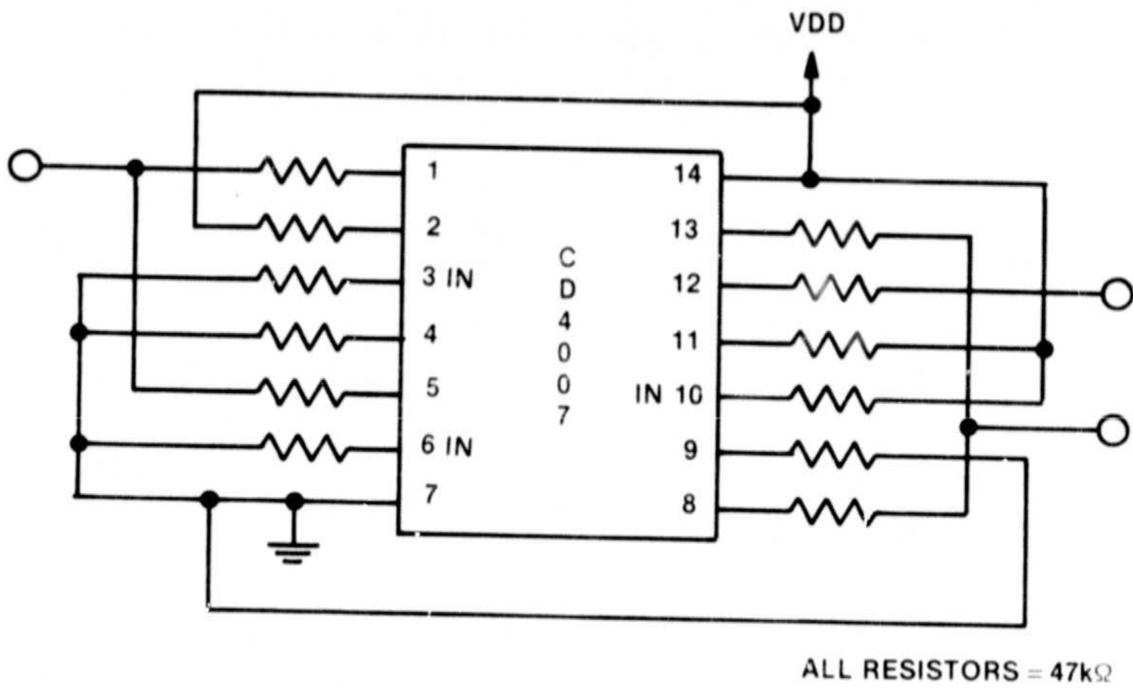

Fig. 4 - Burn-in connections.

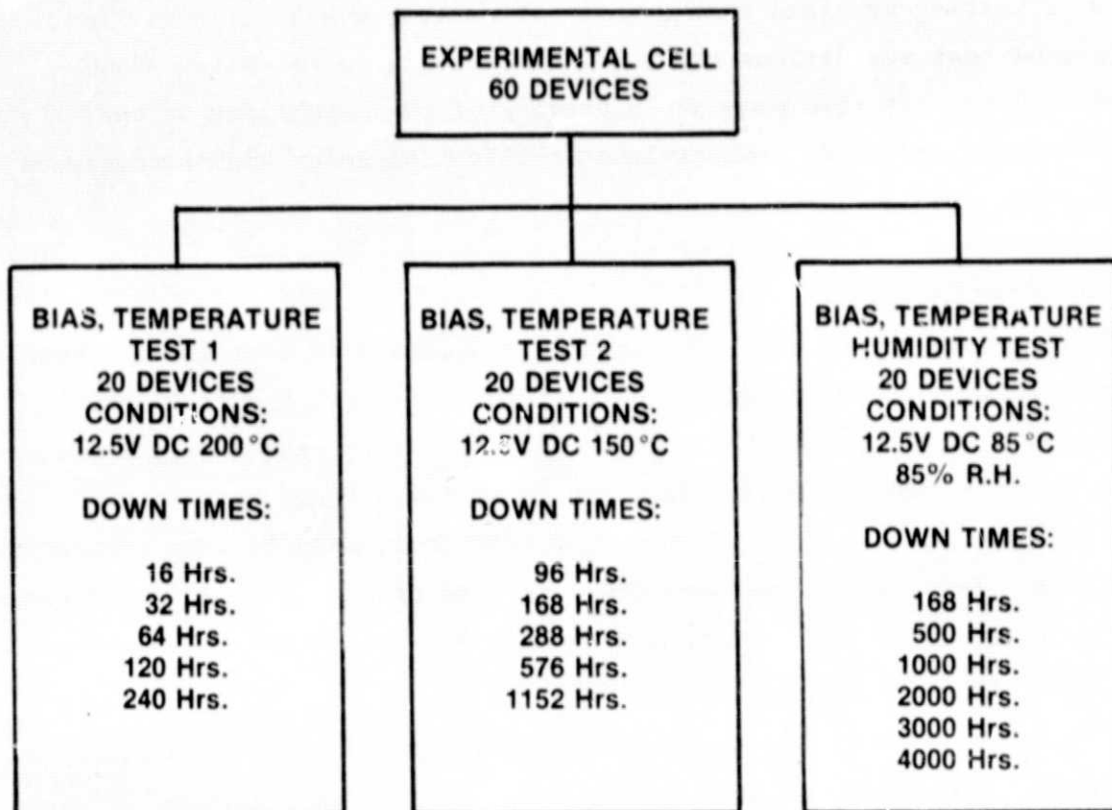

Fig. 5 - Testing and evaluation of each cell.

three test cells Nos. 9, 10, and 11. Test-cell No. 10 had the low temperature Si_3N_4 layer only while test-cell No. 11 had both the low-temperature and the high-temperature Si_3N_4 layers. Test cell No. 9 was accidentally lost during handling.

The electrical measurements on this group of devices were performed by using the test programs based on the MIL-M-38510 detail specifications. This method of testing provided test results directly comparable to earlier accelerated-test evaluations of CMOS microcircuits to the MIL-M-38510 specifications. It also provided a preview of the capability of the eutectic-mount and Si_3N_4 protect-layer combination under high-temperature accelerated-test conditions.

VII TEST RESULTS

The test matrix in this experiment was designed so that the analysis of the test results could be conducted in steps. At first a determination must be made as to whether there is an improvement in either of the two test groups over the control cell. If there is an improvement in more than one cell, a comparative evaluation among the test cells must be made to determine which of the test cells possesses the best characteristics. The improvement must be demonstrated in both the high-temperature and high-humidity environments. The test results are summarized in Table I.

The 150°C bias/temperature test can be eliminated from consideration immediately because the control cell has not produced a single out-of-specification device in this test. The results of the other two tests, the 200°C bias/temperature and the 85°C/85% relative-humidity tests, can be analysed by the application of the three regions in the life of a device: The "infant-mortality" region, the "constant-failure-rate" region, and the "wear-out" region.

None of the test devices has been burned-in; consequently, the devices which exceeded the specification limits during the first 16 hours in the 200°C test as well as the out-of-specification devices occurring within the first 168 hours in the 85°C/85% relative-humidity test could be attributed to the infant mortality. The constant-failure-rate region appears to fall between the 16-hour point and the 500-hour point in the 200°C test. At the 500-hour point, devices begin exceeding the specification limits in numerous cells,

Table I - Test Result of Cells No. 1 Through 8; Number of Out-of-Specification Devices

Test Description	Cell No.	Standard Process With Low Temp. Si_3N_4 1	2	3	4	High Temp. Si_3N_4 Layer With Low Temp. Si_3N_4 5	6	7	8
	Si_3N_4 Thickness	0A	3kA	6kA	9kA	0A	3kA	6kA	9kA
	Sample Size	20	20	20	18	20	20	20	19
	Downtime Hours								
200°C Bias/Temperature Test	16	0	0	0	2	0	0	0	0
	32	0	0	0	0	0	0	0	0
	64	0	0	2	0	0	0	0	0
	120	0	0	1	0	0	0	0	1
	240	0	0	0	0	0	0	0	0
	500	1	0	4	0	8	0	5	3
	768	14	18	10	16	12	17	12	12
	Cumulative	15	18	17	18	20	17	17	16
	Sample Size	20	20	20	20	18	19	16	20
	Downtime Hours								
150°C Bias/Temperature Test	96	0	0	0	0	1	1	2	0
	168	0	0	0	0	0	0	0	0
	288	0	1	0	0	0	0	0	0
	576	0	0	1	0	0	0	1	0
	1152	0	0	1	0	0	0	0	0
	Cumulative	0	1	2	0	1	1	3	0
	Sample Size	19	20	20	20	19	20	18	20
	Downtime Hours								
85°C/85% R.H. Bias/Humidity Test	168	1	0	0	0	0	0	0	0
	500	0	0	0	0	1	0	0	0
	1000	0	0	1	0	0	0	0	0
	2000	0	2	0	0	2	0	0	0
	3000	0	1	0	0	3	1	2	3
	4000	5	7	1	1	1	6	0	1
	Cumulative	6	10	2	1	7	7	2	4

an indication of the onset of the wear-out region. The test data at 768 hours clearly indicates that the wear-out region for all the cells has been reached before that time. Because of the absence of out-of-specification devices in the control cell within the constant-failure-rate region, the wear-out region must be used as the criterion for comparative evaluation of cells. By using that criterion, cells 2, 4, and 6 appear as having demonstrated characteristics equal to or better than those of the control cell. None of these cells has had an out-of-specification device in the constant-failure-rate region, up to and including the 500-hour point. The two out-of-specification devices in cell No. 4 are attributed to infant mortality. The control cell had an out-of-specification device at the 768-hour point. The wear-out region for these test cells lies somewhere between 500 hours and 768 hours. The rate of deterioration for the devices in this region is probably similar for all cells, as can be judged by the recorded number of out-of-specification devices at the 768-hour point.

Similarly, the onset of the wear-out region in the 85°C/85% relative-humidity test, at least for some cells, is evidenced at the 4000-hour point. From among the test cells identified earlier, only cell No. 4 remains in the contest with the control cell because of the condition that a cell must demonstrate improvement in both the 200°C and the 85°C/85% relative-humidity test to be in contention. At the 4000-hour point cell No. 4 has had one out-of-specification device versus five such devices (exclusive of one early out-of-specification device) in the control cell. This result tends to indicate the possibility that the heavy coat (9kÅ) of low-temperature Si_3N_4 is presenting a barrier to moisture. The group with two Si_3N_4 layers did not do as well, in general, suggesting that perhaps the technique of depositing the thin high-temperature Si_3N_4 layer may need further perfecting.

Test cells No. 10 and 11 were tested at 200°C and evaluated to the MIL-M-38510 detail specifications. At the 16-hour down time, both test cells had produced devices out of specification in leakage (I_{SS}); test cell No. 11 has had decreasing threshold voltage (V_{TH}) in addition to out-of-specification leakage (I_{SS}).

Table II summarizes the number and kind of out-of-specification devices which occurred in test cells No. 10 and 11. The threshold problems have occurred in the same devices that failed leakage tests. The early problems of the kind that were observed indicated the possible presence of mobile ions. This possibility was checked in both test cells by baking devices at 150°C for 24 hours. A complete recovery in some cases and partial recovery in many others was observed. The bias/temperature test was repeated for another 16 hours, and a recurrence of excessive I_{SS} and V_{TH} problems was observed. The threshold deterioration in test cell No. 11, which has both Si_3N_4 layers, is further evidence that there may have been a problem in the deposition of the high-temperature Si_3N_4 layer. The results of this testing do not compare favorably with the results of tests conducted in Phase II of this contract on CD4011A, CD4013A, and CD4024A devices.

CONCLUSION

The results of the evaluation of the high-temperature and low-temperature Si_3N_4 protect layers conducted within the scope of this effort lead to the following conclusions:

1. The application of the Si_3N_4 layers in all of the tested combinations failed to lead to a demonstrably conclusive improvement in device reliability characteristics.

2. There is some evidence that a heavy (9kÅ) layer of low-temperature Si_3N_4 presents a barrier to moisture. A further, more detailed study is required for a more conclusive statement.

3. The testing of eutectically mounted devices has not produced a desirable degree of improvement in reliability characteristics.

Table II - Test Results, Cells No. 10 and 11

Cell No.	Sample Size	No. & Type of Failure I_{SS}	V_{TH}
10	20	8	-
11	20	15	9