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DEVICE MODEL FOR FETSIM CIRCUIT SIMULATION PROGRAM

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STANDARD ABBREVIATIONS

Symbol	Definition
s	second
m	meter
l	liter
g	gram
V	volt
A	ampere
K	kelvin
Hz	hertz
cm^3	cubic centimeter
min	minute
in.	inch
mil	10^{-3} inch
C	Celsius
k	kilo, 10^3
M	mega, 10^6
c	centi, 10^{-2}
m	milli, 10^{-3}
μ	micro, 10^{-6}
n	nano, 10^{-9}

NONSTANDARD ABBREVIATIONS

Symbol	Definition
PMOS	P-channel Metal Oxide Semiconductor
IC	Integrated Circuit
MSFC	George C. Marshall Space Flight Center
NASA	National Aeronautics and Space Administration

NONSTANDARD ABBREVIATIONS (Concluded)

Symbol	Definition
LSI	Large Scale Integration
LSIC	Large Scale Integrated Circuit
MSI	Medium Scale Integration
MSIC	Medium Scale Integrated Circuit
SSI	Small Scale Integration
SSIC	Small Scale Integrated Circuit
CAD	Computer Aided Design
FETSIM	MOS circuit simulation computer program
MOS	Metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
SOS	Silicon on sapphire

LIST OF SYMBOLS

Symbol	Definition
V_G	Gate voltage
V_T	Threshold voltage
V_{Tn}	Threshold voltage for n devices
V_{Tp}	Threshold voltage for p devices
V_{TH}	Effective threshold voltage; this term accounts for the gating effect.
V_D	Drain voltage
V_S	Source voltage
V_{DS}	Drain-to-source voltage
V_{SAT}	Saturation voltage
I_{DS}	Drain-to-source current
$\phi_{n,p}$	A constant which is a function of the MOS fabrication process (n for NMOS devices; p for PMOS devices).

LIST OF SYMBOLS (Concluded)

Symbol	Definition
$K_{n,p}$	Channel conductance of MOS devices (n for NMOS devices; p for PMOS devices).
ϕ_F	Fermi potential of the substrate
T_{ox}	Thickness of gate oxide
E_{ox}	Dielectric permittivity of gate oxide (silicon dioxide)
Q	Charge on an electron
E_s	Dielectric permittivity of channel region (silicon)
N_A	Channel doping level concentration for n devices (acceptors)
N_D	Channel doping level concentration for p devices (donors)
μ_n	Channel mobility of electrons
μ_p	Channel mobility of holes
$MOVA_{n,p}$	An empirically determined factor which accounts for the mobility variation as a function of gate voltage.
W	Effective channel width
L	Effective channel length
$a_{n,p}$	An empirically calculated factor which accounts for the finite slope of the drain characteristics in the saturation region (n for NMOS devices; p for PMOS devices).
R	Electrical resistance
p	Refers to p-device type
n	Refers to n-device type
Du	Lateral diffusion
T_s	Thickness of sapphire
I_{DO}	Channel leakage
C_{ox}	Poly-over-epi capacitance
C_{mp}	Metal-over-poly capacitance
BV_{DS}	Breakdown voltage (measured between drain and source)

Section I

INTRODUCTION

The information presented in this report includes a description of the MOS transistor model used in the FETSIM analysis program. CMOS/SOS device parameters are included. Typical device mobilities are given as well as the empirically determined constants necessary to model second-order effect conductance variations due to gate voltage and saturated drain voltage.

Section II

FETSIM MOS MODEL

The MOS model used in the FETSIM circuit analysis program is based on a derivation following that of Ihantola.[1] By considering the doping level(s) of the ionized acceptors (or donors) in the substrate material, several second-order physical effects are implicitly accounted for. These include the apparent decreased carrier mobility resulting from heavy substrate doping and the gating effect associated with stacked devices.

A linearized empirical approach[2] is utilized as a means of handling the finite drain conductances in the saturation region. In addition, surface channel mobility modulation, as a function of gate voltage, is modeled along the lines proposed by Schrieffer.[3]

The resulting four-terminal, MOS-device model is ideally suited for large-signal analysis and is directly applicable to either bulk MOS calculations or dielectrically isolated device (SOS) calculations.

Essentially the model divides MOS transistor operation into one of three possible cases.

<u>CASE I:</u> $\left|V_G\right| < \left|V_T\right| \qquad \left|V_G\right| < \left|V_{TH}\right|$

$$I_{DS} = 0$$

Case I is the trivial case; here the magnitude of the gate voltage is below the effective threshold voltage necessary to cause transistor conduction. In this case the device current is zero.

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1. H.K.J. Ihantola, "Design Theory of a Surface Field Effect Transistor," Solid State Electron., vol. 7, pp. 423-430, June 1964.

2. S.R. Hofstein, Field Effect Transistors, Ed. by J.T. Wallmark and H. Johnson, Prentice-Hall, Englewood Cliffs, New Jersey, 1966.

3. J.R. Schrieffer, "Effective Carrier Mobility in Surface-Space Charge Layers," Physical Review, February 1955.

CASE II: $|V_G| > |V_T|$ $|V_D| < |V_{SAT}|$

All SOS Devices or Bulk Devices when source and substrate common

$$I_D = K \left\{ 2V_{DS}(V_{GS}-V_T) - V_{DS}^2 - (4/3)\phi_n (V_{DS} + 2\phi_F)^{3/2} \right\} (1 + aV_{DS})$$

Case II handles the special case of a conducting transistor with its source and substrate electrically connected. The expression for the channel current contains three terms - the first two of which are those found in the generally accepted model of Sah.[4] The third term, $(4/3)\phi_n (V_{DS} + 2\phi_F)^{3/2}$, introduces the effect of the substrate doping level. (The expressions for ϕ, K, V_{TH}, V_{SAT}, and α can be found in Table 1). It is this term that accounts for the reduced effective mobility associated with highly doped MOS substrates. The $(1 + \alpha V_{DS})$ factor accounts for the finite slope of the drain characteristics in the saturation region. SOS devices are always handled with CASE I and CASE II.

CASE III: $|V_{GS}| > |V_{TH}|$ $|V_D| \leq |V_{SAT}|$ $|V_S| \leq |V_{SAT}|$

All Bulk devices where source and substrate are <u>not</u> connected

$$I_D = K \left\{ 2(V_G-V_T)(V_D-V_S) - (V_D^2-V_S^2) - (4/3)\phi_n \left[(V_D + 2\phi_F)^{3/2} - (V_S+2\phi_F)^{3/2} \right] \right\} (1 + aV_{DS})$$

Note: V_G, V_D, & V_S are measured relative to the substrate.

Case III covers the generalized and more complicated case where neither the source nor the drain is connected to the substrate. (When either the source or the drain is connected to the substrate, Case III reduces to Case II.)

Case III permits the accurate handling of "stacked" transistors (for example, three input NOR gates). Generally, this case applies to bulk devices only. However, it is used in SOS calculations whenever device substrates are not permitted to "float".

The model is programmed in such a way as to set $V_D=V_{SAT}$ whenever $V_D \geq V_G - V_{TH}$, and $V_S = V_{SAT}$ whenever $V_S \geq V_G - V_{TH}$.

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4. C.T. Sah, "Characteristics of Metal-Oxide-Semiconductor Transistors," <u>IEEE Transactions on Electron Devices</u>, July 1964, pp. 324-325.

TABLE 1. MOS MODEL CONSTANTS

Symbol	Value	Comments
$\phi_{n,p}$	$\frac{T_{ox}}{E_{ox}} \sqrt{2E_S Q N_{A,D}}$	A constant which is a function of the MOS fabrication process.
K	$K_n = \frac{\mu_n}{1+MOVA_n (V_G-V_S-V_T)} \frac{E_{ox} W}{2T_{ox} L}$ $K_p = \frac{\mu_p}{1+MOVA_p (V_G-V_S-V_T)} \frac{E_{ox} W}{2T_{ox} L}$	
V_{TH}	$V_T \pm \phi_{n,p} \sqrt{V_S + 2\phi_F}$	The sign is "+" for enhancement mode NMOS transistors. This term accounts for the gating effect.
$\alpha_{n,p}$	Typical Values $\alpha_n = 0.01$ $\alpha_p = 0.02$	This is an empirically calculated factor which accounts for the finite slope of the drain characteristics in the saturation region.
V_{SAT}	$-2\phi_F + \left[-\frac{\phi_{n,p}}{2} + \sqrt{\left(\frac{\phi_{n,p}}{2}\right)^2 + 2\phi_F + V_G - V_T}\right]^2$	
ϕ_F	$0.026 \log \left(\frac{N_{A,D}}{1.45 \times 10^{10}}\right)$	The Fermi potential of the substrate.

TABLE 1. MOS MODEL CONSTANTS (Continued)

Symbol	Value	Comments
	Typical Value	
$MOVA_{n,p}$	0.03	This is an empirically determined factor, which accounts for the mobility variation as a function of gate voltage.
W, L		Effective channel width and channel length.
Q	0.16×10^{-18}	Charge on an electron, in coulombs.

The programming technique permits saturated transistors and the gating effect to be handled.

MOS transistors processed in a bulk LSI technology share a common substrate. Generally NMOS devices are fabricated within a common p-well while PMOS devices are fabricated within a common n-type material. Inherent in this scheme is the possibility that the sources and drains of "stacked" transistors (in functional gates and transmission gates) can become back biased with respect to the fixed potential of the common substrates. This "gating effect" gives rise to an apparent increase in the threshold voltages of the associated transistors. This phenomenon is modeled in the equations of CASE III.

In comparison, MOS transistors processed in one of the SOS LSI technologies are fabricated within separate, independent islands of substrate material. This technique leaves the channel material free to be defined by the source or drain potentials of each transistor. In the case of NMOS devices, the p-type channel material is defined by the source or drain — whichever is at the lower potential. Similarly for PMOS devices, the n-type channel material is defined by the source or drain, whichever is the higher potential. This phenomenon is modeled by automatically defining the substrate of each SOS-LSI transistor to be at the lowest of the source or drain potentials for n-devices and highest of the source or drain potentials for p-devices. When this is done, the more generalized CASE III reduces to CASE II.

A nominal set of parameter values that is applicable for the current CMOS/SOS processes available at the RCA Solid State Technology Center is shown in Table 2. From the channel conductance values listed, typical mobility values can be calculated. For example,

$$\mu_n = \frac{K_n (2\, T_{ox})}{E_{ox}} = 319 \text{ cm}^2/\text{volt-second}$$

$$\mu_p = 191 \text{ cm}^2/\text{volt-second.}$$

Using the typical device parameters listed in Table 2, the FETSIM model calculates saturated device currents (at 10 volts) of 1.2 and 0.8 mA for the n and p transistors, respectively. These currents are based on an assumed device width of 1.0 mil. The mobilities used for the calculation are 319 and 191 cm^2/volt-second for the n and p devices, respectively. In addition, the mobility modulation terms $MOVA_{n,p}$ were assumed to be 0.

When it becomes necessary to model the effects of mobility variation as a function of gate voltage, the $MOVA_{n,p}$ terms must be chosen to match the observed mobility modulation phenomenon. The empirical data will be a function of the particular

TABLE 2. CMOS/SOS DEVICE PARAMETERS

Parameter	Symbol	Units or Test Conditions	Min.	Typical	Max.
Threshold voltage	V_{Tn}	$V_D = V_G$, $I_D = 10\ \mu A$ T = 25°C, w = 2.0 mils	0.5		2.5
Threshold voltage	V_{Tp}	$V_D = V_G$, $I_D = 10\ \mu A$ T = 25°C, w = 2.0 mils	-0.5		-2.5
Channel conductance	K_n	$K = \frac{\mu E_{ox}}{2 T_{ox}} AV^2 (x 10^{-6})$		5.0	
	K_p	$K \frac{\mu E_{ox}}{2 T_{ox}} AV^2 (x 10^{-6})$		3.0	
Breakdown voltage	BV_{DSp}	$I_D = 10 \mu A$, $V_G = 0$ V	20	23	
	BV_{DSn}	$I_D = -10 \mu A$, $V_G = 0$ V	-20	-30	
Dielectric constant	E_{ox}	0.885×10^{-13} F/cm	3.9	3.9	
Oxide thickness	T_{ox}	Channel Å	1000	1100	1200
	T_{ox}	Field Å	6000	7000	8000
Channel length	l	As defined in mils		0.25 0.30	
Lateral diffusion	Du_n	mils		0.03	
	Du_p	mils		0.03	
Sapphire thickness	T_s	mils		14	
Metal-to-metal spacing		mils		0.3	
Metal-to-diffused region spacing		mils		0.1	
Metal thickness	T_{Al}	Å	10,000		
Metal width		mils		0.4	
Diffused-region to diffused-region spacing		mils		0.2	
N-epi doping		$(X\ 10^{15}\ cm^{-3})$		2	
P-epi doping		$(X\ 10^{15}\ cm^{-3})$		3	
N+ epi resistance	R	ohms/square		85	
P+ epi resistance	R	ohms/square		65	
N+ poly resistance	R	ohms/square		200	
P+ poly resistance	R	ohms/square		70	
Channel leakage	I_{DOn}	$V_G = 0$ nA/mil		10	25
Channel leakage	I_{DOp}	$V_G = 0$ nA/mil		10	25
Body region tie		Floating			
Poly-over-epi capacitance	C_{ox}	pF/square		0.28	
Metal-over-poly capacitance	C_{mp}	pF/square		0.076	

process under examination. Generally the $MOVA_{n,p}$ terms may be set equal to each other ($MOVA_n = MOVA_p$). Measured conductances for both the bulk and SOS technologies suggest a typical mobility reduction of 20 percent over a 10-volt operating range. Specifically, the mobility at V_G = 10 volts is reduced to 80 percent of its value measured at the onset of conduction ($V_G = V_T$). To model this mobility variation, the MOVA terms should be set equal to 0.030 ($MOVA_n = MOVA_p$ = 0.03). It is important to note, however, that whenever finite MOVA terms are introduced, the mobility terms used with the model must be artificially increased to guarantee correct scaling. For example, fixed electron mobilities of 319 cm^2/volt-second would appear as 319 cm^2/volt-second at $V_G = V_T$ and as 246 cm^2/volt-second at V_G = 10 volts.

Section III

CONCLUSION

The FETSIM MOS transistor model has been described. The means by which this model handles both SOS and bulk transistor devices has been discussed. In addition, a complete set of typical processing and empirically derived model constants has also been provided.

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16. ABSTRACT

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17. KEY WORDS

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