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Low-Cost Solar Array Project

5101-104

DOE/JPL-1012-7
Distribution Category UC-63b

LSA Project Technology Development Update

John V. Goldsmith
Donald B. Bickler

August 30, 1978

Prepared for
U.S. Department of Energy
by
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

(JPL PUBLICATION 79-29)

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ABSTRACT

This document presents copies of the viewgraphs and a condensation of the comments by John V. Goldsmith and Donald B. Bickler of the LSA Project at its 10th Project Integration Meeting, August 16 and 17, 1978, at Caltech University, Pasadena, California. Their presentations focus on the state of the technology aimed at achieving the $500/kW goal by 1986.

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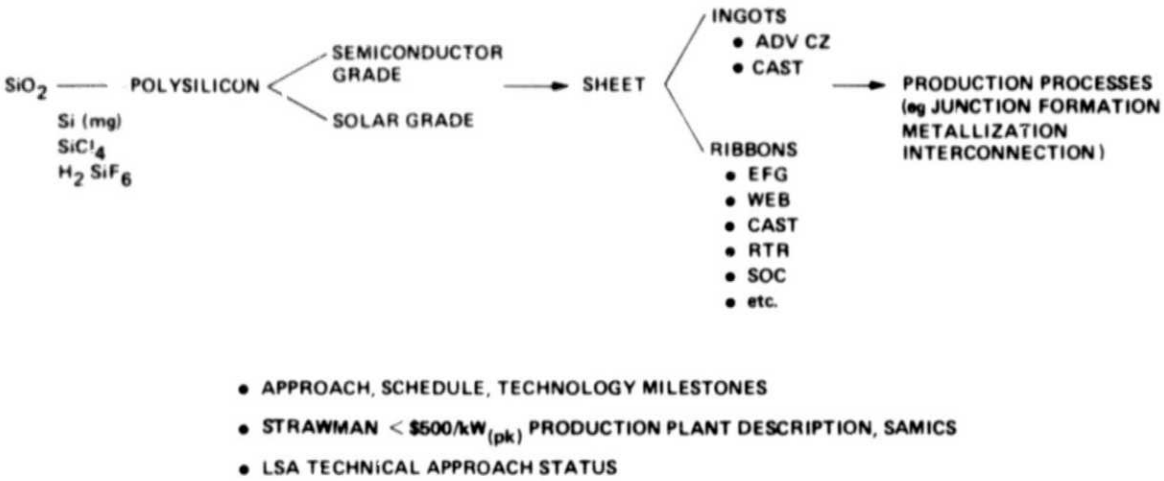


Figure 1

TECHNOLOGY STATUS OVERVIEW

John Goldsmith:

Areas of concern in the LSA Project range from silicon dioxide, through various processes, to the fabrication of solar arrays. The first step is to produce high-purity polysilicon that allows high-efficiency solar cells. Generally, and somewhat arbitrarily, two types of silicon are referred to: semiconductor-grade quality, which is available to the industry today and is normally described as being one part per billion pure; and solar grade, which is less pure than semiconductor grade and therefore not suitable for the entire semiconductor industry but might be very suitable for manufacturing high-efficiency solar cells.

Next is conversion of either one of these two materials into sheets. This can be done by the Czochralski approach, which results in a large diameter cylindrical ingot that is sliced into wafers, or by casting, which also produces wafers, or by some technique associated with growing ribbons. These ribbons or wafers, which can be integrated into a sheet, are processed into a solar array. This operation includes steps to form junctions, to metallize the solar cells and interconnect them, to create a module, to encapsulate it, and then to distribute the modules.

- PROJECT OBJECTIVE: FY86 $500/kW, 500 MW/YR, COMMERCIAL READINESS ACHIEVED
- 5-YEAR OBJECTIVE: FY81 TECHNOLOGY AND ECONOMIC POTENTIAL DEMONSTRATED
- TECHNOLOGY READINESS
- PHASE II COMMERCIAL READINESS

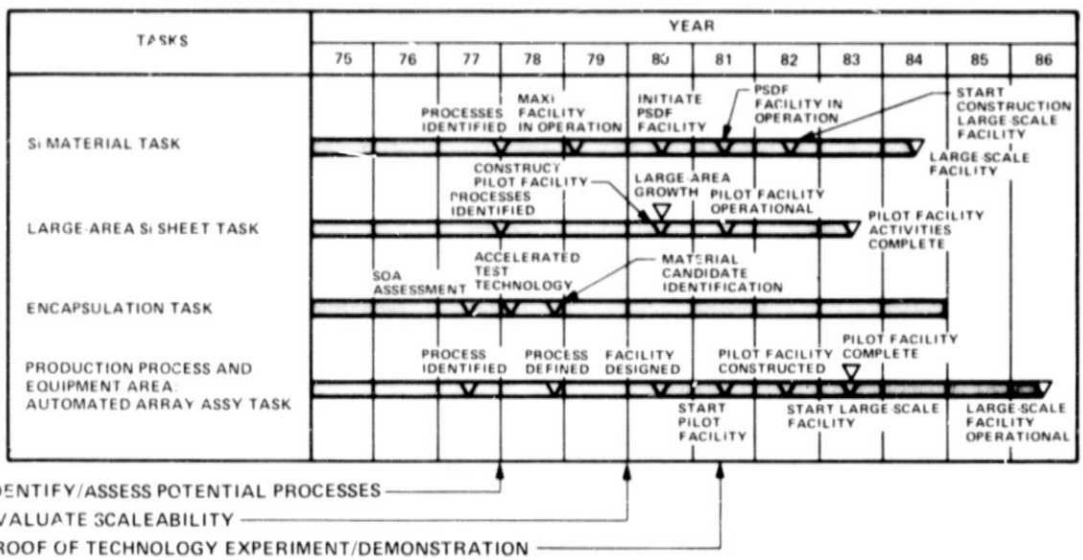


Figure 2

SUMMARY PLAN AND MILESTONES

There is a three to five year span between technology readiness and industrial readiness. The LSA objective is to provide technology readiness five years in advance of the 1986 overall goal; that means technology readiness for silicon solar arrays should be achieved by 1981. To expedite this, the LSA Project is using a parallel approach: developing sheets in parallel with developing polysilicon in parallel with developing encapsulation, etc. These activities must be integrated to make sure that the material from the polysilicon program is compatible with the sheet techniques, and so forth.

As shown in Figure 2, technology readiness demonstration is preceded by scale-up potential evaluation and proof-of-technology demonstration.

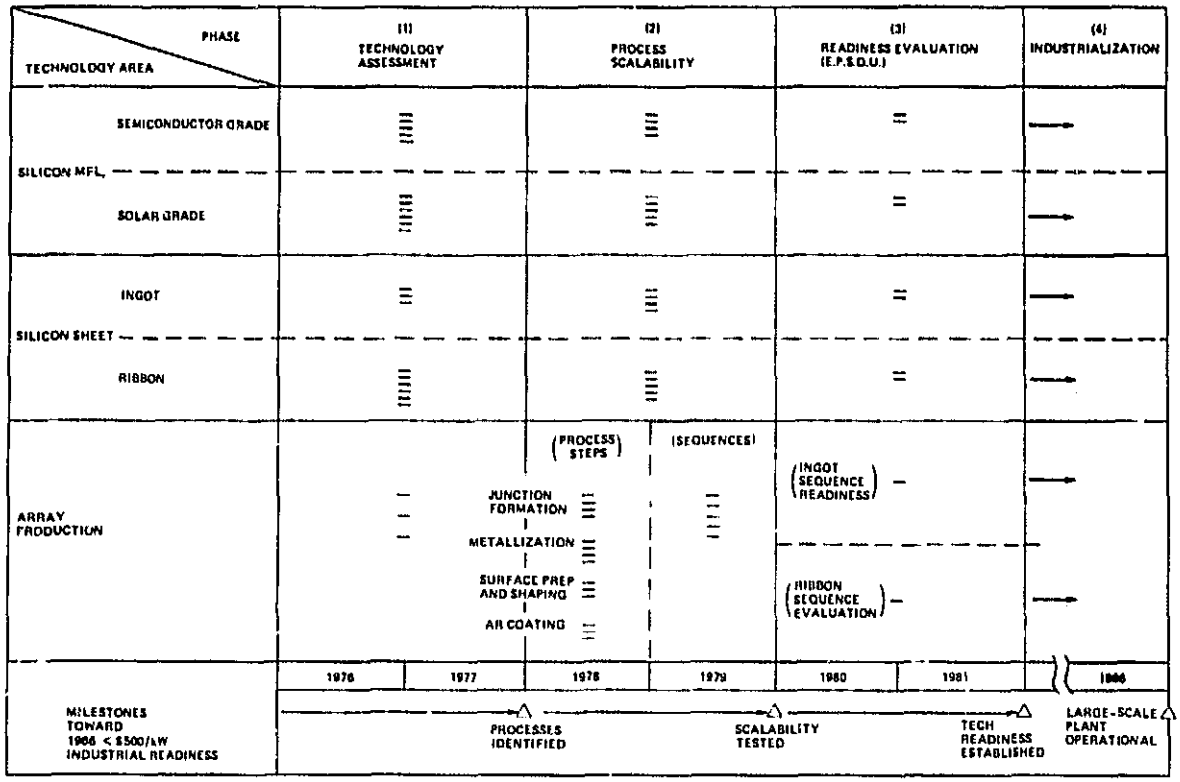


Figure 3

INDUSTRY TECHNOLOGY DEVELOPMENT/COMPETITION

Major milestones in reaching technology readiness in the 1981 period are indicated at the bottom of Figure 3. The 1981 through 1986 period, the industrialization phase, involves large-scale plant development.

Can promising technologies be found within each area to meet the overall goals of the program? For instance, can sheet processes that appear to have an added value cost goal be identified? They cannot cost more than $\$18/m^2$ if they are to be compatible with the overall objective of $50¢/W_{pk}$ or less.

The LSA Project believes it has passed through the technology assessment phase and has identified not one but many viable approaches, and that it is now in the process scalability phase. The number of apparently viable approaches have not greatly diminished; in fact, from the silicon material point of view, it has been encouraging to see that the alternatives seem to be increasing.

The array production area is in a second phase that includes identifying key process steps needed in developing technologies to move from sheets to high-efficiency cells and arrays. In the period from the end of 1978 to the end of 1979, the LSA Project expects to build a sequence to help in understanding how near readiness is for large-scale development.

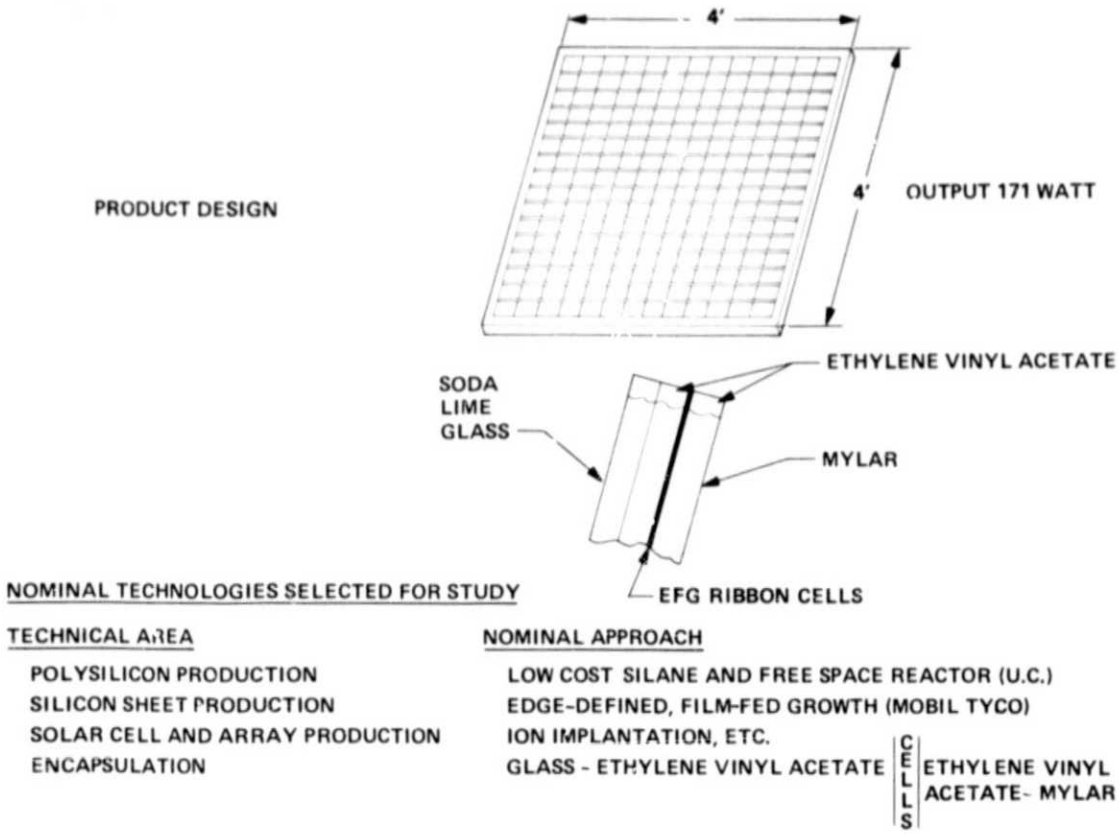


Figure 4

$500/kW$_{pk}$ STRAWMAN FACTORY

Certain technologies have been selected for the strawman to indicate what the 50¢/watt technology might look like. This is not the "JPL approach" or the "LSA Project approach," and does not imply that JPL no longer has interest in other processes.

This strawman is for a factory that will produce one product: a 4x4 ft solar panel based on polysilicon from the Union Carbide approach, which uses low-cost silane and a free-space reactor to make polysilicon that is compatible with the processes associated with growing the ribbons. The sheet production is based on the edge-defined film-fed growth process being pursued by Mobil-Tyco. The junction formation will be through ion implantation, and the encapsulation approach uses glass/ethylene vinyl acetate. The ribbon cells are 75x100 mm with an aluminum metallization system, an EVA back cover, and Mylar vapor barrier. The strawman module produces 171 W, which makes it a nominally 11.4% efficient module. (See Figure 4.)

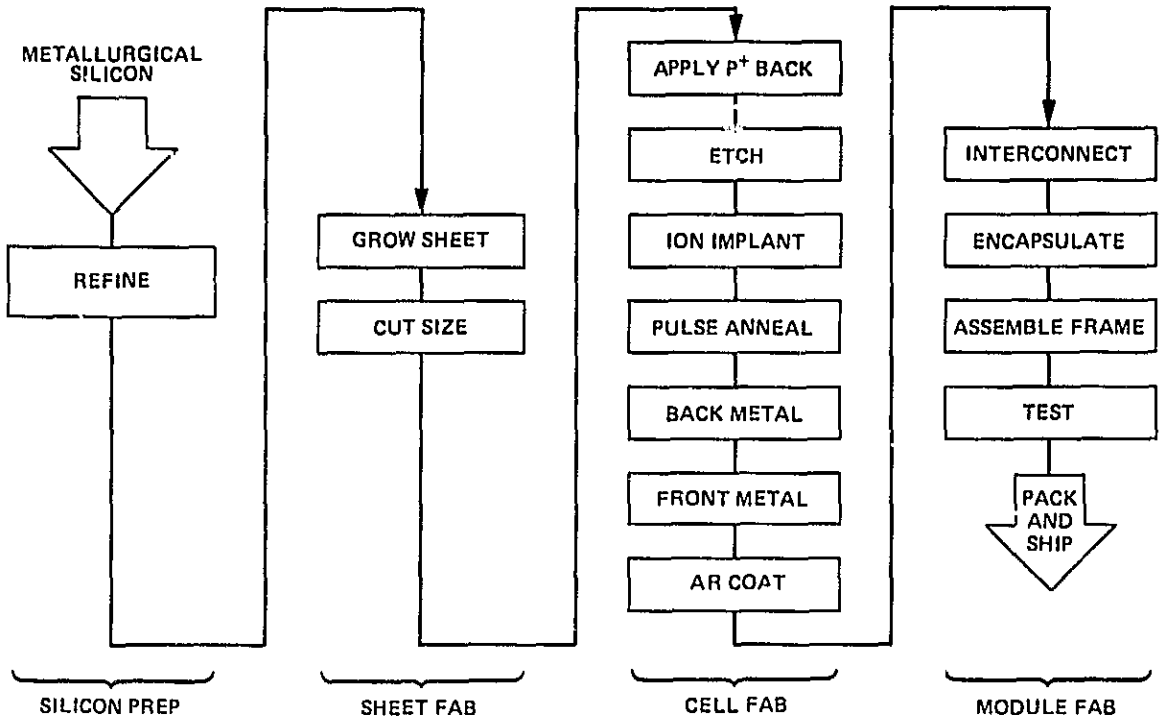


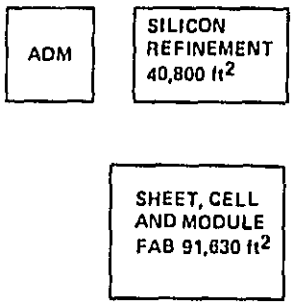
Figure 5

$0.50/WATT CANDIDATE MANUFACTURING SEQUENCE

Donald Bickler:

The cell candidate manufacturing process makes use of a p+ surface that is applied by way of an aluminum powder composition. The etch is simply to remove the oxide. The sequence will ion implant the junction and pulse anneal while still in the vacuum. A grid system with connector pads will be put on the cell backs to reduce electrical resistance. The aluminum p+ is expected to have too high a sheet resistance to be used alone. It may not require as much metallization as has been put in this process, but there is a cost allowance for a thick film back metal grid. After that, a spray-on antireflective coating is applied.

The first step in panel assembly is the interconnecting of 12 cells in parallel using a modified industrial robot-type approach. Ultrasonic bonding of an aluminum interconnect strip to the aluminum back is envisioned, or it could be copper to aluminum, or copper to silver pads. The costs are calculated for the worst case in this regard. These strips are then soldered to the front contact, forming 16 cells in series. The last step is to apply a painted steel frame with gasket.



PRODUCTION RATE	250,000,000 WATTS/YEAR
LABOR FORCE (ALL SHIFTS)	1,152 DIRECT 529 INDIRECT
FACTORY AREA	
SILICON REFINEMENT	40,800 ft²
SHEET GROWTH	19,550
CELL FABRICATION	31,200
MODULE FABRICATION	10,200
WAREHOUSE	9,779
MISC (AISLES, SHOPS, CAFETERIA, ETC.)	20,901
CAPITAL EQUIPMENT	
SILICON REFINEMENT	19,400,000*
SHEET GROWTH	14,820,000
CELL AND MODULE FABRICATION	8,219,000

*UNION CARBIDE

ENERGY PAYBACK TIME SHEET & CELL & MODULE – 0.179 YEARS

Figure 6

$0.50/WATT CANDIDATE PLANT LAYOUT

The silicon refinement building is similar to the model that Union Carbide presented at the 9th PIM. It is 240x170 ft and is set off by itself. The area between buildings is to be composed of lawns and parking lots. Sheet formation, cell and modulation fabrication, with the attending miscellaneous shops (cafeteria, warehouse space, etc.), are in one building, which, according to SAMICS*, will be 91,630 ft^2. "Miscellaneous," listed under "Factory Area," is relatively high because aisles and access space require more than first estimated.

*Solar Array Manufacturing Industry Costing Standards

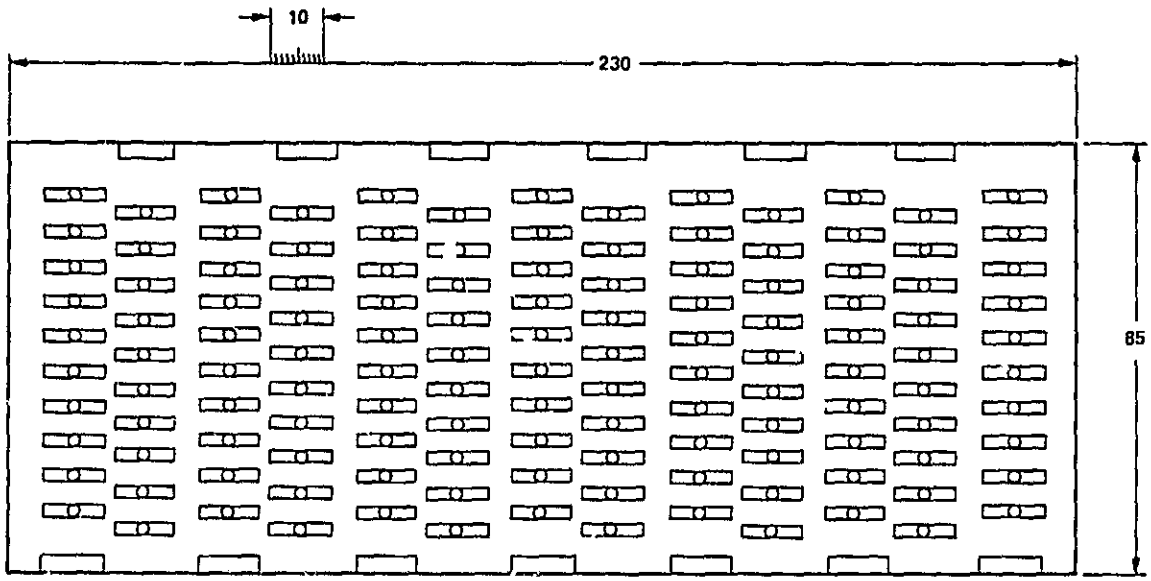


Figure 7

SILICON SHEET GROWTH

The sheet growth area has 130 pairs of ribbon-growing machines. The small circles are melt replenishment vats where the molten silicon is supplied to five ribbon machines on each side. Ten ribbons are simultaneously grown, emerging from the top of an assembly. The machines are spaced for maintenance -- the operators do not need that much space. For maintenance the insides of the machines are drawn out, between their staggered, adjacent neighbors. The ribbons are scribed and cut at the machines and loaded into cassettes. Approximately five sets are grouped to a cassette loader. The entire output of this area is slightly in excess of 30,000 wafers per hour. The output of slices from any one machine is not at a very high speed.

The areas along the wall are maintenance work benches. These are broken into sets of 10 so that one maintenance man and his group of 10 growers function to some extent as an independent unit. Ten operators are in each unit, one operator handling each pair of growing machines.

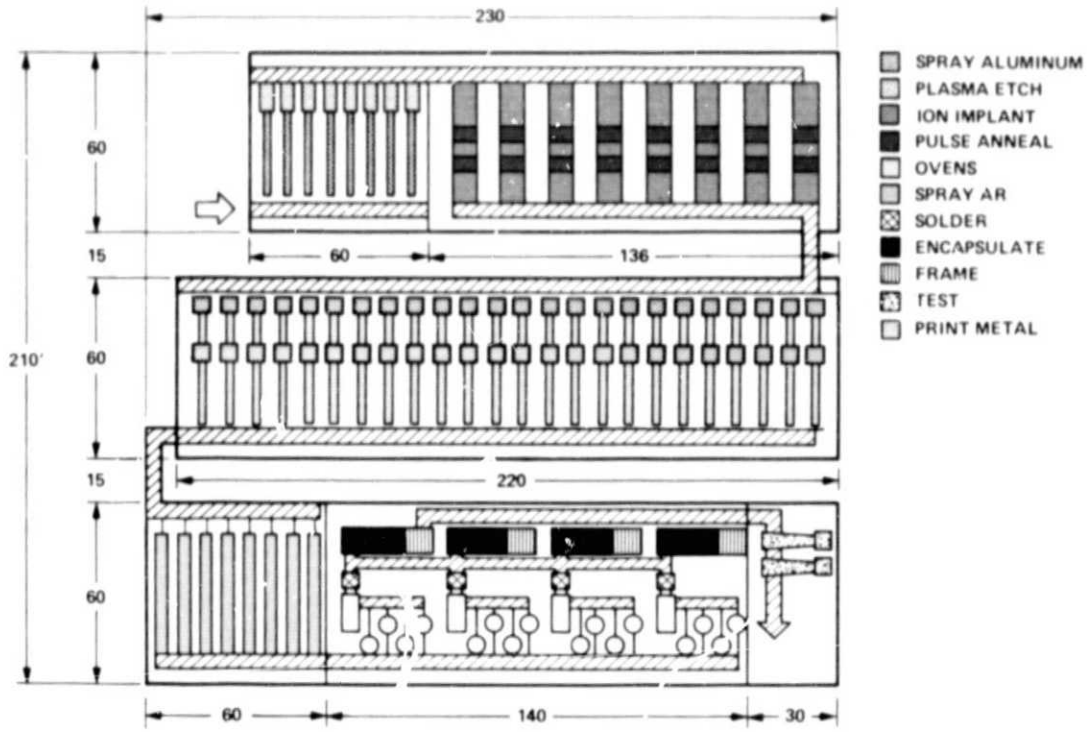


Figure 8

CELL AND MODULE FABRICATION

The cross-hatched spaces are 5 ft wide and reserved for up to a total of eight subconveyors feeding each of the back p+ aluminum spraying machines. The machines are from a catalog and reflect a conservative rate; they are a state-of-the-art type device. Building dimensions are rounded off to 230-ft long sections and each section houses some of the facilities such as QA and immediate supplies for the area. The wafer is sprayed with an aluminum powder, dried, then fired in ovens on the same machines. Plasma etchers remove the oxide and put the wafers back on what is anticipated to be a relatively complex conveyor system. The conveyor system is complex in order to avoid backlogs during times of machine shutdown. This helps to maintain as small an in-line inventory as possible -- an important costing factor.

The ion implanters involve vacuum interlocks and attendant handling equipment. The system offers two-stage operation potential for ion implanting and pulse annealing. This can be done twice and still stay within the cost allocation. If there were a need for a second implantation on the back, the wafers could be flipped over in lieu of the back surface field formed by the aluminum.

The material is carried by conveyor to the largest single operation, which is metallization. This is a "farm" of 24 machine strings. The first step is thick-film printing of metal-based ink on the back of these wafers, then drying in an oven. The wafers are then flipped over, thick-film printed on the other side, dried again, and fired. That is why the second oven is longer. The wafers are then put on conveyors to be sprayed with an antireflection coating, dried, and put back on conveyors to go to the assembly area.

In the assembly area, the 30,000 cells per hour breaks down to the fabrication of 160 modules per hour. There are 192 cells in a module. The operation is divided among four stations, each of which handles about 40 modules per hour.

The circles are industrial robots bonding the cells into strips of parallel cells. It takes four robots at a station to handle the rate. The strips are fed by a short conveyor system to an assembly machine, which puts them into fixtures for solder reflow. The interconnects have solder on them; they are tinned rather heavily to begin with. (Many light bulbs have wires soldered to an aluminum base; it is a standard, high-production technique.) This operation takes place where the cells are not present, so this cost presentation is not involved with the flux removal.

The loaded fixtures are then sent to vapor phase solder reflow ovens, very similar to those proposed in the $2/watt technology. The additional conveyor is for transferring material in the event that one of those areas is down. It prevents having to shut down this operation and allows shifting the material to the other machines -- this philosophy permits the same conveyor to serve a shutdown of the encapsulating and frame assembly machines.

The glass sheet and the ethylene vinyl acetate are bonded to the cells, forming a sandwich with a Mylar vapor barrier on the back. One of the reasons this process is using aluminum interconnects with aluminum back is that if the back has more moisture permeability, the galvanic potential would be more of a concern, so a first-level effort has been made to have all metals similar.

A reasonable amount of labor takes place in frame assembly, which can afford a hand operation to solder the connector and terminal wires. Fixture-assisted, to be sure, but this is similar to the way automobiles are built, i.e., there are many people moving in and out of the assembly line in this area. All of this is included in the cost analysis.

A wide conveyor carries these 4-ft panels to a strobe-flash xenon test. One machine can quite adequately handle the workload, but a second is included for back-up. In the area indicated by the arrow in Figure 8, the panels are put into crates and shipped to the warehouse.

	VALUE ADDED	CAPITAL COSTS	DIRECT LABOR	MATERIALS/ SUPPLIES	UTILITIES	INDIRECT EXPENSES	YIELDS YIELDS
SILICON* PREPARATION	0.043			0.0428			-
SHEET FABRICATION	0.134	0.0545	0.0308	0.0134	0.0047	0.0311	0.80
CELL FABRICATION	0.119	0.0421	0.0088	0.0451	0.0030	0.0187	0.93
MODULE FABRICATION	0.164	0.0440	0.0117	0.0892	0.0001	0.0188	0.98
TOTALS	0.460	0.1406	0.0513	0.1905	0.0079	0.0686	-

* BASED ON 10 $/kg SILICON.

Figure 9

ANNUAL COSTS (IN 1975 $/$W_{pk}$)

These figures involve actual costs, profits, and all the attendant monies that SAMICS takes into consideration.

The sheet fabrication added cost is a considerable drop from the $2/watt strawman, which allowed approximately $130 for that area.

The last step, module fabrication, includes the interconnection, the glass plate, and the metal frame, and has almost 10¢ worth of materials in it. It adds a value of about 16¢, bringing the total to 46¢, a rather encouraging number.

All of this is based upon a 12.9% encapsulated cell efficiency. Analyses have also been done for a 14% encapuslated cell efficiency, and this drops the total by more than 6¢.

	VALUE ADDED	CAPITAL COSTS	DIRECT LABOR	MATERIALS/ SUPPLIES	UTILITIES	INDIRECT EXPENSES	YIELDS YIELDS
SILICON PREP*	0.043			(0.0428)			–
SHEET FAB	0.134	0.0545	0.0308	0.0134	0.0048	0.0311	0.800
P+ BACK	0.002	0.0010	0.0004	0.0002	0.0000	0.0005	0.998
ETCH	0.010	0.0032	0.0018	0.0033	0.0000	0.0018	0.994
ION IMPLANT.	0.011	0.0055	0.0018	0.0000	0.0003	0.0032	0.998
PULSE ANNEAL.	0.018	0.0099	0.0004	0.0000	0.0015	0.0057	0.992
BACK METAL	0.035	0.0095	0.0013	0.0203	0.0005	0.0030	0.980
FRONT METAL	0.035	0.0098	0.0013	0.0199	0.0005	0.0030	0.980
AR COAT	0.008	0.0032	0.0018	0.0014	0.0002	0.0015	0.990
INTERCON	0.042	0.0121	0.0053	0.0178	0.0000	0.0070	0.999
ENCAPSULATE & ASSEMBLE	0.120	0.0314	0.0061	0.0712	0.0001	0.0115	0.999
TEST	0.001	0.0003	0.0002	0.0000	0.0000	0.0002	0.980
PACKAGE	0.001	0.0002	0.0001	0.0002	0.0000	0.0001	0.9999
TOTALS	0.460	0.1406	0.0513	0.1905	0.0079	0.0686	–

* BASED ON 10 $/kg SILICON

Figure 10

ANNUAL COSTS (IN 1975 $/$W_{pk}$)

The materials cost is the only cost in the silicon preparation and is based on $10/kg silicon; rounding off brings it to 4-1/3¢. In the sheet fabrication area, most of the supplies are furance parts. There is little labor; it is very capital-cost intensive.

The metallization figure allows enough money for silver, although that is not anticipated. If some of the ideas discussed in the metallization workshop are successful, that figure could be cut in half.

The interconnection scheme is materials intensive; half of it is the ribbon and the cost of the solder and flux. Encapsulation assembly involves the cost of the glass and encapsulants, which are about 5¢. The other 2¢ is for the frame and connector, etc. Testing and packaging are very small numbers.

	PROCESS	PRELIMINARY ECONOMIC ANALYSIS $/kg
BMI	REDUCTION OF $SiCl_4$ IN FBR	10.67/11.14*
UNION CARBIDE	CONVERSION OF $SiHCl_3$ TO SiH_4, DEPOSITION OF Si IN FSR OR FBR	7.48/8.00*
MOTOROLA	Si REFINING USING SiF_2	8.91
WESTINGHOUSE	REDUCTION OF $SiCl_4$ BY NA IN ARC HEATER REACTOR	10.93
DOW CORNING	PURER SiO_2 + C IN REFINED ARC FURNACE AND UNIDIRECTIONAL SUBDIFICATION	8.56
AEROCHEM	REDUCTION OF SILICON HALIDES BY ALKALI METALS USING FLAME CHEMISTRY	–
SRI	REDUCTION OF SiF_4 BY NA AND SUBSEQUENT Si PURIFICATION	7.19
SCHUMACHER	REDUCTION OF BROMOSILANES IN HIGH VELOCITY REACTOR	–

* INDEPENDENT ANALYSIS BY OTHER THAN PROCESS DEVELOPER

Figure 11

SILICON MATERIAL TASK OVERVIEW

John Goldsmith:

Where is the technology relative to the factors in the strawman model?

In the strawman model, a Union Carbide silicon process was used as the input in the conversion of metallurgical-grade silicon; it is high-quality silicon material that is compatible with the sheet production step. That particular process was costed in the SAMICS and SAMIS* exercise as $10/kg. Now the program is pursuing multiple approaches in this area of polysilicon development, as indicated in Figure 11.

On the far right side are preliminary economic analyses that have been done on these processes. There is no doubt that in some cases it is like comparing apples and oranges as to the details that have gone into compiling these numbers.

The figure of $8/kg for the Union Carbide process should be more like $9.50.

*Solar Array Manufacturing Industry Simulation

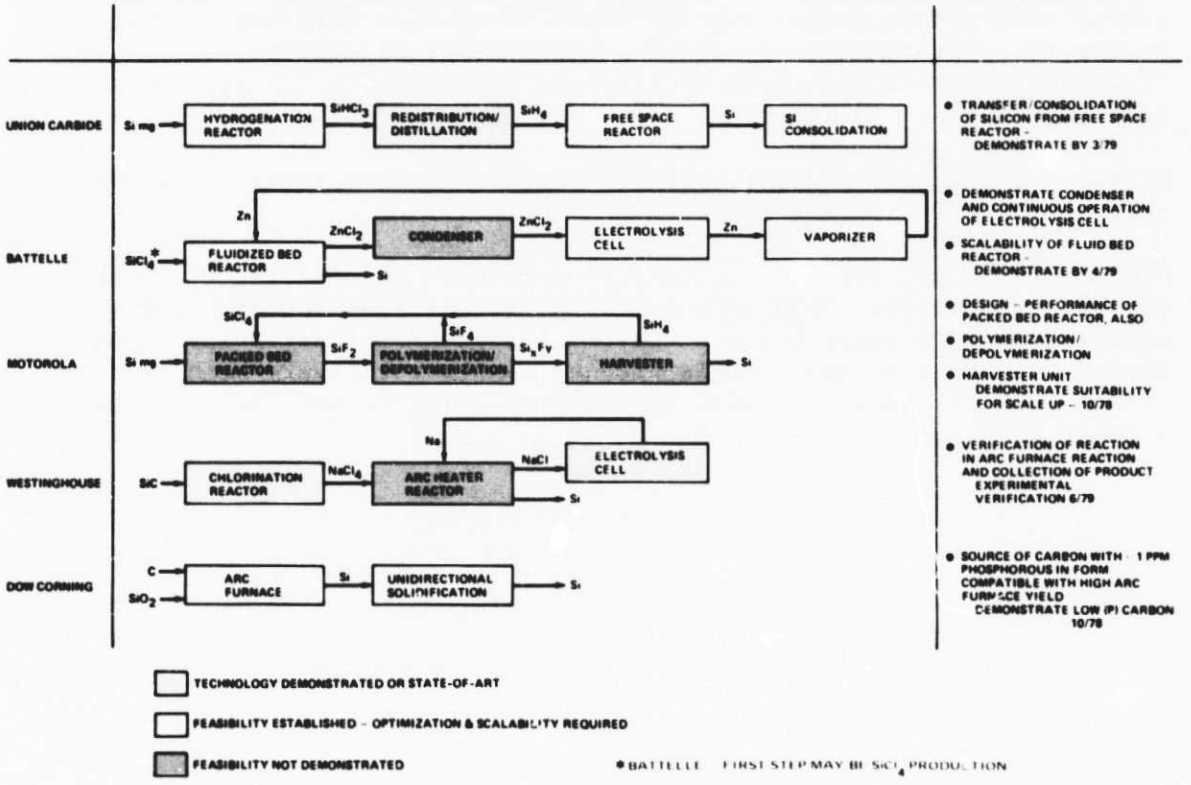


Figure 12

SILICON MATERIAL TASK
TECHNICAL-EMPIRICAL PROCESS VERIFICATION

The presentation on current technology is simplified and thus results in some distortions. Therefore, it should be used only as an indicator of where these technologies are relative to state-of-the-art operations.

Progress in the Union Carbide process appears good. Material is coming from the process, and that material is being transferred into various types of sheet growth approaches. It is believed that by April 1979 the LSA Program will be in good shape in terms of demonstrating the feasibility of that particular process.

The Battelle process is also very interesting, and is based on much technology that is somewhat accessible. It is expected that sometime between April and August of 1979, the Program will have completed those stages associated with demonstrating that the process is compatible with investing in a large-scale demonstration facility.

Motorola's approach of using fluorosilicic acid as the input into this material is a significantly different approach. It has some very excellent potential associated with making high purity silicon that can be considered for all of these various sheet programs, but it is a basically different approach in that it does not allow the same experiences that permit generating the kinds of numbers obtained from some of the other processes. By about October 1978, enough development and information should have been obtained so the approach can proceed to some significant scale-ups.

In the Westinghouse process, verification of the arc furnace reaction step is focused for June 1979.

Dow Corning's arc furnace approach depends upon an improvement in arc furnace technology. This is a higher purity type of approach for material that is ready for production of high-efficiency solar cells. One of the choke points in this process is obtaining very high purity carbon that is compatible with the process. The target date here is October 1978.

	ORGANIZATION	PROCESS APPROACHES	$/W(pk) PRELIMINARY ESTIMATE ADDED VALUE PRICES
INGOT*	HAMCO	ADVANCED CZ	0.12 AT 17%η
	SILTEC	ADVANCED CZ	0.12 AT 17%η
	TI	ADVANCED CZ	0.14 AT 17%η
	VARIAN	ADVANCED CZ	0.13 AT 17%η
CASTING*	CRYSTAL SYSTEMS	HEAT EXCHANGE METHOD	0.035 AT 17%η
WAFERING	VARIAN	MULTIPLE BLADE SAW	(0.07 AT 17%η)
	CRYSTAL SYSTEMS	MULTIPLE WIRE SAW	(0.03 AT 17%η)
RIBBON	MOBIL-TYCO	EDGE-DEFINED FILM-FED GROWTH (EFG)	0.12 AT 14%η
	MOTOROLA	RIBBON-TO-RIBBON (RTR)	0.10 AT 14%η
	WESTINGHOUSE	DENDRITIC WEB (WEB)	0.09 AT 14%η
	IBM	CAPILLARY ACTION SHAPING TECHNIQUE (CAST)	0.10 AT 14%η
	HONEYWELL	SILICON ON CERAMIC (DIP COATING) (SOC)	0.11 AT 12%η
	RCA	LOW COST EPI	0.08 AT 15%η

* WAFERING ASSUMPTION: 0.04 cm SLICE AND KERF THICKNESS (1 m^2/kg)

Figure 13

LARGE AREA SILICON SHEET

In processes associated with trying to convert polysilicon into sheets, interest centers on techniques in ingot technology as well as techniques in ribbon technology

The process used for the strawman model is the EFG approach, a nominally 14% efficiency technique that gives a 12¢ value added price when viewed in a context of an overall 50¢/watt product. From that can be seen the relationships between that approach and the other approaches discussed. At the present, there is probably little doubt that the EFG process has reached maturity in terms of technology that some of the others have not. But the other processes are still being considered and there definitely is significant interest in all approaches associated with what the EFG technology is giving in terms of being compatible with a less than 46¢/watt solar array technology.

Problems associated with achieving good wafering technology is the choke point in ingot technology, and there have been significant problems with Varian and Crystal Systems. There are expectations of broadening that program in FY'79, contingent on available resources. Ingot and casting approaches have been eliminated in competing for the less than 50¢/watt goal.

Figures 14 and 15 indicate the distance yet to go. Using the EFG process as an example, to meet throughput goals a sheet thickness on the order of 200 μm is necessary. This has been demonstrated. In the area of production, five 75 mm wide ribbons must be pulled from one machine at the rate of approximately 3 inches per minute. This has been demonstrated. The primary questions in terms of the EFG process are: can that process be automated? Can it be scaled up? Can the system deliver satisfactory performance when it is run on a long-term, continuous basis?

SHEET TECHNOLOGY	SHEET THICKNESS (μm)		AREA PRODUCTION RATE (m^2/hr)		SILICON MAT'L UTILIZATION (m^2/kg)		SOLAR CELL EFFICIENCY η (%)		PROJECTED 1986 ADD-ON PRICES	
INGOT	1986	1978	1986	1978	1986	1978	1986	1978	$/$m^2$	$/$W_{pk}$
ADV CZ*	250	250	2	1.6	0.95	0.85	17%	16%	25.00	0.45
HEM CASTING	250	250	2	0.6	0.95	0.85	17%	14%	10.62	0.08
RIBBON										
EFG	200	200	1.7	0.6	2.15	2.15	14%	12%	16.57	0.12
WEB	100	100	0.15	0.05	4.3	4.3	14%	15%	14.40	0.09
RTR	100	150	0.8	0.30	4.3	2.9	14%	12%	15.00	0.10
CAST	100	200	1.2	0.12	4.3	2.18	14%	12%	12.62	0.09
SOC	100	100	1.0	0.27	4.3	4.3	12%	10%	14.00	0.11
EPI	30	30	9.4	0.01	14.5	NA	15%	13%	12.00	0.08

* ASSUMES WAFERING CONVERSION 1 m^2/kg 1986
(MULTIWIRE SAWING) 0.89 m^2/kg 1978

Figure 14

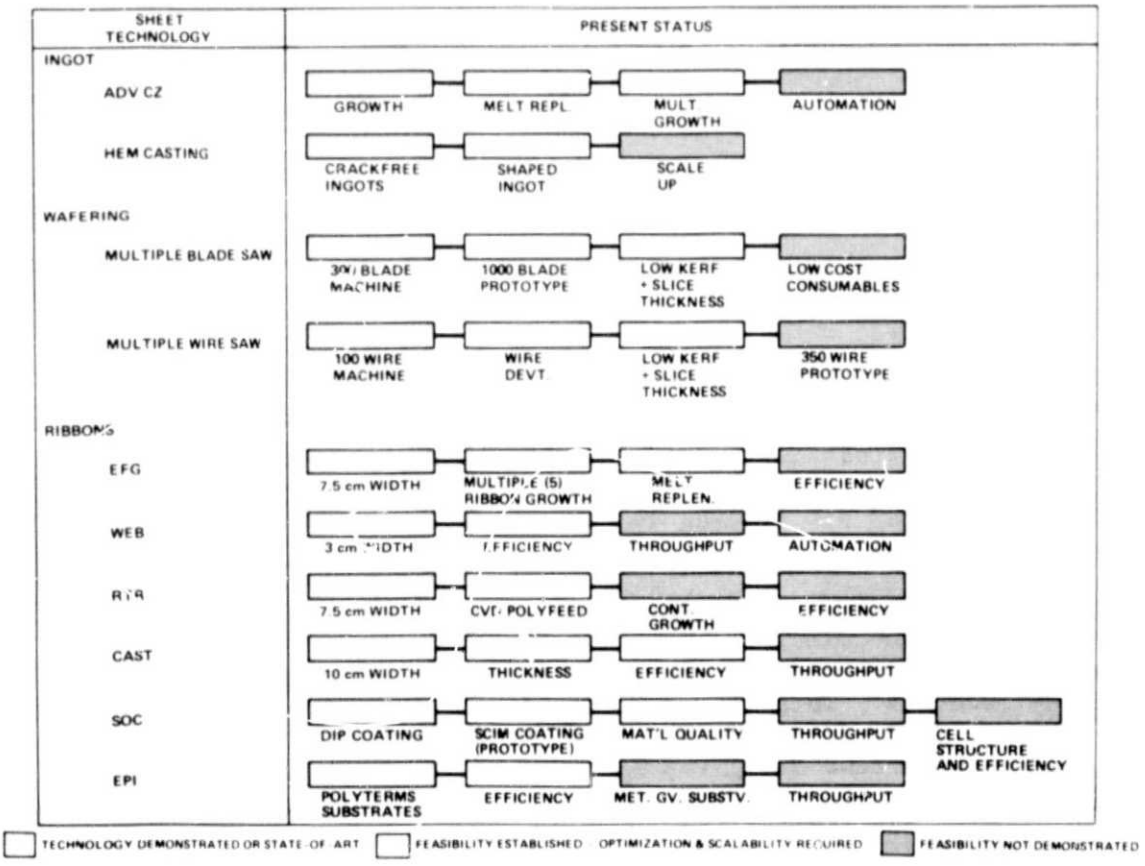


Figure 15

KEY PROCESS	OPTIONS	CONTRACTORS
SHAPING	LASER SCRIBING, SAWING	SENSOR TECH, WESTINGHOUSE S.O.A.
BACK SURFACE FIELD	ALUMINUM GROUP III POLYMERS ION IMPLANTATION CVD DIFFUSION	SOLAREX, ARCO, SPECTROLAB SENSOR TECH SPIRE, MOTOROLA WESTINGHOUSE, RCA S.O.A.
SURFACE PREPARATION	PLASMA WET CHEMICAL	MOTOROLA, TEXAS INSTRUMENTS S.O.A.
JUNCTION FORMATION	ION IMPLANTATION DIFFUSION GROUP V POLYMERS	KINETIC COATINGS, MOTOROLA, LMSC, RCA, SPIRE S.O.A. SENSOR TECH, SOLAREX, SPECTROLAB, TEXAS INSTRUMENTS
ANNEAL	PULSE FURNACE	SPIRE, LMSC S.O.A.
METALLIZATION	PLATING THICK FILM	MOTOROLA, SENSOR TECH, SOLAREX LMSC, ARCO, RCA, SPECTROLAB
AR COATING	CVD SPRAY SPUTTER EVAPORATE	MOTOROLA LMSC, RCA KINETIC COATINGS S.O.A.
INTERCONNECT	SOLDER WELDING	S.O.A. RCA, SOLAREX

Figure 16

PRODUCTION PROCESS AND EQUIPMENT

EFG concerns that part of the program having to do with understanding the efficiency of the system -- the performance, the yield numbers, and the resulting performance of the ribbons themselves. This implies a significant need for scaling up the program in order to gain understanding as to whether this is going to be possible.

In the wafering area, one of the major areas of concern, progress is good as far as the machines themselves are concerned. But concerns remain about the consumables that are going to have to be compatible with the machines. This is a key item for next year.

The available options are given in the middle column of the chart in Figure 16, and on the far right are the organizations that have contracts with the LSA Project to study problems associated with shaping and back surface field formation, for instance, and surface preparations, etc., all compatible with the low-price goals.

PROCESS INVESTIGATION	ADDED VALUE COST GOAL	PRESENT TECHNOLOGY	KEY TECHNICAL MILESTONE NEEDED TO BE DEMONSTRATED
BACK SURFACE FIELD	0.002	0.018/0.040	AUTOMATION DEMO REQUIRED
SURFACE PREPARATION	0.010	0.015/0.100	INCREASED THROUGHPUT
JUNCTION FORMATION	0.011	0.039/0.460	LARGER ION IMPLANTER
ANNEAL	0.018	0.027/0.041	DEVELOP PULSE/SCAN PROCESS
METALLIZATION	0.070	0.020/0.564	CONSISTANT RELIABILITY
AR COATING	0.008	0.017/0.274	PROCESS DEMONSTRATED; EQUIPMENT AVAILABLE
INTERCONNECT	0.042	0.600/2.000	AUTOMATION DEMO REQUIRED
ASSEMBLE	0.120	0.400/10.000	GLASS SUPERSTRATE DEMONSTRATED AUTOMATION DEMO REQUIRED
TEST AND PACK	$<$0.002	0.032/0.500	LARGE MODULES – INCREASED THROUGHPUT

Figure 17

PRODUCTION PROCESS DEVELOPMENT

How far can the strawman and an extrapolation from today's technology be carried? Much time and effort have been spent in disseminating information about technologies that are available within the semiconductor industry and how they might be applied to LSA Project goals.

For instance, in the back surface field area it can be seen that this process is appropriate for the LSA goals. The major concern is building a machine to demonstrate it. This means using the technology that exists, but to build machines that prove scalability is compatible with the value added cost goals.

A major deviation from that might be in the junction formation area. An ion implantation approach has been used as the primary means of forming the junction, thus requiring approximately 100 milli ampere machines in order to have the throughput compatible with the overall goals of the progam. The present largest machines are on the order of 3 to 4 milli amperes. A significant effort has been spent with SPIRE, for instance, in evaluating the problems associated with performance of 3 to 4 milli ampere ion implanters that are compatible with solar cell formation. Solar cells having a Czochralski type of wafer have been produced with efficiencies greater than 16% using the LSA ion implanter. LSA has not entered into the EFG type of sheet formation, but it should be done soon.

The 16% solar cell was based on a furnace anneal. The program proposed something such as an electron beam, pulsed anneal approach. This has been demonstrated in the laboratory where solar cells with 15% efficiencies have been produced using ion implantation with a 3 milli ampere machine, and using the pulsed annealing approach.

Larger machines are certainly needed. Designs have been produced of a 100 milli ampere machine configuration that is compatible with the overall program.

There has been much work on pulsed annealing -- laser, electron beam, and other techniques. Now it must be proved that this technology definitely exists. It is necessary to enter these large machine technologies so that the problems associated with throughput and its impact on overall efficiencies can be evaluated again.

Metallization is one of the most critical elements in the program, and one where it is the least easy to discuss present technology. Because of that uncertainty, the figure 7¢/watt is used in the strawman. Even the basic model is based on using aluminum as the contact material. This number is based on silver. It is a number that is compatible with silk screening. Numbers as low as 2¢ have been forecast.

The major theme in the area of production processes and process development seems to be that much of the technology that is state-of-the-art is there. The problem is innovation in trying to bring the processes from their present stages into a configuration compatible with the high-efficiency, large-throughput technologies needed for a $500 kW factory.

APPROACHES IDENTIFIED

- TOPSTRATE – GLASS, ACRYLICS, UV SCREEN
- POTTANTS – EVA, PVC, ACRYLICS, SILICONES
- SUBSTRATES – WOOD, MYLAR, FOILS, STEEL

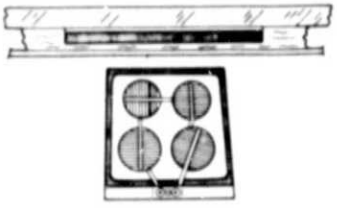
TECHNOLOGY	ORGANIZATIONS	STATUS	NEEDED R&D
MATERIALS	SPRINGBORN DOW CORNING (SILICONES)	CANDIDATE SYSTEMS SELECTED 2.5¢ – 10¢/WATT	• UV SCREENS FOR LOW-COST POTTANTS • DESIGNS FOR OPTIMUM OPTICAL, ELECTRICAL, STRUCTURAL, THERMAL PERFORMANCE
PROCESSES	SPIRE ENDUREX MOTOROLA	PRODUCTION PROCESSES AVAILABLE ELECTROSTATIC BONDING DEMONSTRATED ION-PLATING DEMONSTRATED AR COATING GLASS DEMONSTRATED	• TAILOR MATERIAL SYSTEMS TO HIGH PRODUCTION RATES • SCALE-UP ESB PROCESS AND EQUIPMENT • POROSITY PROBLEM AND SCALE-UP • AR COATING SCALE-UP AND PROCESS CONTROL
LIFE PREDICTION	BATTELLE ROCKWELL CASE WESTERN CAL TECH	ACCELERATED TESTING METHODS AVAILABLE FAILURE MODES IDENTIFIED	• IMPLEMENT LIFE TEST AND PREDICTION OF MEAD ARRAY PLUS OTHERS • HIGH ACCELERATION LIFE TEST METHODS AND FACILITIES (10-50x)

Figure 18

ENCAPSULATION TASK

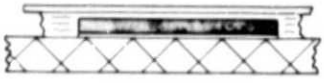
Encapsulation is in approximately the same circumstances as production processes. The various encapuslation techniques have been identified with costs ranging from 2-1/2¢ to 10¢; the strawman uses a 5¢ approach. The largest problem may not be putting together an encapsulation package resembling the strawman, but in proving that it will last the desired 20 years. A much more serious effort is being made now in testing and analyzing candidate systems.

SUPERSTRATE CONFIGURATIONS (STRUCTURAL TRANSPARENCY)



GLASS SUPE (STRATE	ADHESIVE	POTTANT	BACK	QUAL TESTS −40° +90°C 50 CYCLES 95% RH 40°C 168 hr	OUTDOOR TEST 3 MONTHS 14 MODULES
1. BOROSILICATE	ELECTRO-STATIC BOND	PVB	SL GLASS	PASS	—
2. BOROSILICATE	ESB	EPOXY	AL FOIL	PASS	—
3. BOROSILICATE	ESB	BUTYL	AL FOIL	PASS	—
4. SUNADEX TEMPERED	PVB	PVB	SL GLASS	PASS	CONT
5. SUNADEX	PVB	PVB	MYLAR	PASS	CONT

SUBSTRATE CONFIGURATIONS (STRUCTURAL BACK)



COVER	POTTANT	ADHESIVE	SUBSTRATE		
1. ACRYLIC	←	SILGRIP	POLYESTER/FG	PASS	CONT
2. SPRAYLON (FLUOROCARBON)	←	←	ALUMINUM	FAIL	—
3. ACRYLIC UV-FILM	EVA	←	STEEL	PASS	CONT
4. ACR-UV-FILM	IONOMER	←	THERMOPLASTIC	FAIL	—
5. ACR-UV-FILM	PVC	←	WOOD	DARKEN	CONT
6. ACR-UV-FILM	ACRYLIC ELASTOMER		THERMOSET	—	—
7. EVA	EVA	ACRYLIC	PAPER HONEYCOMB		CONT

NOTE:

PVB	– POLYVINYL BUTYRAL
EVA	– ETHYLENE VINYL ACETATE
SL	– SODA LIME GLASS
PVC	– POLYVINYL CHLORIDE
ACR-UV	– ACRYLIC-UV SCREEN

Figure 19

INTERIM ASSESSMENT: 1986 ENCAPSULATION CANDIDATES

The LSA Project is emerging from the effort to identify systems that look as if they will probably work, and is entering the effort to gain enough data from real time and accelerated testing.

Figure 19 does not show the strawman package, but the intention is to have that configuration tested soon.