

Fully Integrated, Low Drop-Out Linear Voltage Regulator in 180 nm CMOS - DTU Orbit (09/11/2017)

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This paper presents a capacitor-free low dropout (LDO) linear regulator based on a dual loop topology. The regulator utilizes two feedback loops to satisfy the challenges of hearing aid devices, which include fast transient performance and small voltage spikes under rapid load-current changes. The proposed design works without the need of a decoupling capacitor connected at the output and operates with a 0-100 pF capacitive load. The design has been taped out in a 0.18 μm CMOS process. The proposed regulator has a low component count, area of 0.012 mm² and is suitable for system-on-chip integration. It regulates the output voltage at 0.9 V from a 1.0 V - 1.4 V supply. The measured results for a current step load from 250-500 μA with a rise and fall time of 1.5 μs are an overshoot of 26 mV and undershoot of 26 mV with a settling time of 3.5 μs when CL between 0-100 pF. The proposed LDO regulator consumes a quiescent current of only 10.5 μA . The design is suitable for application with a current step edge time of 1 ns while maintaining ΔV_{out} of 64 mV.

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