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Research Article

Operation and control design of an input-series–input-parallel–output-series conversion scheme for offshore DC wind systems

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Abstract: High-power converters for high-voltage direct current transmission systems and collecting networks are attracting increasing interest for application in large offshore wind farms. Offshore wind farms are capable of generating more electric energy at lower cost when compared with onshore wind systems. In this study, DC/DC voltage conversion should be achieved with a power converter that uses readily available semiconductor devices. A modular DC/DC converter can achieve the required system currents and voltages without exceeding semiconductor ratings. In this study, the operation and control strategy for an input-series–input-parallel–output-series (ISIPOS) energy conversion system for wind systems are presented. The ISIPOS system allows the direct connection of wind turbines to the DC grid. In this research, the design process to control the input and output currents and voltages is explained. In addition, a new method to ensure voltage and current sharing between the different modules is presented and explained. The basic structure, control design, and system performance are tested using MATLAB/SIMULINK. Practical results validate the control design flexibility of the ISIPOS topology when controlled by a TMSF280335 DSP.

1 Introduction

Presently, >3000 offshore wind turbines have been installed in the European sector with total capacity of ∼11 GW. In 2015, the allocated investment for offshore wind farm projects exceeded £14bn [1]. Offshore wind farms are preferred over onshore farms for many reasons, including increased power capability, lower environmental impact and the ability to install larger wind turbines [2, 3]. Therefore, it is expected that offshore farms will form approximately one-third of the total generated wind power in the near future [2]. Thus, the international trend towards offshore wind farms necessitates long distance and large transmission networks with high power ratings.

For wind farms located >75 km offshore, advanced high-voltage direct current (HVDC) transmission systems become more promising. This is because HVDC systems require fewer transmission lines when compared with AC architectures, in addition to their stability and controllability [4]. The absence of reactive power circulation in the submarine cables of HVDC systems reduces power losses in the cables and increases the total efficiency [5]. Moreover, large-scale offshore wind power systems form weak connection points where HVDC system can assist with grid code compliance, increasing the power quality onshore and dealing with the voltage and current unbalance at high power levels [4]. Considered as important merits in weak grids, HVDC transmission systems offer the capability of black start as well as the ability to operate at relatively low wind speeds [4].

Presently, the most common configuration for offshore wind farms with an HVDC transmission network uses an AC collection network to connect all the wind turbines to an offshore AC/DC platform [6, 7]. However, this configuration has high total cost and size because it requires a bulky low-frequency AC transformer. For this reason, replacing the AC collection network with a DC network can add additional advantages. First, the circulating reactive currents will be eliminated and hence, the total efficiency will be improved. Second, DC collection networks will omit the need for the line-frequency AC transformer and hence, the total footprint of the system can be reduced. In this paper, the main challenge of this configuration would be the ability to boost the wind turbine low voltage to the desired transmission level. The DC/DC converters proposed to achieve this should have acceptable efficiency and offer the same reliability when compared with the eliminated AC transformer [8].

Modular DC/DC converters for medium-voltage applications have been discussed extensively in the literature [9–14]. Due to their capability to operate with zero-voltage switching, phase-shift full-bridge converters are widely used for high-power applications [12]. Many configurations for parallel and series connection of several modules are proposed in order to reduce the current and voltage stresses in the semiconductor devices and hence, the device technologies that are readily available in the market can be used in the implementation. Therefore, each module is exposed to a small fraction of the total voltage and current and hence, the semiconductor devices can operate at relatively high switching frequency (> 10 kHz). In addition, the turn's ratio of the isolation transformers can be reduced if the converter outputs are series connected. This leads to a lower leakage inductance in each module. These types of DC/DC converter are suitable for both unidirectional and bidirectional power applications. Traditionally, the configurations of multi-module DC/DC converters can be classified into four main types: input-parallel–output-parallel, input-parallel–output-series (IPOS), input-series–output-parallel and input-series–output-series (ISOS) [14].

A novel configuration for a modular energy conversion system has been presented [3] where each phase of the AC system is connected to several single-phase power stacks, as shown in Fig. 1*a*. Each stack consists of an AC/DC converter followed by an IPOS DC/DC converter cluster. Then, the output of each phase is connected in series to maximise the output DC voltage and consequently, parallel or series connection of the power devices will be avoided. Accordingly, the design of the modular single-phase converters will not be complicated. Although offshore wind turbine systems require unidirectional power flow, this configuration can be used for other applications where the bidirectional power flow is required. The whole configuration can be viewed as an input-series–input-parallel–output-series (ISIPOS) AC/DC converter. The modularity of this converter provides high reliability, internal module fault tolerance and it allows for correct operation at different terminal voltages. Moreover, current and

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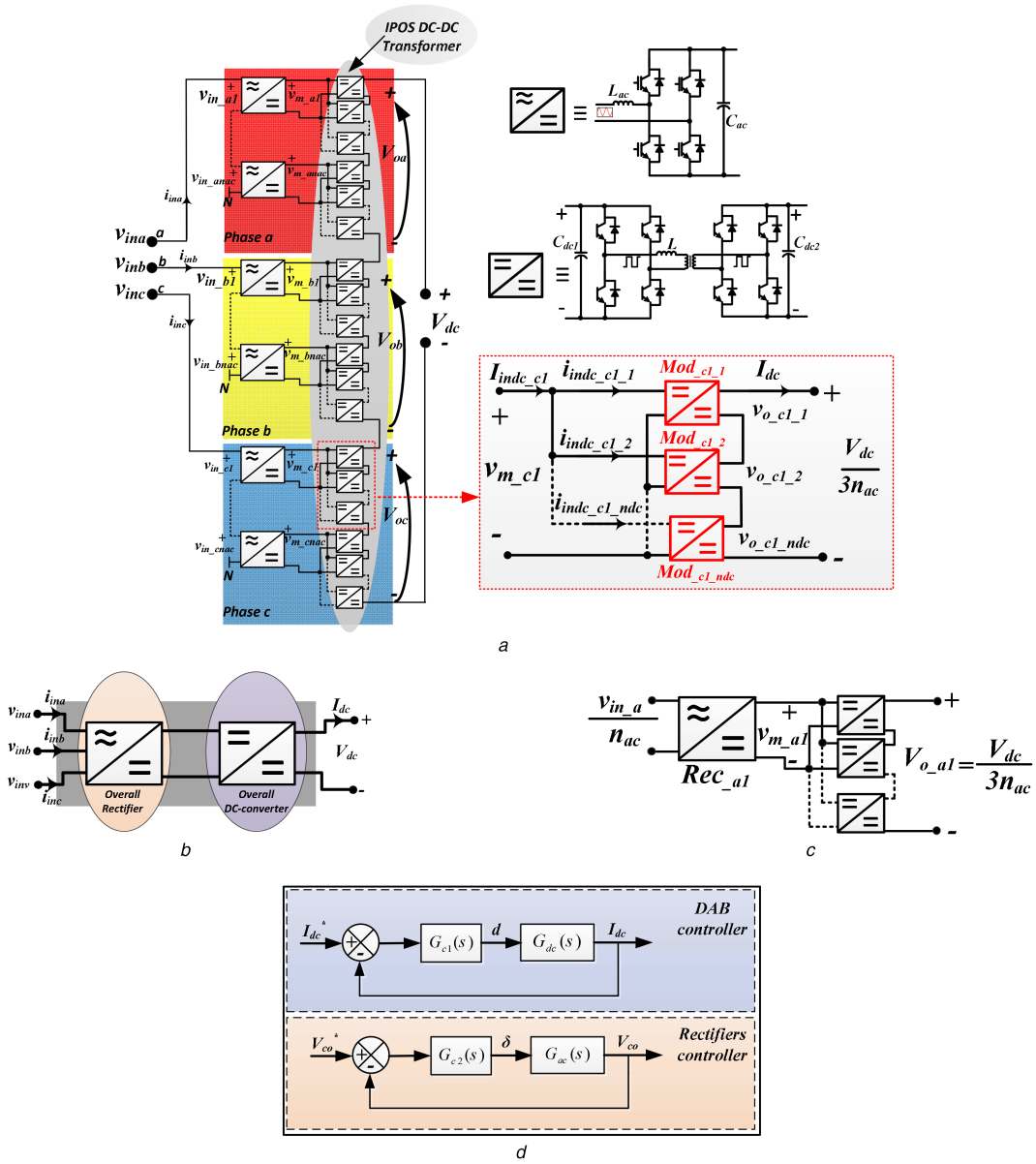

Fig. 1 *ISIPOS AC/DC energy conversion system*
(a) Full system, ***(b)*** Simplified AC–DC ISIPOS system, ***(c)*** Single rectifier with its DC/DC converter, ***(d)*** Simplified block diagrams of overall controllers

voltage ripples in the passive components can be reduced significantly when interleaved modulation of the sub-modules is used, leading to better performance. However, the control strategy of this configuration should achieve three main objectives:

i. Controlled power flow between the input and output sides while keeping the converters voltages and currents within the acceptable limits.
ii. A fast dynamic response during abnormal operating conditions.
iii. Voltage and current sharing between the different sub-modules.

Generally, two main control techniques have been used for these types of converters, namely, fixed frequency and variable frequency techniques. Variable frequency control adds to the complexity of controller design, as well as creating undesired EMI components which necessitate increased filtering [15–17]. However, fixed frequency control, such as phase-shift control (PSC) [18, 19], avoids these disadvantages and offers better performance, especially for the DC/DC converter part of the system. Using the fixed frequency control approach, this paper explains the operation and modelling of the previously mentioned ISIPOS AC/DC converter for medium-voltage applications. In addition, the paper identifies important issues in the implementation of control algorithms to satisfy both simplicity and desired performance using classical proportional + integral (PI) control loops. The remaining of this paper is organised as follows: Section 2 describes the system under investigation and explains its basic structure and operation. Section 3 discusses the control methodologies of the system from the perspective of overall power transfer control as well as power sharing control. In power transfer control, the AC/DC rectifiers and DC/DC converter modules are considered as if their series semiconductor switches operate simultaneously, and any small voltage and current mismatches are neglected. In power sharing control, the decentralised controllers are responsible for ensuring equal power sharing between the different rectifiers and modules in order to improve the modularity and reliability. MATLAB/SIMULINK simulations for power transfer and power sharing controllers are presented in Section 3. Section 4 presents the experimental results of the ISIPOS system when controlled with a TMS320F28335 DSP.

2 System description

The symbols and variables used to describe the system shown in Fig. 1*a* are listed in Table 1 and the overall AC/DC system is shown in Fig. 1*b*. For practical operation at 5 MW and a DC collecting voltage of 50 kV, the input and output currents and voltages of the system are listed in Table 2. A single rectifier with

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its DC/DC group is shown in Fig. 1*c* where n_{ac} is the number of rectifiers per phase, n_{dc} is the number of DC/DC converters per rectifier and N_{dc} is the total number of DC/DC converters in the system. For the dual-active bridge (DAB) DC/DC converter circuit, it is preferable to operate the converter in the condition that the input and output voltages are close to each other to ensure that the circulating current and the converter inductor values are as low as possible [20].

Therefore, the intermediate voltage V_m is chosen as

$$V_m = \frac{V_{dc}}{N_{dc}} = \frac{V_{dc}}{3n_{dc}n_{ac}} \tag{1}$$

To ensure reliable operation, the de-rating factor of the switches should be ~70%. In view of this, the IGBT switches for the rectifiers and DC/DC converters are rated at 1.7 and 1.2 kV/200 A, respectively. The number of modules and the operating conditions are listed in Table 3. The inductor value L is selected to transfer the module power at a duty ratio $D = 0.25$ while the other passive elements are chosen to allow for <10% ripple across the capacitors and inductors.

Table 1 System variables

Symbol	Variable
n_{ac}	number of rectifiers per phase
n_{dc}	number of DC/DC converter modules per rectifier
N_{dc}	total number of DC/DC converter modules
$v_{in_k}\ k \in \{a, b, c\}$	phase *k* AC voltage
$i_{in_k}\ k \in \{a, b, c\}$	phase *k* AC current
$k \in \{a, b, c\}$ $v_{in_kp}\ p \in \{1, 2, \ldots, n_{ac}\}$	AC voltage of the *p*th AC/DC rectifier in phase *k*
$k \in \{a, b, c\}$ $v_{m_kp}\ p \in \{1, 2, \ldots, n_{ac}\}$	DC voltage of the *p*th AC/DC rectifier in phase *k*
$k \in \{a, b, c\}$ $I_{indc_kp}\ p \in \{1, 2, \ldots, n_{ac}\}$	DC current of the *p*th AC/DC rectifier in phase *k*
$k \in \{a, b, c\}$ $i_{indc_kp_j}\ p \in \{1, 2, \ldots, n_{ac}\}$ $j \in \{1, 2, \ldots, n_{dc}\}$	input current of the *j*th DC/DC module of the *p*th rectifier in phase *k*
$k \in \{a, b, c\}$ $v_{o_kp_j}\ p \in \{1, 2, \ldots, n_{ac}\}$ $j \in \{1, 2, \ldots, n_{dc}\}$	output voltage of the *j*th DC/DC module of the *p*th rectifier in phase *k*
$k \in \{a, b, c\}$ $Mod_{kp_j}\ p \in \{1, 2, \ldots, n_{ac}\}$ $j \in \{1, 2, \ldots, n_{dc}\}$	DC/DC module number *j* connected to the *p*th rectifier in phase *k*
$k \in \{a, b, c\}$ $Rec_{kp}\ p \in \{1, 2, \ldots, n_{ac}\}$ $j \in \{1, 2, \ldots, n_{dc}\}$	AC/DC rectifier number *p* in phase *k*
$k \in \{a, b, c\}$ $V_{o_kp}\ p \in \{1, 2, \ldots, n_{ac}\}$	total output DC voltage of DC/DC series converters group connected to the *p*th rectifier in phase *k*
$V_{o_k}\ k \in \{a, b, c\}$	total output DC voltage of DC/DC series converter group in phase *k*
V_{dc}	total output DC voltage
I_{dc}	output DC current

Table 2 Main characteristics of the system under consideration

Parameter	Value
P_{rated}	5 MW
v_{ac}	4 kV (line-to-line)
i_{in}	722 A (rms)
V_{dc}	50 kV
I_{dc}	100 A
power factor	0.99

3 Control structure

Overall, the system under investigation can be viewed as a two-stage power converter, as shown in Fig. 1*b*. For such a system, controller design becomes complex for several reasons. The overall system bandwidth of the power transfer controller is restricted to guarantee that undesired voltages and currents at the resonance frequencies are not excited because of the existence of the resonant poles. Consequently, the dynamics and transient response of the system are limited. In addition, other control loops should be inserted to assure equal current and voltage sharing between the series and parallel modules. These loops should respond more quickly than the main power controller and should not interact with it. This adds to the complexity of the control design process. In this context, the control system can be divided into two parts:

- Overall controller which controls the power transfer from the input to the output sides and sets the operating points of the system.
- Module-based controller to ensure equal power sharing between the modules and to cater for the small mismatches in the different power modules.

The following subsections will discuss the design process for these loops in order to achieve correct operation, acceptable transients and suitable dynamic response during faults and abnormalities, as well as to achieve correct sharing between the different power modules.

3.1 Overall control

Assuming that all the passive components of the converters are identical and that all converters have the same duty ratio and gate drive signals, i.e. all the semiconductor switches are switched on and off in the same time, the equivalent circuit of the IPOS DC converter will be as the DAB circuit shown in Fig. 8*a* with $C_1 = C_{dc1}/n_{dc}$, $C_2 = n_{dc}C_{dc2}$, and $L = L/n_{dc}$. In the same way, the equivalent circuit of the ISOS AC converter will behave as the circuit shown in Fig. 8*c*. In other words, the series–parallel combinations of AC and DC converters are viewed as two cascaded converters (Appendix).

3.1.1 DC converter control: The closed-loop block diagram of the overall DC converter is shown in Fig. 1*d* (the accompanying mathematical analysis can be found in Appendix), where

$$G_{c1}(s) = K_{p1} + \frac{K_{i1}}{s} \tag{2}$$

(see (3)) where d is the small-signal duty ratio of the DAB converter and D is equilibrium duty ratio where its maximum value $D_{max} = 0.5$. To ease the gain selection process, a point at the middle of the trajectory, $D = 0.25$, is selected to be the equivalent operating point. Then, the root loci of the closed-loop system can be drawn in two ways. In the first way, the proportional gain K_{p1} is kept constant at 0.5 while the integral gain K_{i1} is changed in the range of [10:50]. In the second way, K_{i1} is constant at 15 and K_{p1} is changed from 0.1 to 1. The resulting loci are shown in Figs. 2*a* and *b*. The ranges of the gains are selected initially to keep the system stable. From the presented analysis, the system always has real poles and no oscillations. The controller gains are selected to be $K_{p1} = 0.45$ and $K_{i1} = 25$ to give acceptable dynamics and 90° phase margin.

3.1.2 AC converter control: Using the same approach, the equivalent circuit of the series-connected AC converters can be considered to be as shown in Fig. 8*c*, with $L_{in} = n_{ac}L_{ac}$ and $C_o =$

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C_{ac}/n_{ac}. Therefore, the overall AC control system can be expressed as shown in Fig. 1*d*. Figs. 2*c* and *d* show the frequency domain analysis of the control loops. The gain values are selected as $K_{p2} = 3$ and $K_{i2} = 15$ to ensure fast response (acceptable bandwidth) and to reduce system oscillations

$$G_{c2}(s) = K_{p2} + \frac{K_{i2}}{s} \tag{4}$$

$$G_{ac}(s) = \frac{\tilde{v}_{co}}{\tilde{\delta}} = \frac{G_{14}}{G_{14}(1 + C_o L_{in} s^2) + L_{in} s} V_{in}$$
$$\text{where}$$
$$L_{in} = L_{ac} \cdot n_{ac}, \quad C_o = C_{ac}/n_{ac} \tag{5}$$

Fig. 3*a* shows the MATLAB/SIMULINK simulation results for the system using these parameters and control gains. Fig. 3*b* shows the simulations for the case when 80% pole-to-pole fault occurs at the DC collection terminals.

3.2 Module-level control

Equal power sharing inside the converter modules may be disturbed during normal operation and switching transients. Voltage and/or current control balancing techniques should be employed to ensure equilibrium between the series or parallel connected converters [21]. In this section, decentralised power sharing techniques are implemented in parallel with the overall voltage and current control, i.e. module-level control works separately but alongside the overall AC and DC control schemes. To ensure that the overall control, which is responsible for controlling the output total voltages and currents, is not affected by module-level control schemes, the latter should be fast and have high bandwidth with respect to the main overall controllers.

3.2.1 IPOS DC/DC converter controller: Considering the first DC/DC converter cluster of phase *a* as a case study (see Fig. 4*a*), it is necessary to ensure that either the voltages ($v_{o_a1_1}$, $v_{o_a1_2}$, …, $v_{o_a1_ndc}$) or the currents ($i_{indc_a1_1}$, $i_{indc_a1_2}$, …, $i_{indc_a1_ndc}$) are evenly shared. It is well known that for input–parallel connected systems, input-current sharing (ICS) between the different modules satisfies output-voltage sharing (OVS) and vice versa.

Table 3 Power module characteristics

Parameter	Value
n_{ac}	6
n_{dc}	4
N_{dc}	72
voltage stress (rectifier)	695 V
voltage stress (DC converters)	695 V
current stress (rectifier)	1 kA (peak)
current stress (DC converters)	100 A
switching frequency f_s	50 kHz
DAB inductance value *L*	13 μH
operational duty ratio *D*	0.25
transformer turns ratio *n*	1
L_{ac}	100 μH
C_{ac}	180 μF
C_{dc1} and C_{dc2}	2 μF

However, it is reported in [22] that OVS cannot be stable for this configuration. In this work, ICS is achieved using decentralised droop controllers where the individual output voltages and input currents are sensed. Note that the total output voltage is controlled by the aforementioned overall DC controller. The droop controller for module 1 is shown in Fig. 4*a*. The main purpose of the proposed controller is to ensure that the total voltage of the cluster ($V_{dc}/3n_{ac}$) is equally distributed across the individual output voltages of the modules ($v_{o_a1_1}$, $v_{o_a1_2}$, …, $v_{o_a1_ndc}$). Taking module 1 as an example, the reference voltage $V_{ref_a1_1}$ is calculated from the actual total voltage V_{dc}.

It is important to highlight the relationship between the duty ratio of the DC/DC modules and their currents and voltages. Under steady-state conditions, the relationship between the output and input voltages and currents can be written as

$$\begin{cases} v_{o_a1_1} = f(d_{a1_1}) v_{m_a1} \\ v_{o_a1_2} = f(d_{a1_2}) v_{m_a1} \\ \vdots \\ v_{o_a1_ndc} = f(d_{a1_ndc}) v_{m_a1} \end{cases} \tag{6}$$

For DAB circuits, $f(d_{a1_i})$ is an increasing function of d_{a1_i}. From the power balance equations

$$\begin{cases} i_{indc_a1_1} = f(d_{a1_1}) I_{dc} \\ i_{indc_a1_2} = f(d_{a1_2}) I_{dc} \\ \vdots \\ i_{indc_a1_ndc} = f(d_{a1_ndc}) I_{dc} \end{cases} \tag{7}$$

For module number *k* in the group, the proportion of individual input current $i_{indc_a1_k}$ to the total input current of the group I_{indc_a1} can be expressed as

$$P_k = \frac{i_{indc_a1_k}}{i_{indc_a1}} = \frac{f(d_{a1_k}) I_{dc}}{\sum_{j=1}^{n_{dc}} f(d_{a1_j}) I_{dc}} = \frac{f(d_{a1_k})}{f(d_{a1_k}) + \sum_{j=1, j \neq k}^{n_{dc}} f(d_{a1_i})} \tag{8}$$

From (8), a perturbation increase in the duty ratio of module *k* leads to an increase in its input current. In other words, the individual input current $i_{indc_a1_k}$ and individual output voltage $v_{o_a1_k}$ are monotonous increasing functions of the duty ratio d_{a1_k}. As depicted in Fig. 4*a*, the duty ratio of Mod_a1_1 is composed of two parts, namely *d* and d_{sha1_1}. *d* is common for all different modules and generated from the overall central controller, whereas d_{sha1_1} is generated from the IPOS sharing controller for Mod_a1_1. Assume that all the converters have the same parameters and that Mod_a1_1 is operating at the equilibrium point 'O' as shown in Fig. 4*b*. The module output voltage $v_{o_a1_1}$ then increases as the result of a perturbation. Due to output current I_{dc} passes through all modules, Mod_a1_1 will now be delivering increased power. Consequently, $i_{indc_a1_1}$ will start to increase and the operating point moves to 'A'. However, the controller will force d_{sha1_1} to decrease because of the negative feedback of the controller at summing point 1 (Fig. 4*a*), leading the operation point to move back towards 'O'. The opposite operation is true for point '*B*' when $v_{o_a1_1}$ decreases.

The ICS PI controller $G_{sh_dc}(s)$ can be expressed as

$$G_{dc}(s) = \frac{I_{dc}}{d} = \frac{LC_1 V_{dc1} f_s r_1 (1 - 2D)s - (2D - 1)(V_{dc2} r_2 D(D - 1) + LV_{dc2} f_s)}{(C_1 C_2 L^2 f_s^2 r_1 r_2)s^2 + L^2 f_s^2 (C_1 r_1 + C_2 r_2)s + r_1 D^2 (r_2 D^2 - 2r_2 D + r_2) + L^2 f_s^2} \tag{3}$$

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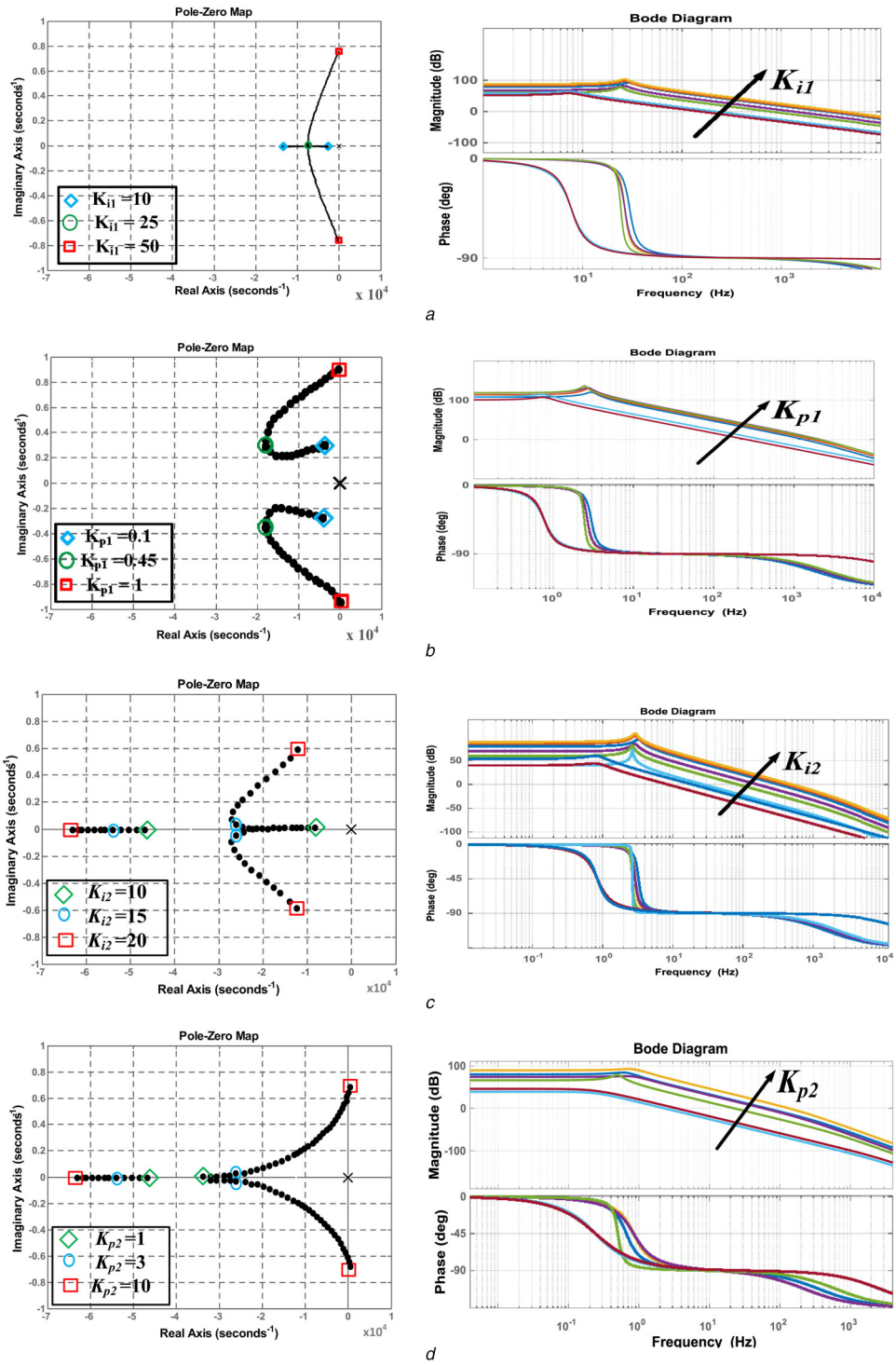

Fig. 2 *Frequency domain analysis of overall DC/DC converters*
(a) Closed-loop pole-zero map and open-loop Bode plot ($K_{p1} = 0.5$ and $K_{i1} = [10 : 50]$), ***(b)*** Closed-loop pole-zero map and open-loop Bode plot ($K_{i1} = 15$ and $K_{p1} = [0.1:1]$), ***(c)*** Closed-loop pole-zero map and open-loop Bode plot ($K_{p2} = 3$ and $K_{i2} = [10:20]$), ***(d)*** Closed-loop pole-zero map and open-loop Bode plot ($K_{i2} = 15$ and $K_{p2} = [1:10]$)

$$G_{sh_dc}(s) = K_{p_sh1} + \frac{K_{i_sh1}}{s} \tag{9}$$

The transfer function of the closed-loop system $T_{sh1}(s)$ can be deduced from

$$g_{11}(s) = \frac{\tilde{v}_{o_a1_1}}{\tilde{v}_{r_a1_1}} = \frac{G_{sh_dc}(s)G_{23}(s)}{1 + G_{sh_dc}(s)G_{23}(s)} \tag{10.1}$$

$$\tilde{v}_{r_a1_1} = \tilde{V}_{ref_a1_1} - K_d\,\tilde{i}_{indc_a1_1} \tag{10.2}$$

$$T_{sh}(s) = \frac{\tilde{v}_{o_a1_1}}{\tilde{V}_{ref_a1_1}} = \frac{g_{11}(s)}{1 + K_d g_{11}(s) g_{13}(s)} \tag{10.3}$$

where

$$g_{13}(s) = \frac{\tilde{i}_{indc_a1_1}}{\tilde{v}_{o_a1_1}} = G_{11}(s)/G_{14}(s) = \frac{(C_1C_2L^2f_s^2r_2)s^2 + L^2f_s^2C_1s + D^2(r_2D^2 - 2r_2D + r_2)}{L^2f_s^2(sC_2r_2 + 1)} \tag{10.4}$$

The droop gain K_d affects the gradient of the droop controller regulation characteristic and hence, increasing its value can

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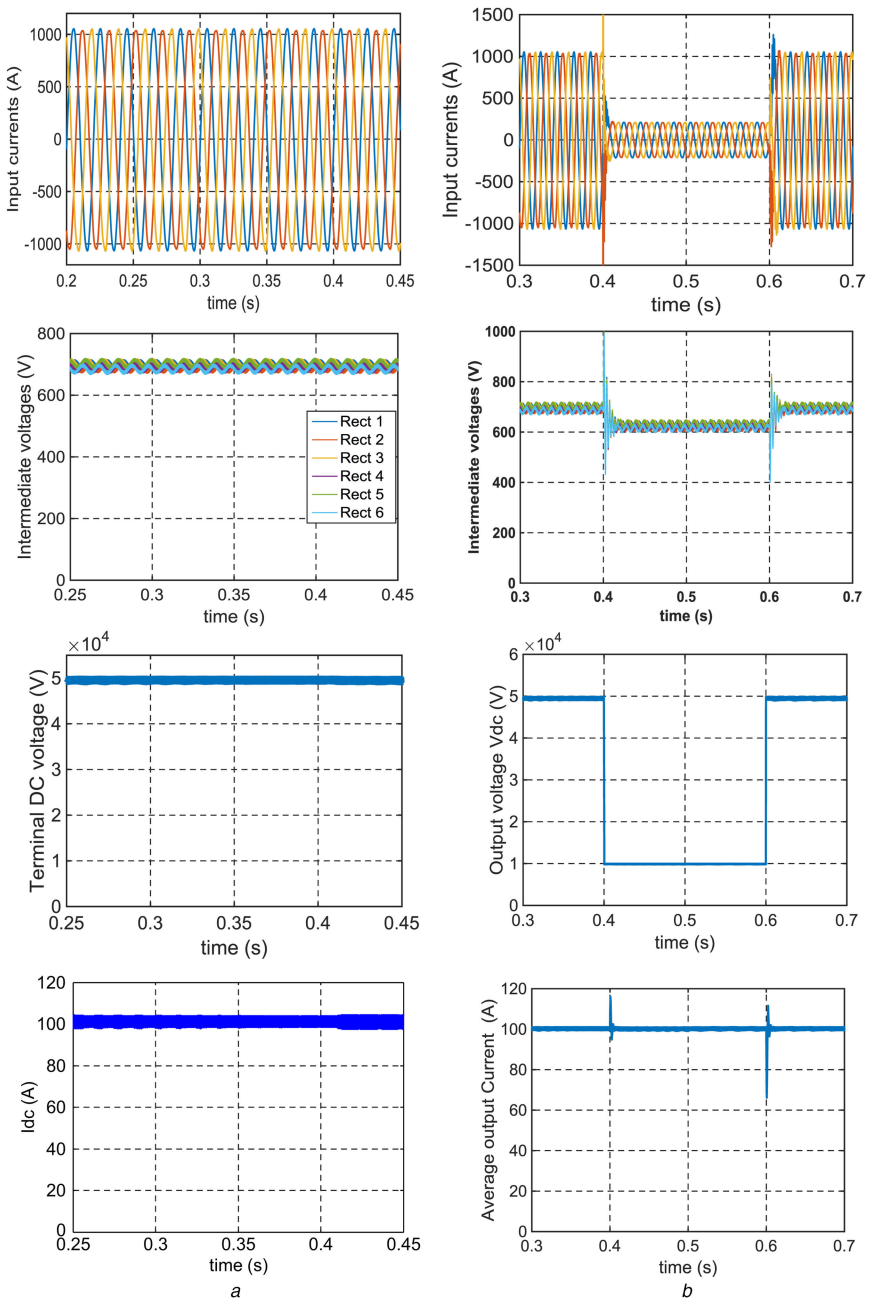

Fig. 3 *MATLAB simulations of AC/DC ISIPOS system*
(a) Normal operation, ***(b)*** With 80% sudden drop in terminal voltage

theoretically provide faster current sharing. To avoid prolongation, examination of the specific effect of K_d on the sensitivity of the sharing technique will be postponed until a future publication. The stability limits of the controller gains K_{p_sh1}, K_{i_sh1} and K_d can be found using the Routh–Hurwitz stability criterion or using the MATLAB/SISOTOOL toolbox. Fig. 5 shows the closed-loop pole trajectories in response to variation of the controller gain K_{p_sh1} and with different values of K_{i_sh1} and K_d. The values are changed until the desired characteristics of the controller are been found. These characteristics should achieve the lowest oscillation, stable operation, and increased bandwidth in comparison with the overall DC controller mentioned in Section 2. With this large bandwidth, the DC converter sharing techniques should not affect the main overall control of active power transfer. The gain values are selected as $K_{p_sh1} = 25$, $K_{i_sh1} = 200$ and $K_d = 500$ to provide relatively stable operation and bandwidth equal to ten times that of the overall DC controller.

3.2.2 ISOS AC/DC converter controller: Considering AC/DC converter group of phase a as a case study, the input voltages (v_{in_a1}, v_{in_a2}, …, v_{in_anac}) and the output voltages (v_{m_a1}, v_{m_a2}, …, v_{m_anac}) have to be shared equally. Generally for input–parallel connected systems, input-voltage sharing (IVS) is sufficient to achieve OVS [23]. Under steady-state conditions, the relationship between the output and input voltages can be written as

$$\begin{cases} v_{m_a1} = f(\delta_{a1})v_{in_a1} \\ v_{m_a2} = f(\delta_{a2})v_{in_a2} \\ \vdots \\ v_{m_anac} = f(\delta_{anac})v_{in_anac} \end{cases} \tag{11}$$

For module number k in the group, the proportion of individual input voltage v_{in_ak} to the total input voltage of the group v_{ina} can be expressed as

$$S_k = \frac{v_{in_ak}}{v_{ina}} = \frac{1}{1 + f(\delta_{ak})\sum_{j=1, j\neq k}^{n_{dc}} f(\delta_{aj})} \tag{12}$$

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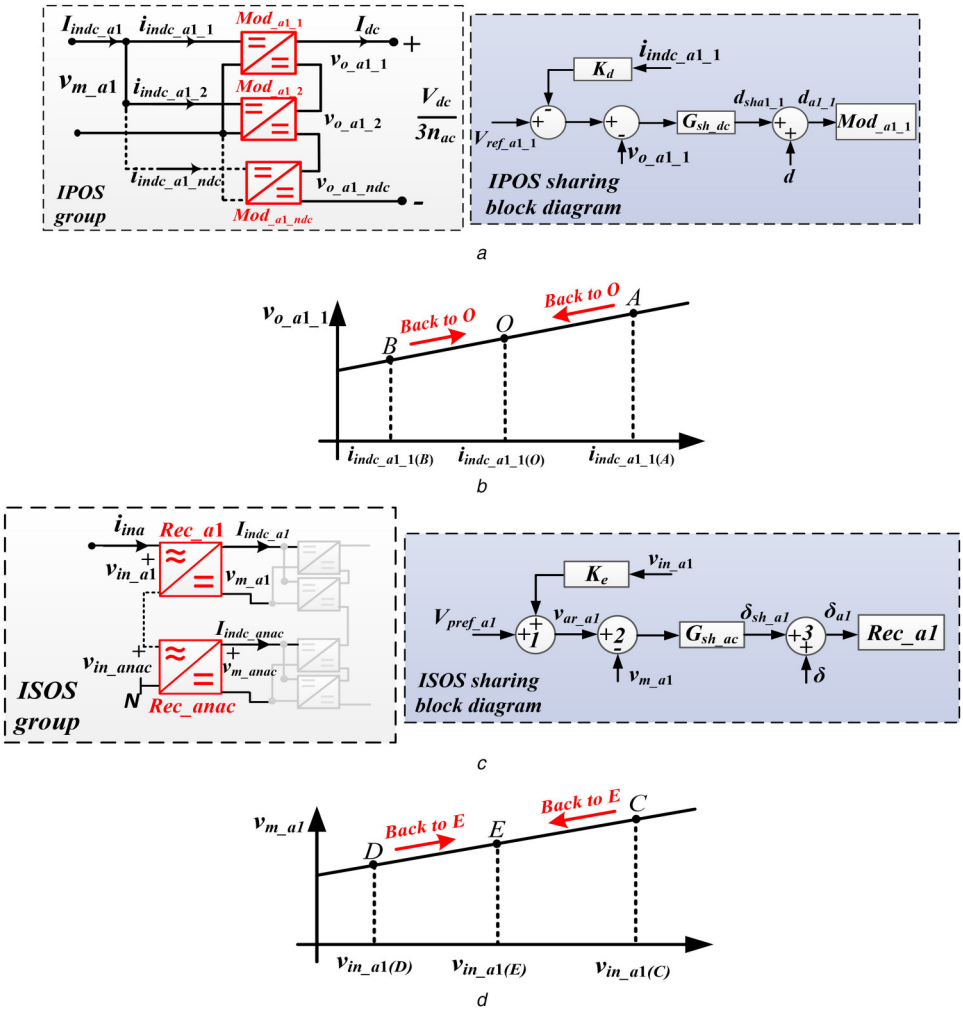

Fig. 4 *Converters and rectifier power sharing*
(a) Block diagram of IPOS droop controller, ***(b)*** Regulation characteristic of IPOS controller, ***(c)*** Block diagram of ISOS droop controller, ***(d)*** Regulation characteristic of ISOS controller

From (12), a perturbation increase in the duty ratio of module k leads to a decrease in its input voltage in relation to the other rectifier input voltages. As depicted in Fig. 4*c*, the duty ratio of Rec_a1 is composed of two parts, namely δ and δ_{sh_a1}. δ is common for all phase a rectifiers and generated from the overall central controller while δ_{sh_a1} is generated from the ISOS sharing controller for Rec_a1.

In this research, IVS can be achieved using the decentralised droop controllers shown in Fig. 4*c*. Unlike the previous IPOS sharing technique, the ISOS technique has positive feedback at summing point 1 (Fig. 4*c*) in order to give the positive droop regulation characteristics as shown in Fig. 4*d*. The IVS PI controller $G_{sh_ac}(s)$ can be expressed as

$$G_{sh_ac}(s) = K_{p_sh2} + \frac{K_{i_sh2}}{s} \tag{13}$$

The transfer function of the closed-loop system $H_{sh1}(s)$ can be deduced from

$$g_{21}(s) = \frac{\tilde{v}_{m_a1}}{\tilde{v}_{ar_a1}} = \frac{G_{sh_ac}(s)g_{rec}(s)}{1 + G_{sh_ac}g_{rec}(s)} \tag{14.1}$$

$$g_{rec}(s) = \frac{\tilde{v}_{m_a1}}{\tilde{\delta}_{sh_a1}} = \frac{G_{14}(s)}{G_{14}(s)\cdot(1 + C_{ac}L_{ac}s^2) + L_{ac}s} \tag{14.2}$$

$$\tilde{V}_{ar_a1} = \tilde{V}_{pref_a1} + K_e\tilde{v}_{in_a1} \tag{14.3}$$

$$H_{sh}(s) = \frac{\tilde{v}_{m_a1}}{\tilde{v}_{pref_a1}} = \frac{g_{21}(s)}{1 - K_e g_{21}(s)g_{rec}(s)} \tag{14.4}$$

The same approach as that for the IPOS sharing technique with the analysis shown in Fig. 5 was followed, and the controller gains are selected as $K_{p_sh2} = 5$, $K_{i_sh2} = 120$ and $K_e = 750$ to provide relatively stable operation and a bandwidth equal to seven times that of the overall AC controller. The presented sharing methods are decoupled from the power transfer process and they do not require communication between the different modules and rectifiers. The system modularity and flexibility are therefore improved. The regulation features of the sharing controllers are not affected by the variation of input and output voltages or currents. The sharing controllers can achieve IVS and ICS of the AC/DC rectifiers and DC/DC modules during transients and under steady-state conditions.

Figs. 6*a* and *b* show the MATLAB simulations of the sharing technique for one IPOS group consisting of four of the DC/DC DAB converters shown in Fig. 4*a*.

At $t = 0.1$ s, a perturbation occurs and output voltage v_{o1} increases. It can be seen that the total output voltage was not significantly affected and the controller succeeded in restoring normal operation. Figs. 6*c* and *d* show the MATLAB simulations of the sharing techniques for one ISOS group consisting of four DC/AC rectifiers. At $t = 0.1$ s, a perturbation occurs and output voltage v_{m1} increases. The controller is able to share the output voltage between the different rectifiers equally.

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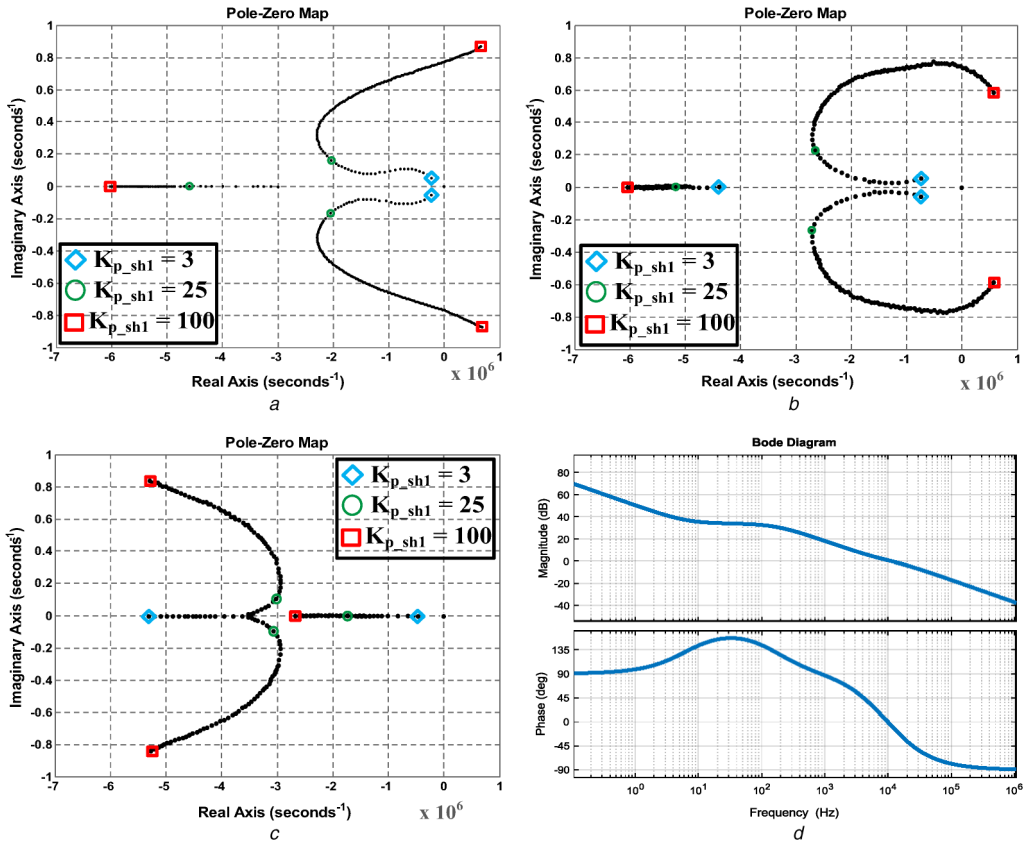

Fig. 5 *Variation of IPOS DC converter closed-loop poles with controller proportional gain K_{p_sh1}*

(a) $K_d = 100$, $K_{i_sh1} = 200$, $K_{p_sh1} = 3,\ldots,100$, ***(b)*** $K_d = 500$, $K_{i_sh1} = 200$, $K_{p_sh1} = 3,\ldots,100$, ***(c)*** $K_d = 500$, $K_{i_sh1} = 200$, $K_{p_sh1} = 3,\ldots,100$, ***(d)*** open-loop Bode plot at $K_d = 500$, $K_{i_sh1} = 200$ and $K_{p_sh1} = 25$

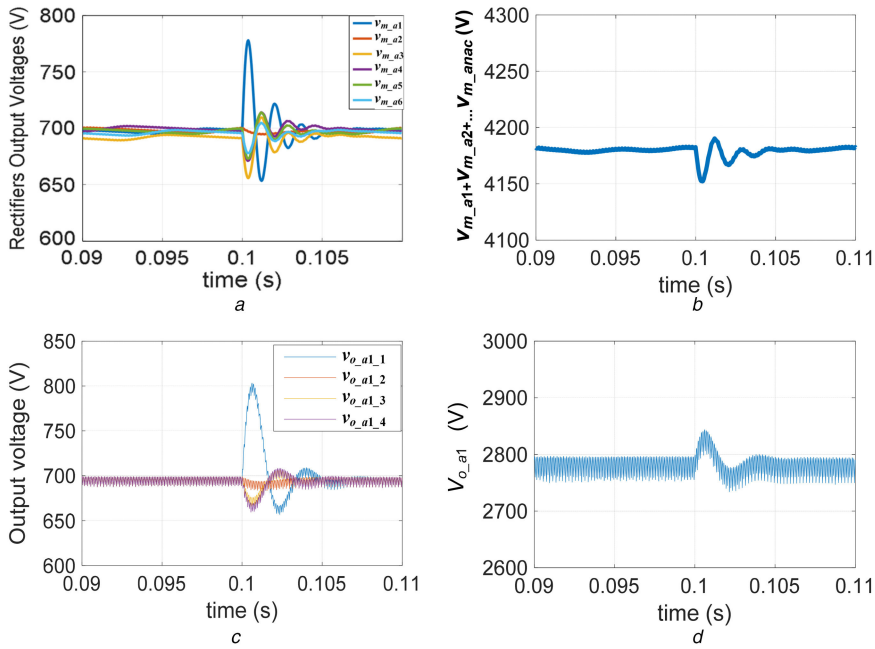

Fig. 6 *Simulated output voltage of ISOS and IPOS sharing technique during voltage perturbations*

(a) Individual output voltages of one ISOS group, ***(b)*** Total output voltage of one ISOS group, ***(c)*** Individual output voltages of one IPOS group, ***(d)*** Total output voltage of one IPOS group

4 Experimental results

A 1 kW prototype controlled with TMS320F28335DSP was built, as shown in Fig. 7*a*, to validate the presented concept, mathematical analysis and control schemes. The system parameters in this case are shown in Table 4. FGY75N60SMD IGBTs have been employed for the semiconductor switches while RURG3060 diodes have been used for the anti-parallel diodes. During the normal operation shown in Figs. 7*b* and *c*, power is transferred from the input AC side to the output DC side through the ISIPOS system. Fig. 7*b*(i) shows that phase *a* current i_{ina} is in phase with the input AC voltage v_{ina}. However, the power factor is controlled over the full range according to the operation. Fig. 7*b*(ii) shows the output voltages of the rectifiers. As shown, these voltages have oscillating components beside the desired DC components. However, as long as these components are small they will not affect the normal operation of the system as the rectifier voltage

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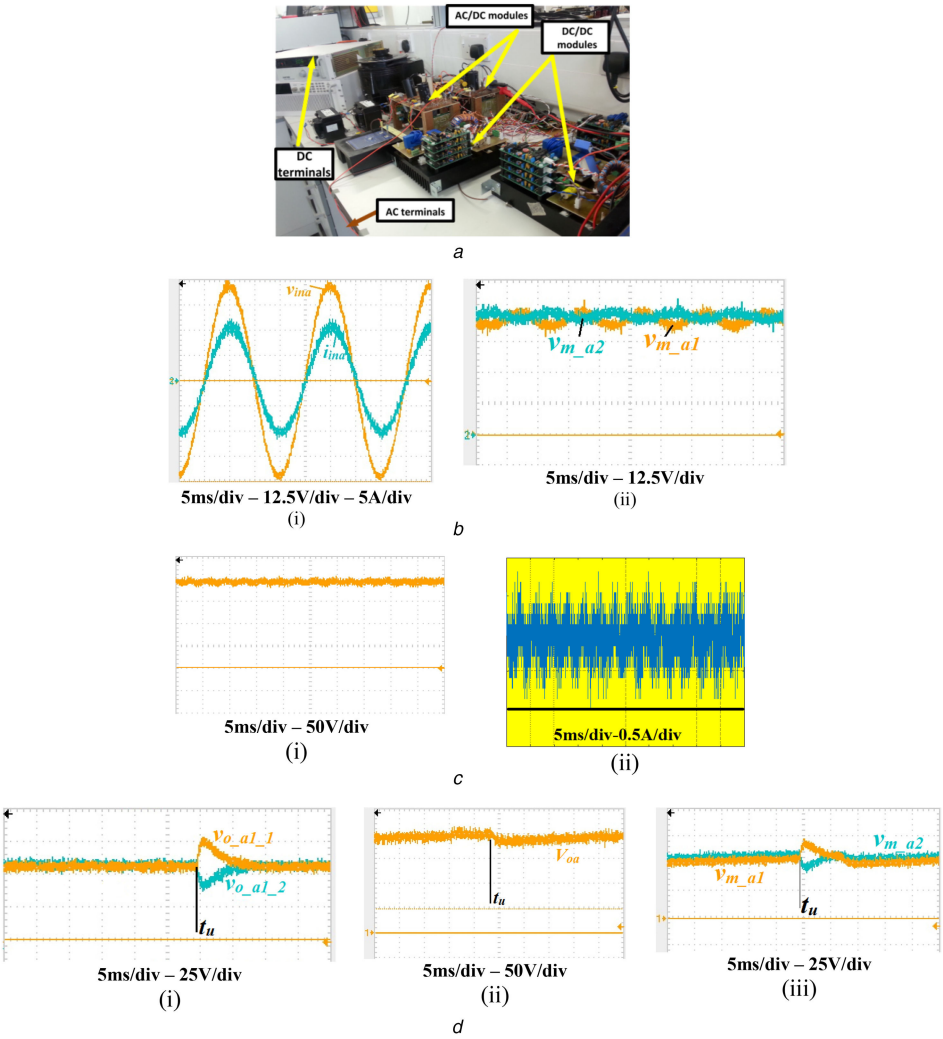

Fig. 7 *Experimental results*

(a) Experimental setup, ***(b)*** (i) input current with input voltage and (ii) rectifiers output voltages, ***(c)*** (i) total output voltage from phase *a* and (ii) sampled output current from the controller, ***(d)*** (i) and (ii) IPOS sharing technique and (iii) ISOS sharing technique

Table 4 Circuit conditions of experimental setup

Parameter	Value
n_{ac} and n_{dc}	2
switching frequency f_s	50 kHz
DAB inductance value L	30 μH
transformer turns ratio n	1
L_{ac} and C_{ac}	1 mH and 45 μF
C_{dc1} and C_{dc2}	20 μF
v_{in} and i_{in}	50 V and 10 A (peak)
K_{p1} and K_{i1}	0.25 and 10
K_{p2} and K_{i2}	1 and 8
K_{p_sh1}, K_{i_sh1} and K_d	10, 80 and 200
K_{p_sh2}, K_{i_sh2} and K_e	2, 40 and 300

will be converted using the next stage (IPOS groups). Fig. 7*c*(i) shows the output DC voltage of the system, whereas Fig. 7*c*(ii) shows the output current. The oscillating component of the output current can be eliminated either by increasing the value of output filter capacitance or by using simple resonant controllers tuned at the oscillation frequency. The efficiency of the total system is 95% in this case. The results can be compared with the MATLAB simulations in Fig. 3. Fig. 7*d* shows the results when an intended unbalance occurs at time instant 't_u' in the first module of the IPOS DC/DC converter in phase *a*. In Fig. 7*d*(i), the output voltages of the DC/DC modules were forced back to the equilibrium operating point again after a very short duration by the sharing controllers. Fig. 7*d*(ii) shows that the total output of the DC/DC group of phase '*a*' has not been significantly affected by the sudden unbalance. Fig. 7*d*(iii) shows that the output voltages of the ISOS AC/DC rectifiers in phase *a* have been restored to their desired equal sharing values shortly after the sudden unbalance.

5 Conclusion

In this paper, control schemes suitable for a modular ISIPOS AC/DC energy conversion system are presented and analysed. ISIPOS AC/DC converters are considered as promising solutions for medium-voltage high-power wind energy applications. However, because of their modularity, they can be extended to other applications, such as high-voltage high-power applications. Unfortunately, because the ISIPOS energy conversion system consists of many stages, control design becomes complicated and not straight forward. In this research, the control scheme comprises two main parts, namely, overall control and module-level control. In the overall AC/DC converter control, the series connected AC/DC rectifiers of the input–parallel output-series connected modules are viewed as equivalent AC/DC and DC/DC modules, and the mismatches between the system parameters are neglected. The duty ratios of the different modules are fed from central controllers. In the module-level controllers, each module has its own controller to cater for small mismatches between the different parameters, and to ensure equal voltage and current sharing between the power converters. System-level MATLAB simulations have been conducted to show the effectiveness of the proposed controller design. In addition, scaled-down experiments verify the

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presented mathematical analysis and simulation results using a 1 kW prototype controlled with TMS320F280335 digital signal processor.

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8 Appendix

8.1 Average model of bidirectional DAB

Operation when the DAB is controlled with PSC can be explained as shown in Fig. 8*b*. The state-space representation can be arranged as

i I: $0 < t \le Dt_s$

$$\begin{bmatrix} \frac{dV_1}{dt} \\ \frac{di_L}{dt} \\ \frac{dV_2}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-1}{r_1C_1} & \frac{-1}{C_1} & 0 \\ \frac{1}{L} & 0 & \frac{1}{nL} \\ 0 & \frac{-1}{nC_2} & \frac{-1}{r_2C_2} \end{bmatrix} \begin{bmatrix} V_1 \\ i_L \\ V_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{r_1C_1} & 0 \\ 0 & 0 \\ 0 & \frac{1}{r_2C_2} \end{bmatrix} \begin{bmatrix} V_{dc1} \\ V_{dc2} \end{bmatrix} \tag{15}$$

ii II: $Dt_s < t \le (1-D)t_s$

$$\begin{bmatrix} \frac{dV_1}{dt} \\ \frac{di_L}{dt} \\ \frac{dV_2}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-1}{r_1C_1} & \frac{-1}{C_1} & 0 \\ \frac{1}{L} & 0 & \frac{-1}{nL} \\ 0 & \frac{1}{nC_2} & \frac{-1}{r_2C_2} \end{bmatrix} \begin{bmatrix} V_1 \\ i_L \\ V_2 \end{bmatrix} + \begin{bmatrix} \frac{1}{r_1C_1} & 0 \\ 0 & 0 \\ 0 & \frac{1}{r_2C_2} \end{bmatrix} \begin{bmatrix} V_{dc1} \\ V_{dc2} \end{bmatrix} \tag{16}$$

Operation in durations (I and II) is symmetrical to that during (III and IV), so durations I and II will be considered.

It can be noted that two states, namely V_1 and V_2, are varying much more slowly than the third variable i_L. So, the system under investigation is a two-time scale system [24].

Equating (di_L/dt) to zero and substituting for i_L in (dV_1/dt) and (dV_2/dt), the equations yield

$$\left.\begin{aligned} \frac{dV_1}{dt} &= \frac{1}{r_1C_1}V_{dc1} - \frac{1}{r_1C_1}V_1 - \frac{1}{C_1}i_L \\ \frac{dV_2}{dt} &= \frac{1}{r_2C_2}V_{dc2} - \frac{1}{r_2C_2}V_1 - \frac{1}{nC_2}i_L \\ i_L &= \frac{V_1 + V_2/n}{L}t + \frac{1}{2f_sL}[(1-2D) - nV_1]) \end{aligned}\right\} 0 < t \le Dt_s \tag{17}$$

where

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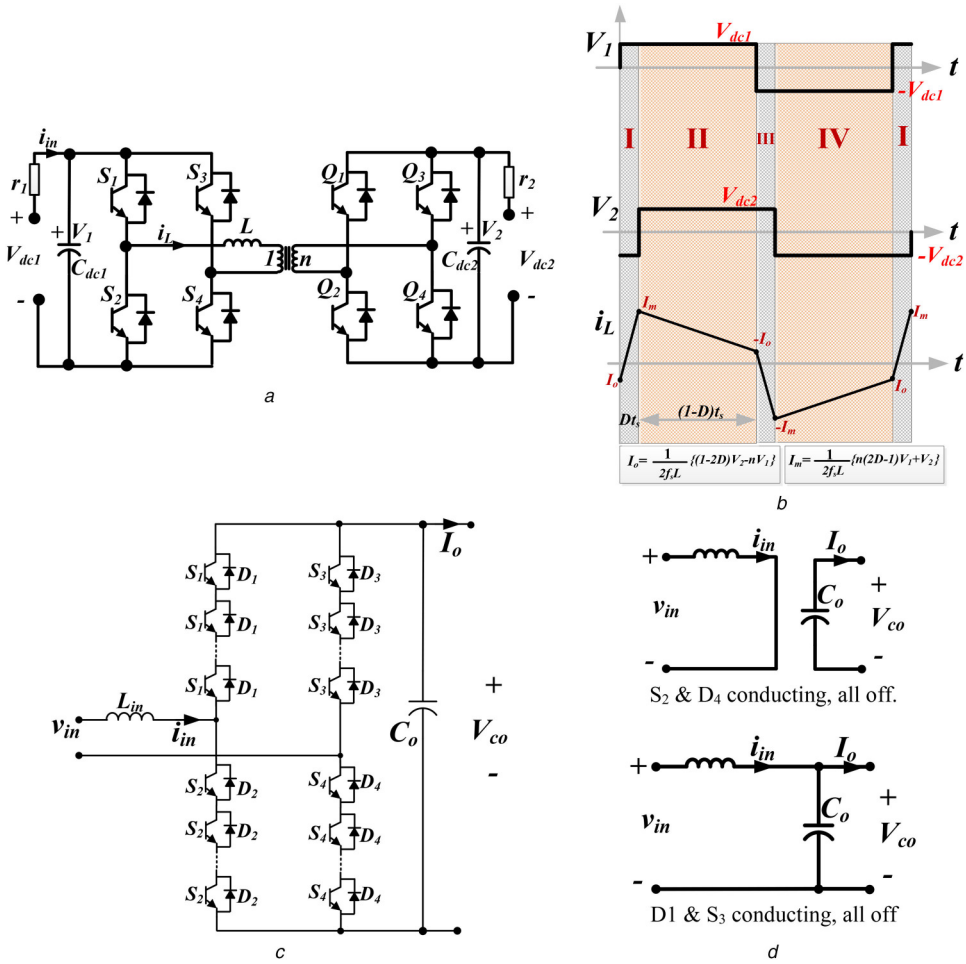

Fig. 8 *DAB and AC/DC rectifiers*
(a) Simplified DAB circuit, ***(b)*** DAB operation with PSC, ***(c)*** AC/DC bidirectional converter, ***(d)*** AC/DC bidirectional converter operating modes (positive half cycle of i_{in})

$$\left.\begin{aligned}\frac{dV_1}{dt} &= \frac{1}{r_1C_1}V_{dc1} - \frac{1}{r_1C_1}V_1 - \frac{1}{C_1}i_L\\ \frac{dV_2}{dt} &= \frac{1}{r_2C_2}V_{dc2} - \frac{1}{r_2C_2}V_1 + \frac{1}{nC_2}i_L\\ i_L &= \frac{V_1 - V_2/n}{L}(t - Dt_s) + \frac{1}{2f_sL}[V_2 - n(1-2D)V_1])\end{aligned}\right\} Dt_s \tag{18}$$

$< t \le t_s$

Arranging and averaging over the period t_s gives

$$\begin{bmatrix}\frac{d\bar{V}_1}{dt}\\ \frac{d\bar{V}_2}{dt}\end{bmatrix} = \begin{bmatrix}\frac{-1}{r_1C_1} & \frac{D^2-D}{Lf_sC_1}\\ \frac{D-D^2}{Lf_sC_2} & \frac{-1}{r_2C_2}\end{bmatrix}\begin{bmatrix}\bar{V}_1\\ \bar{V}_2\end{bmatrix} + \begin{bmatrix}\frac{1}{r_1C_1} & 0\\ 0 & \frac{1}{r_2C_2}\end{bmatrix}\begin{bmatrix}V_{dc1}\\ V_{dc2}\end{bmatrix} \tag{19}$$

8.2 DAB converter small-signal model

The equations in (19) can be written as

$$\begin{aligned}\frac{dV_1}{dt} &= \underbrace{\frac{-1}{r_1C_1}V_1 + \frac{D^2-D}{Lf_sC_1}V_2 + \frac{1}{r_1C_1}V_{dc1}}_{f_1}\\ \frac{dV_2}{dt} &= \underbrace{\frac{D-D^2}{Lf_sC_2}V_1 + \frac{-1}{r_2C_2}V_2 + \frac{1}{r_2C_2}V_{dc2}}_{f_2}\end{aligned} \tag{20}$$

The small-signal model can be expressed as [25, 26]

$$\begin{bmatrix}\frac{d\tilde{v}_1}{dt}\\ \frac{d\tilde{v}_2}{dt}\end{bmatrix} = \begin{bmatrix}\frac{\partial f_1}{\partial V_1} & \frac{\partial f_1}{\partial V_2}\\ \frac{\partial f_2}{\partial V_1} & \frac{\partial f_2}{\partial V_2}\end{bmatrix}\begin{bmatrix}\tilde{v}_1\\ \tilde{v}_2\end{bmatrix} + \begin{bmatrix}\frac{\partial f_1}{\partial V_{dc1}} & \frac{\partial f_1}{\partial V_{dc2}} & \frac{\partial f_1}{\partial d}\\ \frac{\partial f_2}{\partial V_{dc1}} & \frac{\partial f_2}{\partial V_{dc2}} & \frac{\partial f_2}{\partial d}\end{bmatrix}\begin{bmatrix}\tilde{v}_{dc1}\\ \tilde{v}_{dc2}\\ d\end{bmatrix} \tag{21}$$

Hence

$$\begin{bmatrix}\frac{d\tilde{v}_1}{dt}\\ \frac{d\tilde{v}_2}{dt}\end{bmatrix} = \begin{bmatrix}\frac{-1}{r_1C_1} & \frac{D^2-D}{Lf_sC_1}\\ \frac{D-D^2}{Lf_sC_2} & \frac{-1}{r_2C_2}\end{bmatrix}\begin{bmatrix}\tilde{v}_1\\ \tilde{v}_1\end{bmatrix} + \begin{bmatrix}\frac{1}{r_1C_1} & 0 & \frac{2D-1}{Lf_sC_1}V_2\\ 0 & \frac{1}{r_2C_2} & \frac{1-2D}{Lf_sC_2}V_1\end{bmatrix}\begin{bmatrix}\tilde{v}_{dc1}\\ \tilde{v}_{dc2}\\ d\end{bmatrix} \tag{22}$$

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Therefore, the small-signal transfer functions of the system can be expressed as (see (23a))
(see (23b))
(see (23c))
(see (23d))
(see (24a))
(see (24b))
(see (24c))

8.3 Bidirectional AC/DC converter average model

The state-space representation of the circuit can be expressed as

$$\begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} \\ \frac{\mathrm{d}V_{\mathrm{co}}}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L_{\mathrm{in}}} \\ \frac{1}{C_{\mathrm{o}}} & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{in}} \\ V_{\mathrm{co}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{\mathrm{in}}} & 0 \\ 0 & \frac{-1}{C_{\mathrm{o}}} \end{bmatrix} \begin{bmatrix} v_{\mathrm{in}} \\ I_{\mathrm{o}} \end{bmatrix} \tag{25}$$

δ: i_{in} decreases and V_{co} increases (25)

$$\begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{in}}}{\mathrm{d}t} \\ \frac{\mathrm{d}V_{\mathrm{co}}}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{in}} \\ V_{\mathrm{co}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{\mathrm{in}}} & 0 \\ 0 & \frac{-1}{C_{\mathrm{o}}} \end{bmatrix} \begin{bmatrix} v_{\mathrm{in}} \\ I_{\mathrm{o}} \end{bmatrix} \tag{26}$$

$1-\delta$: i_{in} increases and V_{co} decreases (26).

Similarly, the average equations of the AC/DC rectifier can be written as

$$\tilde{v}_{\mathrm{co}} = \frac{\tilde{\delta}}{1 + C_{\mathrm{o}}L_{\mathrm{in}}s^2}V_{\mathrm{in}} - \frac{L_{\mathrm{in}}s}{1 + C_{\mathrm{o}}L_{\mathrm{in}}s^2}\tilde{i}_{\mathrm{o}} \tag{27}$$

Equation (27) can be rewritten as

$$\tilde{v}_{\mathrm{co}} = \frac{\tilde{\delta}}{1 + C_{\mathrm{o}}L_{\mathrm{in}}s^2}V_{\mathrm{in}} - \frac{L_{\mathrm{in}}s}{1 + C_{\mathrm{o}}L_{\mathrm{in}}s^2}\frac{\tilde{v}_{\mathrm{co}}}{G_{14}} \tag{28}$$

Rearranging (28)

$$\begin{aligned} G_{11}(s) &= \frac{\tilde{v}_1}{\tilde{v}_{\mathrm{dc1}}} \\ &= \frac{\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{sC}_2\mathrm{r}_2 + 1)}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{S}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{23a}$$

$$\begin{aligned} G_{12}(s) &= \frac{\tilde{v}_1}{\tilde{v}_{\mathrm{dc2}}} \\ &= \frac{\mathrm{DLf}_{\mathrm{s}}\mathrm{r}_1(\mathrm{D} - 1)}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{23b}$$

$$\begin{aligned} G_{13}(s) &= \frac{\tilde{v}_1}{d} \\ &= \frac{LC_2\mathrm{V}_{\mathrm{dc2}}\mathrm{f}_{\mathrm{s}}\mathrm{r}_1\mathrm{r}_2(2\mathrm{D} - 1)\mathrm{s} + \mathrm{r}_1(2\mathrm{D} - 1)(\mathrm{V}_1\mathrm{r}_2\mathrm{D}(1 - \mathrm{D}) + LV_{\mathrm{dc1}}\mathrm{f}_{\mathrm{s}})}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{23c}$$

$$\begin{aligned} G_{14}(s) &= \frac{\tilde{i}_{\mathrm{in}}}{\tilde{v}_{\mathrm{dc1}}} \\ &= \frac{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{fs}^2\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{C}_1 s + \mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2)}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{23d}$$

$$\begin{aligned} G_{21}(s) &= \frac{\tilde{v}_2}{\tilde{v}_{\mathrm{dc1}}} \\ &= \frac{\mathrm{Lf}_{\mathrm{s}}\mathrm{r}_2 D(1 - D)}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{24a}$$

$$\begin{aligned} G_{22}(s) &= \frac{\tilde{v}_2}{\tilde{v}_{\mathrm{dc2}}} \\ &= \frac{\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{sC}_1\mathrm{r}_1 + 1)}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{24b}$$

$$\begin{aligned} G_{23}(s) &= \frac{\tilde{v}_2}{d} \\ &= \frac{\mathrm{LC}_1\mathrm{V}_{\mathrm{dc1}}\mathrm{f}_{\mathrm{s}}\mathrm{r}_1\mathrm{r}_2(1 - 2\mathrm{D})\mathrm{s} - \mathrm{r}_2(2\mathrm{D} - 1)(\mathrm{V}_{\mathrm{dc2}}\mathrm{r}_2\mathrm{D}(\mathrm{D} - 1) + \mathrm{LV}_{\mathrm{dc2}}\mathrm{f}_{\mathrm{s}})}{(\mathrm{C}_1\mathrm{C}_2\mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2\mathrm{r}_1\mathrm{r}_2)\mathrm{s}^2 + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2(\mathrm{C}_1\mathrm{r}_1 + \mathrm{C}_2\mathrm{r}_2)\mathrm{s} + \mathrm{r}_1\mathrm{D}^2(\mathrm{r}_2\mathrm{D}^2 - 2\mathrm{r}_2\mathrm{D} + \mathrm{r}_2) + \mathrm{L}^2\mathrm{f}_{\mathrm{s}}^2)} \end{aligned} \tag{24c}$$

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$$G_{ac}(s) = \frac{\tilde{v}_{oc}}{\tilde{\delta}} = \frac{G_{14}}{G_{14}(1 + C_o L_{in} s^2) + L_{in} s} V_{in} \qquad (29)$$

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