Neurocomputing 155 (2015) 153–158

Contents lists available at ScienceDirect

Neurocomputing

journal homepage: www.elsevier.com/locate/neucom

Brief Papers

Emulation of spike-timing dependent plasticity in nano-scale phase change memory

Dae-Hwan Kang [a], Hyun-Goo Jun [a], Kyung-Chang Ryoo [a], Hongsik Jeong [b,*], Hyunchul Sohn [c]

[a] Memory Division, Semiconductor Business, Samsung Electronics Co. Ltd., 1, Samsungjeonja-ro, Hwaseong-si, Gyeonggi-Do 445-330, Korea
[b] Yonsei Institute of Convergence Technology, Yonsei University, 85 Songdogwahak-ro, Yeonsu-gu, Incheon 406-840, Korea
[c] Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea

ARTICLE INFO

Article history:
Received 27 July 2014
Received in revised form
20 September 2014
Accepted 18 December 2014
Communicated by: Witali Dunin-Barkowski
Available online 6 January 2015

Keywords:
Spike-timing dependent plasticity
Two-phase change memory cells
Long-term potentiation
Long-term depression
Electronic synapses

ABSTRACT

The spike-timing dependent plasticity (STDP) of biological synapses, which is known to be a function of the formulated Hebbian learning rule of human cognition, learning and memory abilities, was emulated with two-phase change memory (2-PCM) cells built with 39 nm technology. For this, we designed a novel time-modulated voltage (TMV) scheme for changing the conductance of 2-PCM cells, that could produce both long-term potentiation (LTP) and long-term depression (LTD) by applying variable (decreasing/increasing) pulse voltages according to the sign and magnitude in time interval between pre- and post-spikes. Since such schemes can be easily modified to have a variety of pulse shapes and time intervals between pulses, it is expected to be a proper scheme for designing diverse synaptic connection abilities. In addition, the small form factor and low energy consumption of 2-PCM make them comparable to biological synapses, which makes phase change memory a promising candidate for electronic synapses in large-scale neuromorphic system applications.

1. Introduction

The term neuromorphic engineering, which was coined by Carver Mead [1], has given rise to significant progress in the uprising application fields of brain-inspired computing, smart sensors, and associate memory, which is based on CMOS analog, digital and/or combined circuits, called silicon neural networks (SiNs). These networks mimic the information processing pathways of biological neurons such as signal reception, propagation, transference to neighboring neurons, and storage [2–4].

Fig. 1(a) shows a schematic of biological neurons and the synapses in-between, where it is known that signal receipt and transmission are achieved by the generation of action potentials in soma and its propagation along the axons of the neuron, respectively (neuron spiking). Meanwhile, signal transfer and storage are determined by the connection strength of the synapses between neurons (synaptic plasticity). In particular, synaptic plasticity, or the change in synapse connectivity, is widely believed to underlie our learning processes and memory. Though there have been some reports [5–7] of mimicking synaptic plasticity using SiNs, they are somewhat inappropriate for practical use in large scale neuromorphic applications, because of the large consumption of area and power of complicated circuits.

Following the famous hypothesis of a Canadian psychologist [8] on synaptic plasticity, it is expected that the connectivity in between synapses will change plastically when two neighboring neurons spike temporally together. A representative algorithm for such a hypothesis is briefly depicted using three neurons in Fig. 1 (a), synaptic strengths may change depending on the relative timing of pre- and post-synaptic spikes. The synaptic strength is potentiated (or strengthened) if pre-spike A precedes post-spike B ($\Delta t > 0$) whereas it is depressed (or weakened) if pre-spike A follows post-spike C ($\Delta t < 0$). Such a timing algorithm in synaptic strength's modification or change is called spike-timing dependent plasticity (STDP) [2]. In other words, the change in synapse strength (ΔC) is positive (the synaptic connectivity is potentiated) when $\Delta t > 0$, and it becomes higher at smaller Δt, which is called long-term potentiation (LTP). Meanwhile, ΔC is negative (the synaptic connectivity is depressed) when $\Delta t < 0$ and it becomes more negative at smaller negative Δt, which is long-term depression (LTD), as seen in Fig. 1(b).

In this study, we introduce a novel scheme for emulating STDP which is easily applicable to any nano-scale memory device when

* Corresponding author. Tel.: +82 32 749 5845; fax: +82 32 818 5801.
E-mail addresses: daehwan.kang@samsung.com (D.-H. Kang), h9.jun@samsung.com (H.-G. Jun), Kc.ryoo@samsung.com (K.-C. Ryoo), hongsik.jeong@yonsei.ac.kr (H. Jeong), hyunchul.sohn@yonsei.ac.kr (H. Sohn).

http://dx.doi.org/10.1016/j.neucom.2014.12.036

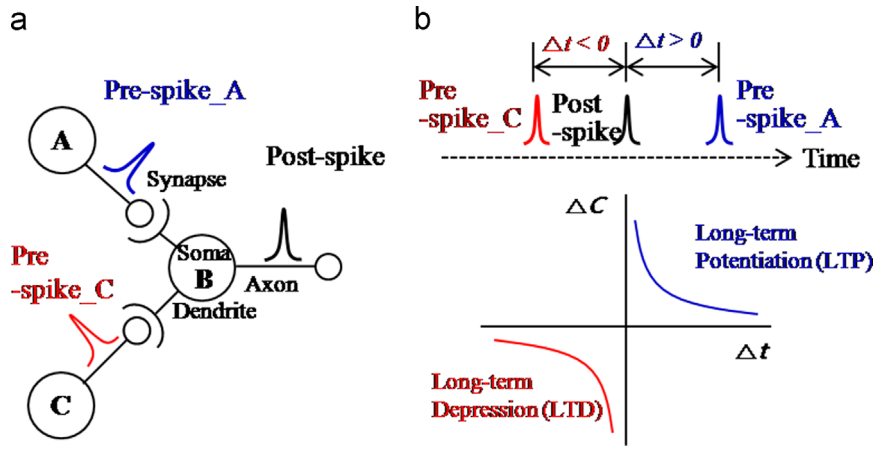


Fig. 1. (a) The schematic of biological neurons and (b) the spike-timing dependent plasticity (STDP) showing long-term potentiation (LTP) and long-term depression (LTD) according to the time-interval between the pre- and post-spikes.

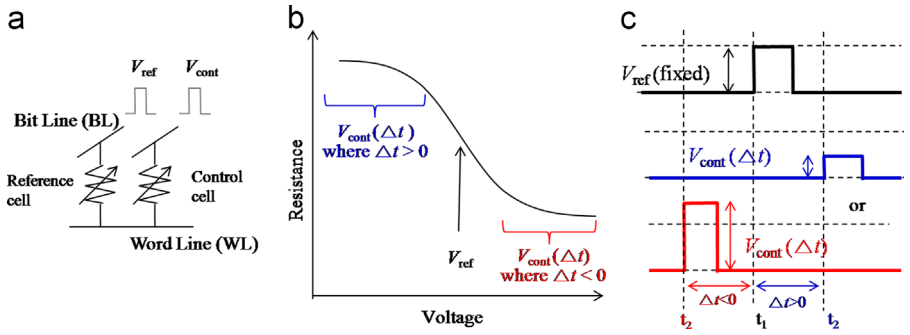


Fig. 2. (a) Schematic of two resistive memory cells, where V_{ref} and V_{cont} are pulse voltages to reference and control cells, respectively. (b) Concept of time-modulated voltage ranges in typical *R-V* analog curve with respect to the time interval between spikes of pre-synaptic and post-synaptic neurons (Δt). (c) The voltage timing diagram, where blue and red texts respectively correspond to LTP and LTD cases.

if having analog resistance behavior with respect to external stimuli. For an experimental verification of this scheme, we emulated STDPs in two-phase change memory (2-PCM) cells made with 39 nm technology by introducing a novel time-modulated voltage (TMV) pulse scheme. Various STDP shapes can be easily obtained by varying the shape of voltage pulses and the time interval between two cells, which helps to design diverse synaptic connection abilities.

2. Concept for STDP emulation in two resistive memory cells

To emulate the STDP of one synapse, we can take into account two resistive memory cells which are connected to pre-synaptic and post-synaptic neurons through their respective bit lines, as shown in Fig. 2(a). One is a reference cell with a fixed resistance and the other is a control cell with variable resistances. After the reset initialization for two cells to be high resistance, independent voltage pulses called set pulses are applied, based on the intrinsic *R–V* curve of Fig. 2(b), to reduce the resistance of the two cells. It should be designed that the set voltage is fixed for the reference cell (V_{ref}) to have always an intermediate resistance whereas the set voltage to control cell (V_{cont}) is modulated to have various resistance levels so that the two cells have different resistance values with respect to the time interval between the spikes of the pre-synaptic and post-synaptic neurons (Δt). As depicted in Fig. 2(c), in the case of $\Delta t > 0$, V_{cont} is set to be inversely proportional to Δt whereas in the case of $\Delta t < 0$, V_{cont} is set to be proportional to Δt. Then, when the reciprocal of the resistance difference of the two cells is considered as the conductance change (ΔC) and it is plotted with Δt, we can obtain an STDP shape.

3. Experiment

For a representative demonstration of the scheme suggested above, we emulated STDP behaviors by making use of two PCM cells, using state-of-the-art 39 nm technology. As shown in Fig. 3(a), a PCM cell has a p–n diode switch epitaxially grown on an N+ Si word line (WL), ring-type bottom electrode (BE), a damascene-type $Ge_2Sb_2Te_5$ (GST) phase change material, line-type top electrode (TE) and bit line (BL). Fig. 3(b) represents the circuit diagram of 2-PCM cells with two-channel pulse generator which can generate two independent pulses with a time interval as precise as 10 ns. In addition, Fig. 3(c) and (d) depict the block diagram of a programming algorithm, and the detailed pulse conditions and their expected resistance change with respected to the sign of Δt.

First, both reference and control cells have high resistance values of several MΩ (R_{init}), using an initial short pulse of 5 V height with a 10 ns-rise, 80 ns-duration, and 10 ns-fall. Then, we make a reference cell to induce a few hundred kΩ (R_{ref}) by applying the fixed voltage of 5 V with a 100 ns-rise, 50 ns-duration, and 100 ns-fall widths at time t_0. Next, we apply a time-modulated voltage (TMV) at time $t_0+\Delta t$ for a control cell to have various resistance values (R_{cont}) according to the sign and magnitude of Δt. Here, we use a 5 V - (5 V/Δt_{max}) × Δt pulse height as a TMV example under the same pulse widths and repeat to write a control cell with an increase of Δt from 1 ms to 20 ms, as described in Fig. 3(c).

4. Emulation of STDP in two-phase change memory cells

Fig. 4(a) shows resistance changes in reference and control cells (R_{ref} and R_{cont}) with respect to Δt, which has resulted from the

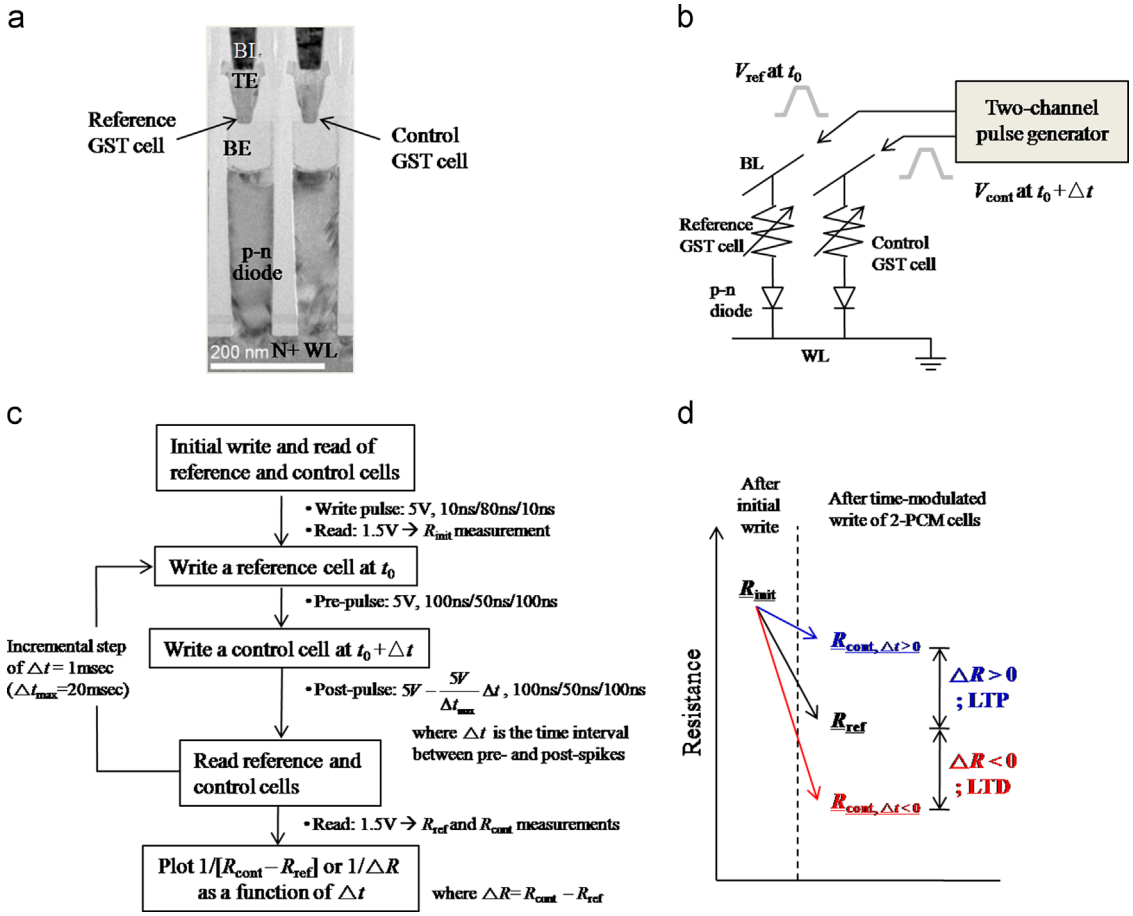


Fig. 3. (a) A cross sectional transmission electron microscope image of phase change memory cells made with 39 nm technology. (b) Circuit diagram of 2-PCM cells with two-channel pulse generators. If V_{ref} is applied to the reference cell at a specific time (t_0) then V_{cont} is applied to the control cell at $t_0+\Delta t$. (c) Block diagram of the programming algorithm. (d) Detailed pulse conditions for STDP emulation in 2-PCM cells and their expected resistance changes with respected to the sign of Δt.

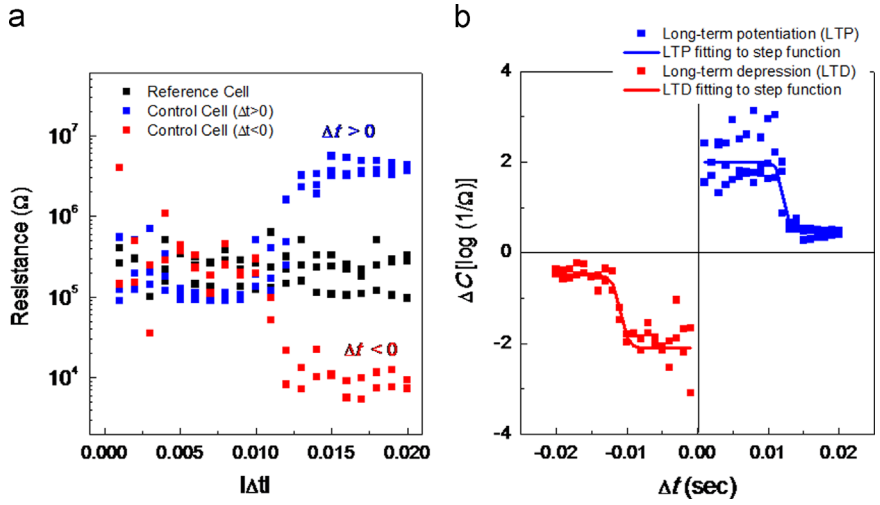


Fig. 4. (a) Resistance changes of the reference and control cells with respect to Δt. (b) Step-like LTP and LTD behaviors are realized in 2-PCM cells by the programming algorithm of Fig. 3(c), where they are fitted by step-like functions.

programming algorithms presented in Fig. 3(c). R_{ref} has a resistance of 100 kΩ–500 kΩ irrespective of Δt, which is due to the fixed pulse condition. Some fluctuations in R_{ref} are attributed to the stochastic crystalline states, which are often observed when set write operations are repeated in the phase change memory while targeting an intermediate resistance level [9]. On the other hand, R_{cont} is similar to R_{ref} for small $|\Delta t|$, but is abruptly increased to 2 MΩ – 6 MΩ (in the case of $\Delta t > 0$) or decreased to 5 kΩ – 20 kΩ (in the case of $\Delta t < 0$) at large $|\Delta t|$, according to the time-modulated pulse schemes, as expected in Fig. 3(d). Since the difference ($\Delta R = R_{cont}$ - R_{ref}) of the two cells can be extracted and its reciprocal can be regarded as ΔC in 2-PCM synapses, a high $|\Delta C|$ can be achieved at small $|\Delta t|$, whereas a

low $|\Delta C|$ is achieved at high $|\Delta t|$. Accordingly, STDP behaviors can be observed when ΔC is plotted as a function of Δt, as shown in Fig. 4(b).

We can fit such STDP behaviors into 2-PCM cells by a step-function of Eq. (1), where a and c are scaling parameters, τ is the characteristic time when ΔC changes abruptly and b is a fitting parameter. That is, ΔC is $a+c$ when Δt approaches to zero whereas it becomes c when Δt is much larger than τ, as touched upon in Eq. (1). In Fig. 4(b), a and c are 1.5 and 0.5, τ is 12 ms, and b is 4.0×10^{-4} for LTP fitting while a and c are -1.6 and -0.5, τ is -11 ms, and b is -5.5×10^{-4} for LTD fitting. It is thought that the step-like STDP in our study has to do with the percolation behaviors in the crystallization process of amorphous phase change material and it needs further study. On the other hand, these step-like shapes are somewhat deviated from biological standard shapes [as in Fig. 1(b)] but they belong to the F2 category when an action potential of pre-synaptic neurons has an asymmetric rectangular shape [5].

$$\Delta C=\frac{a}{e^{\Delta t-\tau/b}+1}+c=\begin{cases}a+c & if\ \Delta t<<\tau\\ \frac{a}{2}+c & if\ \Delta t=\tau\\ c & if\ \Delta t>>\tau\end{cases} \quad (1)$$

We examine how the pulse shape affects the LTP behaviors in 2-PCM cells. The set pulses that induce the crystallization of initially reset (amorphous) reference and control cells, have slow-quenched set pulse forms with tunable rising/duration/falling widths. First, when the duration width is varied from 75 ns to 25 ns [Fig. 5(a)], both τ and $a+c$ reduce as the duration decreases [Fig. 5(b)]. Similar tendencies are also found when the falling width changes from 1600 ns to 50 ns [Fig. 5(c) and (d)]. It is well known that the slow-quenched set pulses are not enough to crystallize, especially when the duration width is smaller than is required for the pre-reset amorphous region not to melt fully or when the falling time is too short to crystallize the melted amorphous phase. Thus, at shorter duration or falling width, the control cell tends to be less conductive, and both τ and $a+c$ decreases. Accordingly, the modification in a slow-quenched set pulse shape is effective at obtaining various τ and $a+c$ values in our 2-PCM cells.

Meanwhile, it is believed that the signal transfer time per each spiking-and-synaptic transfer event (t_{sum}) can be a basis to determine the overall signal processing speed in biological neuron networks. It is composed of three sequential processes: (1) The integration-and-fire time of synaptic potentials in a cell body or soma (t_{soma}), (2) the electro-chemical transfer time at synapse ($t_{synapse}$), and (3) the propagation time of the generated action potential along axon (t_{axon}), as shown in Fig. 6(a). Both t_{soma} and $t_{synapse}$ have time scales of a few tens of milliseconds [10,11], whereas t_{axon} is as short as nanoseconds, or microseconds at most because the propagation speed of the action potential is as fast as $\sim$150 m/s along an axon with its length from micrometer to millimeter [12]. Thus, t_{sum} is mostly determined by t_{soma} and $t_{synapse}$. Here, we only consider $t_{synaspe}$, which can also be represented by τ, since it indicates how fast synaptic transfer (synaptic connectivity) is achieved.

We can achieve good LTP curves to get τ values as small as tens of a few microseconds and hundreds of nanoseconds when the incremental step in Δt is decreased to the microsecond and nanosecond ranges, as plotted in Fig. 6(b). Thus the 2-PCM cells in this study can have a very wide range of τ values by precisely controlling the time interval between the applied set pulses. This means that the 2-PCM cells have faster synaptic transfer times ($t_{synapse}$) by several orders of magnitude compared to biological neurons or SiNs. Accordingly, the 2-PCM synapse in this study can increase the signal transfer rate to speed up learning or memory abilities by reducing the time interval between pre-synaptic and post-synaptic spiking potentials, which helps design diverse synaptic connection abilities when combined with the aforementioned variability in STDP shapes.

5. Discussion

Recently, single resistive memory devices with transition metal oxides [13], Ge-Te-Sb phase change material [14–16], and organic material [17] as electronic synapses have gathered attention, because they can be operated with low power consumption. They have a simple structure that can be easily integrated to have a high density that is comparable to the number of neurons in our neocortex ($\sim10^{11}$) by using nano fabrication techniques in the semiconductor industry. Among them, the phase change memory based on the phase transition between amorphous and crystalline Ge-Te-Sb material is the most promising because it has very similar functionalities to biological neurons [18] and it is matured at the mass production level in the form of non-volatile memory of phase-change random access memory (PRAM) and optical recording media of CD-RW and DVD-RAM during last decades [19].

Kuzum et al. [14] demonstrated various STDP behaviors in one phase change memory cell by applying positive voltage chain pulses in the forwards direction and a single negative voltage pulse backwards, but the pulses are somewhat complicated in the management of pulse shape and directionality. Suri et al. [15] introduced two-phase change memory cells that can play specific roles in flowing LTP and LTD currents, but they require a large area for cell-selecting transistors and extra current comparator circuits. Eryilmaz et al. [16] presented a 10×10 array of phase change synaptic devices that showed simple pattern learning and recognition abilities, but they had to use one metal-oxide-semiconductor (MOS) switch per synaptic device. Relatively, the 2-PCM synaptic device in this work has the advantages of using a simpler pulse pattern and smaller device size over the above-mentioned reports because it makes use of single set pulses and vertical-type diode switches with no area penalty for the device size.

The signal transmission in a biological neuron is mostly unidirectional from pre-synaptic to post-synaptic neurons, where it shows electric features at the axons in pre-synaptic neurons, it turns into chemical characteristics at the synapse, and it returns the electric mode at the dendrite in the post-synaptic neuron [4]. The changes in synaptic connectivity are correlated with the time difference between the pre-synaptic and post-synaptic spikes of the STDP algorithms [5]. The 2-PCM in this study follows such unidirectional features and shows deterministic synaptic plasticity of biological neurons as demonstrated in Figs. 3 and 4. It should also be mentioned that this 2-PCM synaptic device needs extra circuits: Time interval counters and synapse selector/generators to measure the time differences between the pre- and post-spikes and to modulate conductance, respectively, unlike a biological synapse where the synaptic strength is varied *in-vivo* in the course of electro-chemical processes in synapse cleft. The required energy for one synaptic event is 200 pJ – 300 pJ in this 2-PCM synapse with 39 nm technology, which is higher than that of biological synapses (1 pJ – 10 pJ). However, it can be at least reduced to tens of pJ when adopting a sub–10 nm technology phase change memory device [20] and high-speed phase change materials with eutectic Sb_7Te_3-based [21] or Sb-based [22] compositions.

6. Conclusion

Low power consumption, small form factor, and high reliability are prerequisites to emulate the spike-timing dependent plasticity (STDP) for biological synapses in large-scale neuromorphic systems. For this, we have proposed a novel scheme for emulating STDP in analog resistive memory devices and we

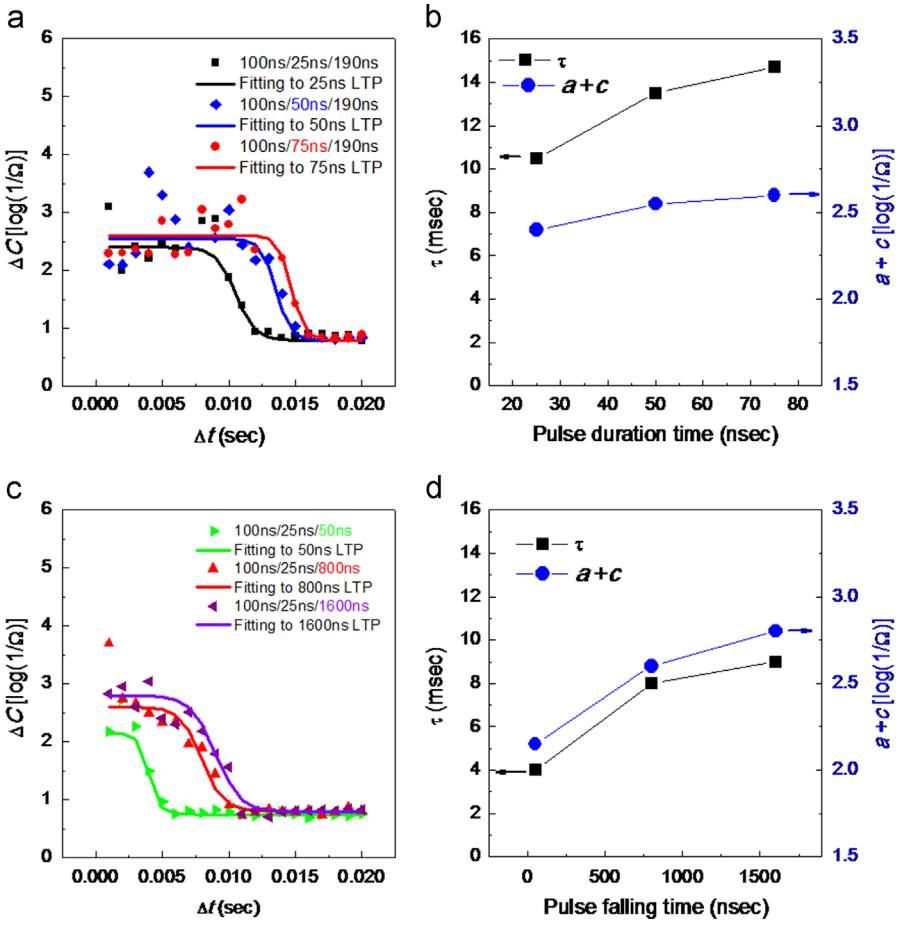


Fig. 5. (a) LTP shapes and (b) changes in characteristic parameters with respect to pulse duration. (c) and (d) are those that correspond to the changes in pulse falling width.

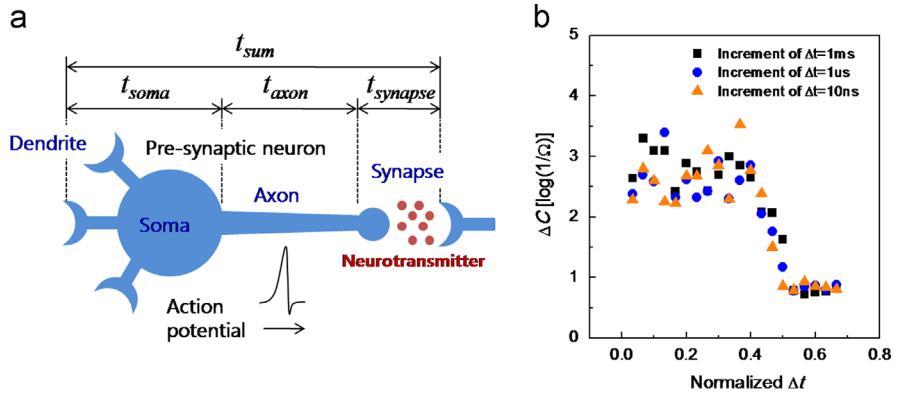


Fig. 6. (a) Three time boundaries at one spike-and-synaptic event in a biological neuron and (b) LTP behaviors when the increment of Δt is changed from milliseconds to microseconds and nanoseconds.

emulated its behavior in 2-PCM synaptic devices made with 39 nm phase change memory cells by applying time-modulated voltage (TMV) pulses. It is observed that control of the duration and falling times in slow-quenched set pulses are effective for obtaining various LTP shapes. In addition, it is demonstrated that the synaptic transfer time can be reduced to as little as hundreds of nanoseconds that is much faster than biological or conventional SiNs synapses. Thus, the 2-PCM synapse in this study is very likely to have advantages for high-speed, high-capacity neuromorphic applications, which enables mass-production-level phase change memory to be a strong candidate for electronic synapses.

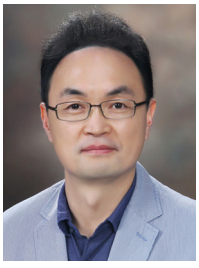
Acknowledgments

This work was supported by the industry–university cooperation project of Samsung Electronics and by the second stage of the Brain Korea 21 project.

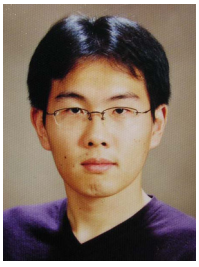
References

[1] Carver Mead, Proc. IEEE 78 (10) (1990) 1629–1636.
[2] G. Indiveri, B. Linares-Barranco, T.J. Hamilton, A. Schaik, R. Etienne-Cummings, T. Delbruck, S.-C. Liu, P. Dudek, P. Häfliger, S. Renaud, J. Schemmel, G. Cauwenberghs, J. Arthur, K. Hynna, F. Folowosele, S. Saighi, T. Serrano-

Gotarredona, J. Wijekoon, Y. Wang, K. Boahen, Frontiers in Neuroscience 5, Article 73 (2011) 1–23.
[3] C.-P. Poon,, K. Zhou, Frontiers in Neuroscience 5, Article 108 (2011) 1–2.
[4] D.S. Modha, Commun. ACM 54 (2011) 62–71.
[5] C. Zamarreño-Ramos, L.A. Camuñas-Mesa, J.A. Pérez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, B. Linares-Barranco, Frontiers in Neuroscience 5, Article 26 (2011) 1–2.
[6] G. Indiveri, E. Chicca, R. Douglas, IEEE Trans. Neural Netw. 17 (2006) 211–221.
[7] J. Seo, B. Brezzo, L. Yong, B.D. Parker, IEEE Custom Integrated Circuits Conference (CISS), (2011) 1–4.
[8] Donald Hebb, The Organization of Behavior: A Neurophysiological Theory, Wiley, New York, 1949.
[9] D.-H. Kang, J.-H. Lee, J.H. Kong, D. Ha, J. Yu, C.Y. Um, J.H. Park, F. Yeung, J.H. Kim, W.I. Park, Y.J. Jeon, M.K. Lee, J.H. Park, Y.J. Song, J.H. Oh, G.T. Jeong, H.S. Jeong, 2008 Symposium on VLSI Technology, 2008, pp. 17–19.
[10] S. Diwakar, J. Magistretti, M. Goldfarb, G. Naldi, E. D'Angel, J. Neurophys. 101 (2008) 519–532.
[11] B. Katz, R. Miledi, Proc. R. Soc. Lond. 161 (1965) 483–495.
[12] B. Belhadj, A. Joubert, O. Temam, R. Héliot, IEEE International Symposium on Circuits and Systems (ISCAS), 2012, pp. 20–23.
[13] S. Yu, B. Gao, Z. Fang, H. Yu, J. Kang, H.-S. Philip Wong, IEEE International Electron Device Meetings, 2012, pp. 10.4.1–10.4.4.
[14] D. Kuzum, R.G.D. Jeyasingh, B. Lee, H.-S. Philip Wong, Nano Lett. 12 (2012) 2179–2186.
[15] M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, B. DeSalvo, IEEE International Electron Device Meetings, 2011, pp. 4.4.1–4.4.4.
[16] S.B. Eryilmaz, D. Kuzum, R.G.D. Jeyasingh, S. Kim, M. BrightSky, C. Lam, H.-S. Philip Wong, IEEE International Electron Device Meetings, 2013, pp. 25.5.1–25.4.1.
[17] S.H. Jo, T. Chang, I. Ebong, B.B. Bhadviya, P. Mazumder, W. Lu, Nano Lett. 10 (2010) 1297–1301.
[18] S.R. Ovshinsky, Jpn. J. Appl. Phys. 43 (2004) 4695–4699.
[19] M. Wuttig, N. Yamada, Nat. Mater. 6 (2007) 824–832.
[20] D.H. Im, J.I. Lee, S.L. Cho, H.G. An, D.H. Kim, I.S. Kim, H. Park, D.H. Ahn, H. Horii, S.O. Park, U-in Chung, J.T. Moon, IEEE International Electron Device Meetings, 2008, pp. 1–4.
[21] S. Lee, J.-h. Jeong, Z. Wu, Y.-W. Park, W.M. Kim, B.-k. Cheong, J. Electrochem. Soc. 156 (2009) H612–H615.
[22] T. Zhang, Z.T. Song, F. Wang, B. Liu, S.L. Feng, B. Chen, Appl. Phys. Lett. 91 (2007) 222102–222104.



Dr. Dae-Hwan Kang is a principal researcher in Samsung Electronics Co. Ltd., who has been working on the development of low-cost, low-power, and high-performance phase change memory for data server or wearable device applications. Recently, he is also researching on electronic neuron and/or synaptic device using nano-scale resistive memories for neuromorphic applications. He was born in 1968 and received a B.E in Materials Science and Engineering from Pohang University of Science and Technology, Korea. And he received an M.E and Ph.D. degree in Materials Science and Engineering from Seoul National University, Seoul, Korea, respectively.



Dr. Hyun-Goo Jun was born in Seoul, Korea, in 1978. He received the Master and Ph.D. degrees in material engineering from Seoul National University, Seoul, Korea, in 2004 and 2011, respectively. During his thesis, he studied on the behavior of phase change material for memory application. Since 2011, he has been a senior engineer in Process Architecture Team, Memory Division of Samsung Electronics Co., Ltd. His research is mainly focused on the implementation and characterization of phase change memory in mass production level, as well as its new application including neuromorphic engineering.

Dr. Kyung-Chang Ryoo was born in Seoul, Korea in1974. He received the B.S. degree and the M.S. degree in School of Material Science and Engineering from Hanyang University, Seoul, Korea in 2000 and 2002 respectively. He has received the Ph.D. degree in Nano-Science in Electrical Engineering from Seoul National University, Seoul, Korea in 2012. Since 2002 he has joined New memory R&D team at Samsung Electronics and has been working as a senior engineer. His current research interests are in circuit design and computer architecture of non-volatile new memories such as PRAM, STT-MRAM and ReRAM. He is currently a member of IEEE society.

Dr. Hongsik Jeong was born in Seoul, Korea, on May 27, 1962. He received the B.S., M.S., and Ph.D. degrees in physics from Yonsei University in 1985, 1987 and 1992, respectively. Since 1992, he joined the Samsung Electronics, he had been engaged in development of process integration for DRAM and new memory devices, such as PRAM, MRAM and FRAM, who received Korean presidential award in 2005. And then he has led new memory project as a Vice President in Samsung Electronics. He has successfully developed and commercialized world first PRAM product for mobile phone. He has published 1 book, 50 technical papers, 37 patents and given over 30 presentations in international conference as a key note and invited speaker.

Dr. Hyunchul Sohn is a professor at Yonsei University since 2006. His main research interests are on materials and process development for non-volatile memories such as Flash and ReRAM, and interconnect such as barrier metal and low k dielectrics. Prior to joining Yonsei University, he was a senior member of technical staff for SK Hynix semiconductor, focusing on developing materials and processes for gate stacks, capacitors, and interconnect for DRAM and Flash memory devices. He received his B.S. and M.S. degrees in Metallurgy from Seoul National University, Seoul, Korean in 1984 and 1986 respectively and Ph.D. in materials science from University of California, Berkeley, USA in 1993.