A polynomial time algorithm for determining zero Euler–Petrie genus of an Eulerian graph

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Abstract

A dual-Eulerian graph is a plane graph which has an ordering defined on its edge set which forms simultaneously an Euler circuit in the graph and an Euler circuit in the dual graph. Dual-Eulerian graphs were defined and studied in the context of silicon optimization of cmos layouts. They are necessarily of low connectivity, hence may have many planar embeddings. We give a polynomial time algorithm to answer the question whether or not a planar multigraph admits an embedding which is dual-Eulerian and construct such an embedding, if it exists.

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1. Introduction

Let $G$ be a connected graph and let $(G, \rho)$ be a map with embedding $\rho: G \to S$ of $G$ into an orientable surface $S$. Let $g(S)$ denote the genus of $S$, and $g(G)$ denote the genus of $G$, that is, the least genus of any orientable surface $S$ such that $(G, \rho)$ is a map. A Petrie circuit (walk) is a circuit (walk) in a map which turns alternatingly left and right, see Fig. 1. We will often indicate a Petrie walk by showing the turns at each vertex by small circular arcs. Obviously the reverse of a Petrie circuit (walk) is also a Petrie walk.

Petrie circuits and walks have many interesting properties and have been studied by Shank [9]. They are special cases of A-trails, see [3]. One useful property of Petrie circuits (walks) is that the same sequence of edges is also a circuit (walk) in the dual map $(G, \rho)^*$. A graph containing an Euler circuit which is also an Euler circuit of the dual is called dual-Eulerian. Note that in order for a graph to be dual-Eulerian, all face boundaries must have even length, which means that the graph is bipartite. However, to detect a dual-Eulerian graph, it is not enough to check whether the graph and its

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dual are Eulerian. For instance, the graph in Fig. 2a is not dual-Eulerian, while that in Figure Fig. 2b is.

A common optimization problem in VLSI design of cmos circuits has as a solution a dual-Eulerian path or circuit, which, for 2-connected plane graphs, is equivalent to an Euler–Petrie path or circuit. One can decide in linear time whether a plane graph has an Euler–Petrie circuit by simply starting from any edge and proceeding left–right–left–... and, if that is not successful, right–left–right–..., seeing if either of these two Petrie walks generate an Euler–Petrie walk or circuit. It is much more difficult for a non-embedded graph $G$ to decide if it has an embedding with an Euler–Petrie path or circuit. A more interesting and useful question is whether a planar graph has an embedding which has an Euler–Petrie path. In [1], it is pointed out that more efficient layouts for cmos functional cells can be determined by deciding whether or not a planar multigraph admits a dual-Eulerian embedding.

Given an Eulerian graph $G$ and an Euler circuit (path) $P$, it is always possible [8] to find a map $(G, \rho)$ on some surface of high enough genus, such that $P$ is an Euler–Petrie circuit (path.) It is natural to define the Euler–Petrie genus of a graph $G$, $\text{epg}(G)$ to be the least genus of any surface in which $G$ has an embedding with an Euler–Petrie circuit or path.

**Example 1.** $K_5$ is Eulerian with genus 1 and Euler–Petrie genus 1, with Euler–Petrie circuit $\{0, 1, 4, 0, 3, 4, 2, 3, 1, 2, 0\}$. See Fig. 3.
Example 2. $K_7$ has genus 1 but Euler–Petrie genus at least 3, since the torus embedding is unique and any embedding of $K_7$ into a surface of genus 2 has at least 6 triangular faces.

Computing the Euler–Petrie genus of a graph seems extremely difficult, [11,1,7,12,14]. Even the Euler–Petrie genus of complete graphs is not known. In this paper we give a polynomial time algorithm to solve the question of whether an Eulerian graph has Euler–Petrie genus 0. This will solve the recognition problem for 2-connected dual-Eulerian graphs, and in particular the case of series parallel networks. In what follows we will only consider Euler–Petrie circuits, the case of paths being similar.

2. The 3-block tree

Since the edges of a Petrie path form also a Petrie path in the dual graph, the dual of a planar graph $G$ with an Euler–Petrie circuit is also Eulerian, which means that $G$ is bipartite. As a consequence, the graph, or its dual, cannot be 3-connected (in the sense of Tutte), since all triangle free simple planar graphs must have at least four vertices of valence at most three. This means that every Eulerian graph $G$ with Euler–Petrie genus 0 must have a non-trivial 3-block tree, or is just a circuit or multilink.

The 3-block tree [10,2] encodes the structure of a 2-connected graph in terms of the operation of edge amalgamation, in which two disjoint graphs are joined along an (oriented) edge and then that edge is erased. See Fig. 4. The atoms of the construction, called 3-blocks, are simple 3-connected graphs, cycles and multilinks (a multilink is the planar dual of a cycle), each with at least three edges. Tutte [10] showed that every 2-connected graph is uniquely encoded as a tree of edge amalgams of 3-blocks. The nodes of the tree correspond to a disjoint collection of 3-blocks, namely 3-connected simple graphs, cycles, or multilinks. Each edge corresponds to a pair of (oriented) edges from the 3-blocks to which it is incident. To obtain a canonical decomposition one must require that no edge in any 3-block is amalgamated more than once, no pair of cycles is amalgamated together, and no pair of multilinks is amalgamated together. An example of a graph and its associated 3-block tree is given in Fig. 5. Hopcroft and Tarjan [4] showed that Tutte’s 3-block tree can be constructed in linear time.
Note that a 2-connected graph is planar if and only if each of its 3-blocks is planar. Moreover, a 3-connected 3-block, or a cycle, is uniquely embeddable in the plane (in two ways counting orientation) and each multilink with \( m \) edges has \((m - 1)!\) distinguishable embeddings, so a 3-block tree all of whose 3-connected 3-blocks are planar is planar with \( 2^z \prod (m_i - 1)! \) different embeddings, where \( z \) is the number of 3-connected 3-blocks plus the number of cycles, and \( m_1, m_2, \ldots \) are the sizes of the multilinks. Thus a brute force attack on the question of whether \( \text{epg}(G) = 0 \) would require us to check each of these embeddings for an Euler–Petrie circuit even if we know in advance that \( G \) is planar and Eulerian. Such an algorithm would be exponential in the number of leaves in the 3-block tree, hence in the number of vertices of \( G \).

3. The topology of Euler–Petrie circuits

It is straightforward to decide whether a graph has a dual-Eulerian embedding if one knows whether or not each of its blocks has such an embedding. Thus, in what follows, we assume that the graph is 2-connected. In this section, we analyze the possible topologies of Euler–Petrie paths as they pass across and back over some pair of separating vertices.

A separating pair of vertices in a plane graph corresponds to two faces (not uniquely determined) which form a 2-cutset in \((G, \rho)^*\). The only way an Euler–Petrie path can
pass from left to right between the two lobes of the plane graph is to make one of the
four turns indicated in Fig. 6. The circuit must use either two or four of the possible
entry and exit turns. If only two are used, then we will replace the right lobe with a
single edge labeled to indicate the topology of traversal as either \( p \) (Petrie-like), \( f \)
(face-like) or \( s \) (spur-like). Specifically, if the entry and exit turns are \( a \) and \( c \), then
by a Whitney flip [13], this is equivalent to \( b \) and \( d \) and the lobe is Petrie-like, see
Fig. 7. Note that the right lobe in this case may be replaced by a single edge to get
a smaller graph with an Euler–Petrie circuit which agrees with the given circuit on
the left lobe. Similarly, if the entry and exit turns are \( a \) and \( d \) (\( b \) and \( c \)) then the
lobe is face-like, see Fig. 8. In this case, the right lobe could be replaced by a path
of length two while preserving the dual-Eulerian property, but we choose to replace it
with a single edge marked \( f \), where the marking contains the instruction to turn the
same way at the endpoints of the edge. If the exit and entry turns are \( a \) and \( b \), so a
Whitney flip only replaces the tour with its reverse, then we say it is spur-like and
we indicate the topology by an oriented edge labeled \( s \), see Fig. 9. The dual-Eulerian
The marking $s$ allows us to use only one edge as a replacement as it contains the instruction to traverse the edge in the given direction, turn around and traverse the edge in the opposite direction. This will modify a given Euler–Petrie circuit by replacing the edges of the right lobe by the spur without any other alterations. It may happen that there are two Petrie tours possible, starting and ending with the complementary pair of turns, in which case, both are Petrie-like, both are face-like, or both are spur-like. If both are spur-like we do not orient the edge labeled $s$.

The other possibility is that the Euler circuit enters the right lobe twice, and the segments of the circuit partition the edges of the lobe into two sets. In the case that turns $(a, d)$, and $(b, c)$ are used in the given Euler–Petrie circuit, the topology of the circuit is like that of Fig. 10 and we label it $2f$. Here, the right lobe could be replaced by a 4-cycle while preserving the dual-Eulerian property. We again replace the lobe by a single marked edge where the marking carries the turning instructions from Fig. 10. If the two segments use turns $(a, b)$ and $(c, d)$, then the topology is that of two spurs, see Fig. 11, and we label it with $2s$. The labeling $2s$ carries the turning instructions from Fig. 11. The case $2p$, with segments bounded by $(a, c)$ and $(b, d)$ cannot occur in the case of Euler–Petrie circuits, since two Petrie paths cannot cross one another transversely without sharing at least one edge in common.

Given a plane graph with an Euler–Petrie circuit, we can, by the above analysis replace parts of the given circuit by marked edges without loosing any information.
about the topological behavior of the circuit, but the induced circuit is not a left-right circuit any more, prompting the following definition.

**Definition 1.** Let \((G, \rho)\) be a map whose edges are labeled from the set \(\{p, f, s, 2f, 2s\}\) with the \(s\) edges perhaps oriented. A \(pfs\)-Euler circuit is a closed covering walk which traverses all the edges of \(G\) labeled \(p\) and \(f\) once, those labeled \(s\), and \(2f\) twice, and those labeled \(2s\) four times, each according to the turning instructions indicated by its label.

An Euler–Petrie circuit in a plane graph is a special case of a \(pfs\)-Euler circuit in which each edge is labeled \(p\). If we can determine whether a \(psf\) labeled graph has a plane embedding realizing the labels as a \(pfs\)-Euler circuit, then the problem of determining Euler–Petrie genus zero is also solved.

It may happen that several neighboring lobes share the same pair of separating vertices. In this case, each may be replaced with a single labeled edge, as above, resulting in a set of parallel edges separated by 2-gons, which we call an induced multilink. Only certain combinations of labels are possible for such a multilink. The easiest way to identify these possibilities is to consider the dual structure, which is a single lobe made up of an induced path. For instance, if the overall topology of the induced path is \(p\), then only \(p\)'s and \(f\)'s can be labels, and the number of \(p\)'s must be odd. Hence, if an induced multilink has topology \(p\), then all the labels must be either \(p\) or \(s\), with an odd number of \(p\)'s. The possibilities for each topology are listed in Table 1.

**Theorem 1.** Let \(G\) be a graph whose edge labels are taken from the set \(\{p, f, s, 2f, 2s\}\). Then we can decide if \(G\) has a planar embedding with a \(pfs\)-Euler tour in polynomial time.

**Proof.** We may assume that \(G\) is planar, and, using the Hopcroft Tarjan algorithm, that we have constructed the 3-block tree. Consider a pendant 3-block \(P\).

*Case 1:* \(P\) is 3-connected as in Fig. 12. If \(G\) has a \(pfs\)-Euler circuit in some planar embedding, then its restriction to the edges of \(P\) must be compatible with the unique
Table 1
Possible label configurations

<table>
<thead>
<tr>
<th>Lobe topology</th>
<th>Labels on an induced path</th>
<th>Labels on an induced multilink</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>f, p (odd)</td>
<td>s, p (odd)</td>
</tr>
<tr>
<td>f</td>
<td>f, p (even)</td>
<td>2s, f (one at end)</td>
</tr>
<tr>
<td>s</td>
<td>2f, s (one at end)</td>
<td>s, p (even)</td>
</tr>
<tr>
<td>2f</td>
<td>2f</td>
<td>2s, 2f (one)</td>
</tr>
<tr>
<td>2s</td>
<td>2f, 2s (one)</td>
<td>2s, f (two)</td>
</tr>
<tr>
<td></td>
<td>2f, s (two opposing)</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 12. Replacing a pendant 3-block.

Fig. 13. A pendant circuit.

embedding of $P$. If compatibility is not met, then the answer is no, and we may stop. If the answer is yes, then, since $P$ is a lobe, the topology of $P$ corresponds to just one of the labels in the set $\{p, f, s, 2f, 2s\}$. We label the edge $(x, y)$ in $G'$ with that label and proceed to check $G''$.

Case 2: The pendant node corresponds to a cycle, as in Fig. 13. Here we may proceed as in the previous case.

Case 3: The pendant node corresponds to a multilink, see Fig. 14. In this case, if the multilink has $m$ edges, there are $(m - 1)!$ embeddings and we have to be careful that no re-embedding of $P$ can give a $pf$s-path with a different topology, since otherwise,
as the algorithm proceeds we will have to check and recheck these possibilities and our algorithm will become exponential.

Since the allowable label sets inducing the various topologies are distinct, we immediately see not only which topologies are possible, but the only possible embeddings which will realize the topology under consideration, see Table 1.

The algorithm now proceeds by pruning the 3-block tree one pendant node at a time.

Now, to decide whether a planar Eulerian graph has an Euler–Petrie circuit, we label all the edges with $p$ and start the algorithm described above.

**Theorem 2.** There is a linear time algorithm to decide whether a graph has Euler–Petrie genus zero.

To illustrate the algorithm let us look at the two graphs in Fig. 2. In both cases, the 3-block tree has four pendant nodes corresponding to the doubled edges, and a central node corresponding to the cube. In both cases, the algorithm produces a cube with four edges labeled $s$, all others marked $p$, and we can determine whether or not there is a $pfs$-Euler circuit by simply following the markings. In case Fig. 2a, the edges labeled $s$ form a cutset, and so there is no $pfs$-Euler circuit. In case Fig. 2b, removal of the $s$ edges leaves a simple cycle all labeled $p$ and so the original graph is dual-Eulerian.

4. Uncited references

[5,6]

References