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4-bit Bipolar Triangle Voltage Waveform Generator Using Single-Flux-Quantum Circuit

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Abstract

SFQ digital-to-analog converters (DACs) are one of the candidates for AC voltage standards. We have proposed SFQ-DACs based on frequency modulation (FM). Bipolar output is required for applications of AC voltage standards, while our previous SFQ-DACs generated only positive voltages. In this paper, we present our design of a 4-bit bipolar triangle voltage waveform generator comprising an SFQ-DAC. The waveform generator has two output ports. Synthesized half-period waveforms are alternately generated in one of the output ports. The bipolar output is realized by observing the differential voltage between the ports. We confirmed a 72-μV_{PP} bipolar triangle voltage waveform at the frequency of 35.7 Hz.

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*Keywords:*Digital-to-analog converter; bipolar output; SFQ circuit; Josephson effect; waveform synthesis

1. Introduction

Josephson junctions generate highly accurate voltage through the Josephson effect. Researches of AC voltage standards using Josephson junctions have been conducted [1], [2]. Since single-flux-quantum (SFQ) circuits which consist of superconducting loops and Josephson junctions can generate highly accurate voltage, SFQ digital-to-analog converters (DACs) are one of the candidates for AC voltage standards [3], [4]. We have developed SFQ DACs based on frequency modulation (FM) of SFQ pulse trains [5-7]. It mainly consists of a variable-pulse number multiplier (V-PNM) and a voltage multiplier (VM). The V-PNM multiplies the repetition frequency (f_{IN}) of the reference SFQ train to $\ell(t)\, f_{IN}$, where $\ell(t)$ is a multiplication factor which is modulated by a digital code. The VM multiplies the voltage by a fixed multiplication factor N. The output voltage V_{OUT} of an SFQ-DAC based on FM is given as follows,

$$V_{OUT} = \Phi_0 f_{IN}\, \ell(t) N \qquad (1)$$

where Φ_0 is a flux quantum.

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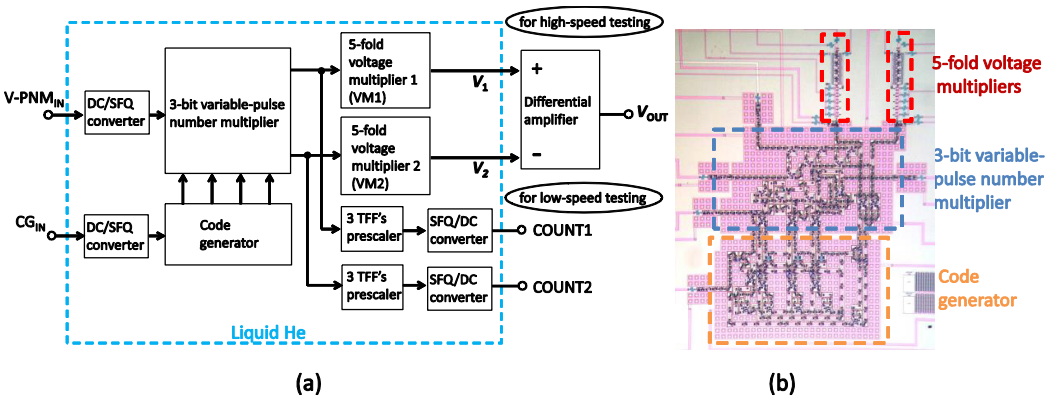

Fig. 1. (a) Test setup and (b) microphotograph of a 4-bit bipolar triangle voltage waveform generator.

Our previous SFQ-DACs generated only positive voltages [5-7], whereas bipolar output is required for applications of AC voltage standards. In this paper, we present our design of a 4-bit bipolar triangle voltage waveform generator comprising an SFQ-DAC.

2. Circuit design

Figure 1 shows a test setup and a microphotograph of a 4-bit bipolar triangle voltage waveform generator. The 4-bit bipolar triangle voltage waveform generator consists of a 3-bit V-PNM, two 5-fold VMs, and a code generator (CG). The differential voltage V_1–V_2, where V_1 and V_2 are respectively the output voltages of VM1 and VM2, becomes bipolar output voltage. The V-PNM generates SFQ pulse trains in which the number of SFQ pulses is multiplied according to a digital code. The CG generates the digital codes which modulate the number of the SFQ pulse in the train and select a working VM. We employed a double-flux-quantum amplifier (DFQA) [8], [9] as the VM. Unipolar half-period triangle voltage waveforms are alternately generated in one of the VMs. The differential voltage of two VMs then becomes a bipolar triangle voltage waveform. This bipolar output method has been proposed for quantum voltage noise source based on SFQ circuits by AIST [10]. We used a 100-fold differential amplifier for observing the differential voltage.

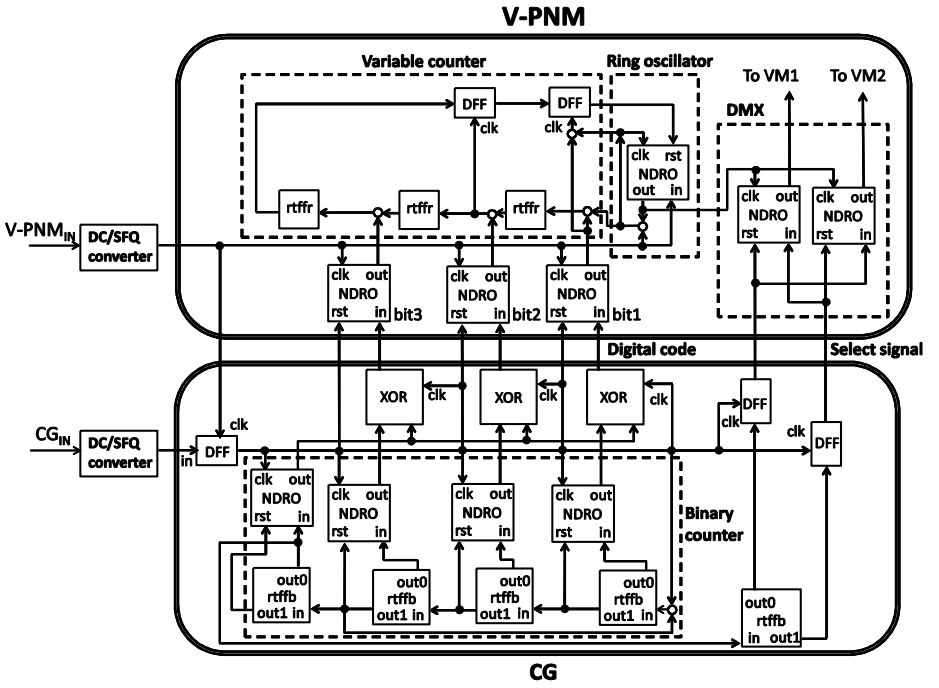

Fig. 2. Block diagram of the V-PNM and the CG. "NDRO", "rtffr", and "rtffb" indicate a non-destructive read out memory, a toggle flip-flop, and a toggle flip-flop with complementary output, respectively.

Table 1. Multiplication factor of the V-PNM (one period).

Clock number	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Multiplication factor $\ell(t)$	0	1	2	3	4	5	6	7	6	5	4	3	2	1
Clock number	15	16	17	18	19	20	21	22	23	24	25	26	27	28
Multiplication factor $\ell(t)$	0	1	2	3	4	5	6	7	6	5	4	3	2	1

The SFQ pulse trains are also transferred to prescalers which consist of 3 TFFs for low-speed testing. We can confirm correct operation of the V-PNM and the CG by observing the output voltage of COUNT1 and COUNT2 through SFQ/DC converters which are connected to the prescalers.

Figure 2 shows block diagram of the V-PNM and the CG. The V-PNM comprises a ring oscillator, a variable counter and a demultiplexer (DMX). We added the DMX to the conventional V-PNM [5], [6]. An SFQ pulse train is generated in the ring oscillator for an SFQ pulse from V-PNM$_{IN}$. The oscillation frequency is design to be 10.1 GHz. The variable counter ends the oscillation of the ring oscillator according to the digital code from the CG. The number of SFQ pulses is modulated by changing the digital code. The SFQ pulse trains are transferred to the DMX. The DMX has two output ports. The output destination of the SFQ pulse train is changed by the select signal from the CG. A core circuit in the CG is a binary counter. The binary counter updates the digital code according to the input signal from CG$_{IN}$. Table 1 shows the multiplication factor $\ell(t)$ of the V-PNM. When $\ell(t)$ changes 0 to 1, the CG switch the output destinations of the DMX.

We used the CONNECT SFQ cell library [11] for the V-PNM and the CG. Test circuits were fabricated using the AIST STP2.

3. Results and Discussion

Figure 3 shows the result of low-speed testing. The frequencies of V-PNM$_{IN}$ and CG$_{IN}$ in the low-speed testing were 8 kHz and 1 kHz, respectively. In Fig. 3, the waveform transitions of the COUNT1 and the COUNT2 alternately occurred. Figure 4 shows sequence of the multiplication factors of the V-PNM obtained from the waveforms in Fig. 3. The multiplication factors of the V-PNM were calculated by counting waveform transitions of the COUNT1 and the COUNT2 for one CG$_{IN}$ period. In Fig. 4, the multiplication factor of the V-PNM is modulated as defined in Table 1. Switching of the output ports is also correctly conducted. We confirmed that the V-PNM and the CG correctly operated in low-speed testing.

Figure 5 shows an output waveform of V_{OUT} in high-speed testing. The frequencies of V-PNM$_{IN}$ and CG$_{IN}$ were 500

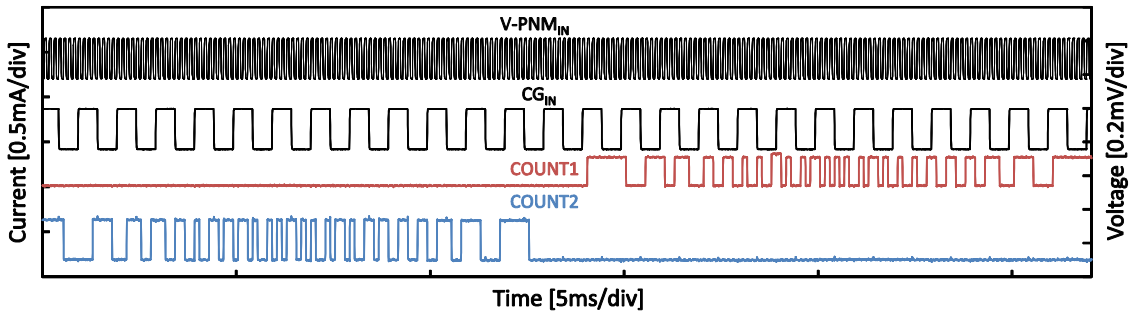

Fig. 3. Input and output waveforms in low-speed testing. The left vertical axis represents currents for V-PNM$_{IN}$ and CG$_{IN}$. The right vertical axis represents voltages for COUNT1 and COUNT2.

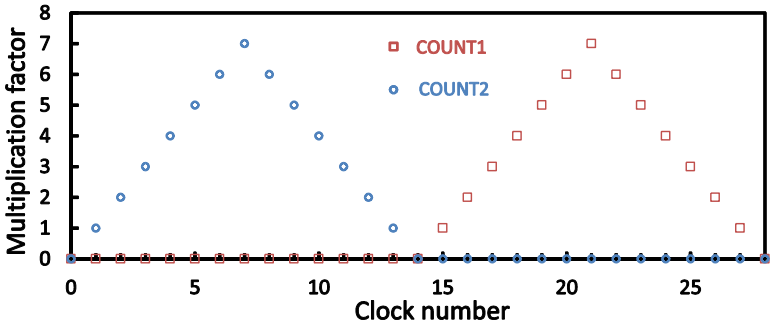

Fig. 4. Sequence of the multiplication factor of the V-PNM.

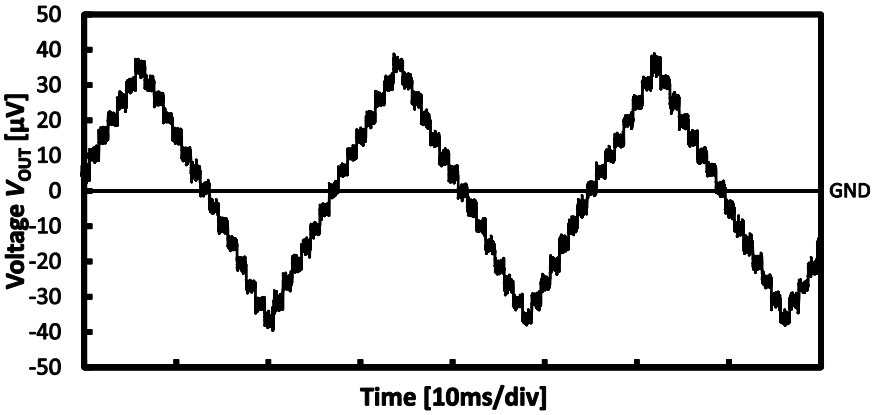

Fig. 5. Output waveform of V_{OUT} in high-speed testing.

MHz and 1 kHz, respectively. While the designed maximum frequency of V-PNM_{IN} was 1.26 GHz, the frequency of V-PNM_{IN} was limited to around 500 MHz by the experimental setup. In Fig. 5, we observe the 72-μV_{PP} bipolar triangle voltage waveform at the frequency of 35.7 Hz. The designed maximum frequencies of CG_{IN} and the synthesized waveform are 1.26 GHz and 45 MHz, respectively. The bandwidth of the differential amplifier limited the synthesized frequency below 100 kHz, although we checked the operation between 10-100 Hz. Figure 5 shows that the bipolar output was realized through differential voltage between two output ports. This bipolar output method can be applied to a sinusoidal voltage waveform generator.

The synthesized output waveform in Fig. 5 contains visible noise. Therefore, we have not conducted accuracy evaluation for the synthesized waveform. Low noise environment should be introduced in our setup. If we employ VMs with large multiplication factor, the noise would also be relatively reduced. We have confirmed operation of the 1000-fold VM up to 13.2 GHz [9].

4. Conclusion

We designed the 4-bit bipolar triangle voltage waveform generator based on the SFQ-DAC. This waveform generator had two output ports. Synthesized half-period waveforms were alternately generated in one of the output ports. The bipolar output was realized by observing the differential voltage between the ports. We confirmed a 72-μV_{PP} bipolar triangle voltage waveform at the frequency of 35.7 Hz. This bipolar output method is applicable to a sinusoidal voltage waveform generator.

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