Abstract

The ATLAS Liquid Argon (LAr) calorimeters are high precision, high sensitivity and high granularity detectors designed to provide precision measurements of electrons, photons, jets and missing transverse energy. ATLAS and its LAr calorimeters have been operating and collecting proton-proton collisions at LHC since 2009. The current front-end electronics of the LAr calorimeters need to be upgraded to sustain the higher radiation levels and data rates expected at the upgraded high luminosity LHC machine (HL-LHC), which will have 5 times more luminosity than the LHC in its ultimate configuration. The complexity of the present electronics and the obsolescence of some of components of which it is made, will not allow a partial replacement of the system. A completely new readout architecture scheme is under study and many components are being developed in various R&D programs of the LAr Calorimeter Group.

The new front-end readout electronics will send data continuously at each bunch crossing through high speed radiation resistant optical links. The data will be processed real-time with the possibility of implementing trigger algorithms for clusters and electron/photon identification at a higher granularity than that which is currently implemented. The new architecture will eliminate the intrinsic limitation presently existing on Level-1 trigger acceptance. This article is an overview of the R&D activities which covers architectural design aspects of the new electronics as well as some detailed progress on the development of several ASICs needed, and preliminary studies with FPGAs to cover the backend functions including part of the Level-1 trigger requirements. A recently proposed staged upgrade with hybrid Tower Builder Board (TBB) is also described.

1. Introduction

The ATLAS experiment [1] is one of the two general-purpose detectors designed to study proton-proton collisions produced at the Large Hadron Collider (LHC) with 14 TeV in the center-of-mass and to explore the full physics potential of the LHC machine at CERN.

Liquid Argon (LAr) calorimeters [2] in ATLAS are high precision, high sensitivity and high granularity detectors designed to provide precision measurements of electrons, photons, jets and missing transverse...
energy. The LAr calorimeters consist of four sub-detectors and are contained within three cryostats between the inner tracking detectors and the outer muon chambers as shown in Figure 1. The central cryostat houses the electromagnetic barrel calorimeter (EMB) which covers the pseudo-rapidity range \(0 < |\eta| < 1.475\), while each end-cap cryostat contains an end-cap electromagnetic calorimeter (EMEC) which covers \(1.375 < |\eta| < 3.2\), two hadronic end-cap wheels (HEC) covering \(1.5 < |\eta| < 3.2\) and a three wheels forward calorimeter (FCAL) which covers the region very close to the beam axis \((3.1 < |\eta| < 4.9)\) to achieve large acceptance.

2. Readout Electronics of Current LAr Calorimeters

The readout electronics architecture of current LAr calorimeters is depicted in Figure 2. When a charged particle traverses and ionizes the liquid Argon in the gap between a LAr electrode and an absorber, an ionization current signal is preamplified, shaped, buffered and digitized by the front-end boards (FEB) [3] installed on the detector. The FEBs send the digitized pulse via optical links to the Readout Drivers (ROD) which are installed in a radiation free area (USA15) next to the detector cavern (UX15). In total 182,468 calorimeter cells are to be read out. Each ROD receives the data from up to 8 FEBs and calculates the energy deposited, the time of the deposition and a quality factor for cells with high energy deposit, using an optimal filtering algorithm [4]. RODs send data to the Readout Buffers (ROBs) hosted on PCs (ROS) through S-links. Analog trigger sum signals are formed on front-end electronics boards and sent to the receiver system through copper cables before interface to the Level-1 calorimeter trigger (L1Calo) system.

The LAr calorimeters readout electronics include two sub-systems, front-end electronics [5] and back-end electronics [6] systems. The front-end electronics system is installed on detector and includes 58 Front End Crates (FEC) which house 1,524 FEBs and other electronics boards. The back-end electronics system consists of 16 back end crates and 68 ROS PCs, and there are total 192 RODs plugged in back end crates and \~800 fiber optical links between RODs and ROS.

3. Readout Electronics Upgrade Motivation for HL-LHC

LHC is expected to be upgraded in two phases. Phase-I is planned in 2018 and Phase-II is planned in 2022 which is also known as HL-LHC. The ultimate configuration of HL-LHC will have 5 times luminosity and the current LAr front-end electronics need to be upgraded to sustain the higher radiation levels [7]. The present front-end architecture is very complex. A FEB has 11 ASICs based on different technologies, some of which (e.g. DMILL) are already obsolete. The FEB is designed and produced for 10 years operation with limited number (\~6\%) of spares, it has also intrinsic limitations on Level-1 trigger acceptance. Therefore
Fig. 2. Current LAr calorimeters readout electronics architecture

component level upgrade is not possible, and a new front-end architecture has been proposed as shown in Figure 3.

The new front-end readout will send out data continuously at each bunch crossing through high speed radiation resistant optical links. Large volume of data (\sim 100Gbps each board) will be processed real-time with the possibility of implementing trigger algorithms for clusters and electron/photon identification at a finer granularity than what is currently implemented. The new architecture simplifies the system design while keeping many options open, such as pipeline design, shaping and gain settings etc. Moreover it will eliminate the intrinsic limitation presently existing on Level-1 trigger acceptance. It requires many R&D efforts and the following section describes these R&D activities for LAr calorimeters readout electronics upgrade.

4. R&D Studies of LAr Calorimeters Readout Electronics Upgrade

4.1. Front-end ASIC Design

Front-end electronics design for HL-LHC becomes more critical with requirements of both high performance and higher radiation levels. The current front-end ASICs have been qualified at least 58kRad(Si) TID (total ionization dosage)[7], the qualification criteria of new front-end ASICs for HL-LHC will be \sim 5
times higher. A few R&D efforts are going on which are focused on the analog front-end and mixed-signal front-end ASIC design.

4.1.1. Analog Front-end ASIC

An analog front-end chip LAPAS (Liquid Argon PreAmplifier Shaper) has been designed and received in 2009. It uses IBM 8WL 0.13 μm SiGe (silicon-germanium) BiCMOS technology. The preamplifier design of LAPAS chip is based on low noise line-terminating circuit topology presently used in LAr calorimeters. It has full 16-bit dynamic range and very low noise (≈0.26 nV/√Hz). The shaper design of LAPAS chip is fully differential and based on CR − (RC)^2 topology with two gain settings (×1 and ×10). The output driver is adjustable, it is compatible with both gain selector block and differential ADC, either 2.34 V or 1.2 V.

The full characterization test of LAPAS chip with new test print circuit board shown in Figure 4 has been performed. The uniformity is better than 5% across 17 tested ASICs, the INL (integral non-linearity) over full scale of two gains is less than 0.1%. The TID test results of LAPAS chip show no significant concern. The measured input impedance (43 Ω) is larger than target value of 25 Ω, which is due to additional 0.8 Ω resistance in layout and can be resolved by adding resistor in series with feedback. The measured equivalent noise current (ENI) is ≈85 nA for 1 nF detector capacitance, which is higher than 75 nA target value and caused by larger layout resistance and increased feedback capacitance.

The future plan is to explore SiGe technologies from different manufactures (e.g., IHP, AMS). IHP 0.25 μm SiGe SG25H3P BiCMOS process has been chosen for next version of preamplifier design, which offers both lower cost and better performance due to the availability of PNP transistors. The layout of
the new preamplifier chip with test structures is shown in Figure 5. The schematics design, layout and simulation is approaching to the end, the new design will be submitted for fabrication in fall of 2011.

4.1.2. Mixed-signal Front-end: ADC

ADC is the most technologically challenging component in the new architecture due to the requirements of high dynamic range, radiation tolerance and SEE (single event effects) immunity. The strategy is to follow industrial development and verify the radiation tolerance of commercial ADCs. Some commercial off-the-shelf (COTS) ADCs have been tested for TID with $^{60}$Co γ source, the summary of TID test results is shown in Table 1. TI ADS5263 and Hittite HMCAD1520 could be potential candidates, but SEE will have to be evaluated carefully. No commercial ADC has been identified as a solution for the readout electronics upgrade so far, custom ADC is being developed.

<table>
<thead>
<tr>
<th>COTS ADC</th>
<th>Dynamic Range [bit]</th>
<th>Max Sampling Frequency [MS PS]</th>
<th>Analog Input Span $[V_{p-p}]$</th>
<th>Number of Channels per Chip</th>
<th>$P_{\text{total}}$ per Channel [mW]</th>
<th>Technology</th>
<th>Vendor</th>
<th>TID [kRad(Si)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD9265-80</td>
<td>16</td>
<td>80</td>
<td>2</td>
<td>1</td>
<td>210</td>
<td>0.18 μm CMOS</td>
<td>ADI</td>
<td>~220</td>
</tr>
<tr>
<td>AD9268-80</td>
<td>16</td>
<td>80</td>
<td>2</td>
<td>2</td>
<td>190</td>
<td>0.18 μm CMOS</td>
<td>ADI</td>
<td>~160</td>
</tr>
<tr>
<td>AD9269-40</td>
<td>16</td>
<td>40</td>
<td>2</td>
<td>2</td>
<td>61</td>
<td>0.18 μm CMOS</td>
<td>ADI</td>
<td>~120</td>
</tr>
<tr>
<td>AD9650-65</td>
<td>16</td>
<td>65</td>
<td>2.7</td>
<td>2</td>
<td>175</td>
<td>0.18 μm CMOS</td>
<td>ADI</td>
<td>~170</td>
</tr>
<tr>
<td>LTC2204</td>
<td>16</td>
<td>40</td>
<td>2.25</td>
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<td>LTC2173-14</td>
<td>14</td>
<td>80</td>
<td>2</td>
<td>4</td>
<td>94</td>
<td>0.18 μm CMOS</td>
<td>Linear</td>
<td>~105</td>
</tr>
<tr>
<td>LTC2193</td>
<td>16</td>
<td>80</td>
<td>2</td>
<td>2</td>
<td>125</td>
<td>0.18 μm CMOS</td>
<td>Linear</td>
<td>~100</td>
</tr>
<tr>
<td>ADS6445</td>
<td>14</td>
<td>125</td>
<td>2</td>
<td>4</td>
<td>320</td>
<td>0.18 μm CMOS</td>
<td>TI</td>
<td>~210</td>
</tr>
<tr>
<td>ADS5263</td>
<td>16</td>
<td>100</td>
<td>4</td>
<td>4</td>
<td>280</td>
<td>0.18 μm CMOS</td>
<td>TI</td>
<td>~680</td>
</tr>
<tr>
<td>HMCAD1520</td>
<td>14</td>
<td>105</td>
<td>2</td>
<td>4</td>
<td>133</td>
<td>0.18 μm CMOS</td>
<td>Hittite</td>
<td>~700</td>
</tr>
</tbody>
</table>

The Nevis09 chip has been designed and received in 2009. The layout and package of the chip is shown in Figure 6. It uses IBM 8RF 0.13 μm CMOS technology to implement 12-bit precision OTA (operational transconductance amplifier) with cascade of two T/H (track-and-hold) to achieve S/H (sample-and-hold) effect for testing. The test results show the OTA could reach 65dB, which is limited by the testing environment. The proton irradiation test of Nevis09 chip at MGH shows that the chip survives $2 \times 10^{14}$p/cm$^2$ fluence without noticeable change in spectral analysis. The proton beam energy is 227MeV, the total proton fluence is equivalent to $\sim 10.6$MRad(Si).

The Nevis10 chip has been designed using same technology as Nevis09 chip and received in late 2010. The layout of the Nevis10 chip is shown in Figure 7. It implements two 4-stage ADC pipelines with 1.5 bits/stage, and gain selector structures for each pipeline. The picture of test board is shown in Figure 8, which is used to test full functionality of Nevis10 chip with FPGA and quad channel 12-bit commercial ADC. The test results show the ENOB (Effective Number of Bits) that Nevis10 chip can achieve is $\sim 10$-bit.
A new test board has been designed to fix issues related to signal distortion, it will be used for detailed characterization test of Nevis10 chip.

![Fig. 8. Test board of Nevis10 chip](image1)

Latency of ADC needs to be minimized to overcome the bottleneck of the latency time from the analog memory used in the present configuration. Pipeline ADC has intrinsic long latency, an alternative ADC architecture is being studied to optimize the ADC latency. An overview of the so called SAFLASH converter is shown in Figure 9. The converter is a cascaded scheme of a flash converter as the MSB stage followed by a SAR converter for the LSB stage. A SAR converter also offers a natural serializing possibility. Flash ADC stage is very fast compared to the SAR stage, so two SAR stages are used in parallel to boost the speed of the full converter. The simulation shows the latency of SAFLASH converter is \( \sim 45 \text{ ns} \). This design is planned to be prototyped in mid 2012.

### 4.1.3. HEC Cold Electronics

The HEC preamplifier and summing boards (PSB) are located at the perimeter of the HEC wheels inside the liquid Argon. The ASIC on PSB is designed and built by Gallium-Arsenide (GaAs) TriQuint QED-A 1 \( \mu \text{m} \) technology[8]. The present ATLAS requirements for the HEC PSB boards are \( 2 \times 10^{12} \text{ n/cm}^2 \) per year. After 10 years of LHC operation, the present HEC cold electronics would be operated at its limit. It is therefore planned to develop a new ASIC that will be ten times more radiation hard against neutrons.

<table>
<thead>
<tr>
<th>Material Transistor</th>
<th>SiGe Bipolar</th>
<th>SiGe Bipolar</th>
<th>SiGe Bipolar</th>
<th>Si Bipolar</th>
<th>Si CMOS FET</th>
<th>Si CMOS FET</th>
<th>Si CMOS FET</th>
<th>GaAs FET</th>
<th>GaAs FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foundry Type</td>
<td>IHP npn</td>
<td>IBM npn</td>
<td>AMS npn</td>
<td>IHP npn</td>
<td>IHP npn</td>
<td>IHP npn</td>
<td>IHP npn</td>
<td>Triquint</td>
<td>Sirenza</td>
</tr>
<tr>
<td>10 MHz</td>
<td>5%</td>
<td>5%</td>
<td>5%</td>
<td>4%</td>
<td>4%</td>
<td>4%</td>
<td>3%</td>
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<td>4%</td>
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<tr>
<td>40 MHz</td>
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<td>5%</td>
<td>2%</td>
<td>3%</td>
<td>3%</td>
<td>2%</td>
<td>2%</td>
<td>2%</td>
</tr>
</tbody>
</table>

The radiation hardness against neutron irradiation has been studied for transistors of SiGe, Si and GaAs technologies. The loss of gain for the transistors for two different frequencies, studied at a neutron fluence of \( 2 \times 10^{15} \text{ n/cm}^2 \) is shown in Table 2. All technologies investigated show only a small degradation of the gain up to the irradiation level expected for HL-LHC. Based on these studies both options, bipolar SiGe as well as CMOS FET technologies, are sufficiently stable under neutron irradiation and are being investigated further. IHP CMOS has been chosen as the technology for HEC cold electronics with IHP bipolar SiGe and IBM bipolar SiGe as backup solutions. The simulation models including radiation and low temperature effects are being developed right now. A first design of amplifier based on IHP SGB25V CMOS technology has been finished and planned to be submitted soon.
4.2. Radiation Resistance Optical Link

The new readout architecture requires high bandwidth radiation resistant optical link to transmit data out of the detector. The SMU_P1 chip based on 0.25 μm Silicon on Sapphire CMOS technology has been received in 2009. It includes a 5Gbps 16:1 serializer LOCs1, a 5GHz LC VCO based PLL, the CML driver, a divide-by-16 circuit, a varactor and an SRAM block.

The full characterization test shows the LOCs1 has ~62ps total jitter and ~69% eye opening at 10^{-12} BER. The jitter tolerance of LOCs1 is larger than 1.8UI when jitter frequency is less than 1.56MHz. The proton irradiation test of LOCs1 at IUCF with 200MeV proton beam shows the extrapolated BER is much less than 10^{-12}, no bit error has been observed. The LOCs1 was functioning well after irradiation with total power current change less than 6%.

The second version of the serializer LOCs2 is being developed right now. It will include two channels of serializers, each channel has 16-bit LVDS parallel input data and 1-bit CML serial output. Each serializer operates at ~8Gbps which is limited by Silicon on Sapphire GC process, new PC process which can reach 10Gbps is being investigated. The detailed description of LOCs1 and LOCs2 design is reported in a separate article by T. Liu in this proceedings.

4.3. Back-end High-speed Processing Unit

The ROD is the heart of the back-end electronics system, serving as the bridge between the front-end electronics system, the ROS and possibly the L1Calo system. With the new front-end architecture, ROD will have to be upgraded to process huge amount of data (≈1.5Tbps per board) from the detector. A possible implementation, currently under study, of the ROD board is shown in Figure 10.

Fig. 10. Schematic representation of the LAr signal dataflow

A SubROD and a SubROD Injector based on ATCA platform have been developed and shown in Figure 11 and 12, the integration test was performed in Oct 2009. They use commercial parallel optical transceiver running at 75Gbps with MPO®/MTP low profile connector. SERDES of Xilinx Virtex-5 FPGA and Altera Stratix II GX FPGA has been tested successfully. The next version of SubROD and SubROD Injector will be in AMC format, which offers low cost MicroTCA test platform while keeping the modular design with the ATCA carrier card. The AMC SubROD and SubROD Injector will use Xilinx Virtex-7 and Altera Stratix V FPGA respectively. Due to limited space and high data bandwidth, the small profile optical receivers, such as Avago MiniPod and MicroPod, are being investigated.

An FMC compliant low cost ATCA Controller Mezzanine has been developed and shown in Figure 13. It is an IPM controller for communication with shelf manager and power management etc. It can provide ATCA board management via Ethernet for firmware upgrade, monitoring and configuration etc. The ARM
Cortex M3 processor and Xilinx Spartan 6 FPGA are being used on this card, the software development is compliant with IPMI 2.0 specification. At the same time, an ATCA Test Board with ATCA Controller Mezzanine mounted on has been developed and shown in Figure 14. It has been used to check board configuration and test ATCA compliant power supplies. It is also used to verify FPGA design, such as communication with DDR3 and flash memory, for ROD Evaluator Board. The ROD Evaluator Board is being developed right now which has three Altera Stratix IV FPGAs and 48 transceivers running at up to 8.5Gbps.

The feasibility of fast and large volume of data preparation within fixed latency budget for Level-1 trigger upgrade is being investigated. The test of commercial boards in ATCA platform to exercise the software framework and verify the 10Gbit Ethernet communications between ATCA blades has been performed.
The interface between ROD and ROS over 10Gbit Ethernet has also been tested. The FPGA firmware for digital signal filter design with minimum latency has been implemented in Xilinx Virtex-5 FPGA. The filter operates up to 350MHz, the latency is only 5 FPGA clock cycles. The calibration constants can be dynamically loaded into the filter without FPGA firmware update.

4.4. Low Voltage Power Supply

The current front-end power supply system is of centralized architecture with each FEC having its own LVPS which takes 280V input from USA15 through $\sim 100$ m cable and provides seven different voltages. A LVPS has high power density ($\sim 3.2$kW) and is water cooled. The new LVPS will have to sustain higher radiation levels, even though total power budget of front-end electronics will be kept same. The number and levels of voltages have to be rationalized, to reduce different voltages across devices. Currently commercial power FETs based on different technologies, such as GaN (gallium nitride) and SiC (silicon carbide), are being evaluated in radiation environment. Two possible LVPS architectures, distributed power architecture and intermediate bus architecture, are being investigated.

5. Evolution from Today to HL-LHC

Before the full replacement of LAr calorimeters readout electronics in HL-LHC, one or more intermediate upgrade steps have been proposed recently. The step one upgrade is to install a demonstrator system in 2013/14 when LHC is shutdown, two TBBs will be replaced by a mixed analog and digital version. The new TBB (sTBB) will keep the analog signal sums and trigger outputs identical to the current TBB, this will keep the L1Calo system intact. At the same time, the digitization of sums of four individual LAr layers will be sent out of the detector, the layer sums of LAr front and middle layers will have finer granularity ($\Delta \eta \times \Delta \phi = 0.025 \times 0.1$). This will provide improved granularity both longitudinally and transversally. The step two upgrade is to extend the sTBB to the full LAr calorimeters in Phase-I upgrade, it will have the potential to implement global object searches through the full calorimeter in the early trigger phases. The proposed new system architecture is shown in Figure 15.

Fig. 15. Proposed new system architecture for demonstrator and Phase-I upgrade.
Integration and system aspects of the sTBB are part of the initial studies and developments given the several external constraints and boundary conditions. The power consumption of the board is limited to 80-100 W, corresponding to a 350mW/channel. Density of the readout channels is a factor 2.5 higher than the current FEB design. Power management, cooling interface, noise minimization and proper grounding are among the system aspects to include in the design and specification. To maximize flexibility, easiness of maintenance and future upgrade of external interfaces, the board is conceived as assembly of different pluggable modules as illustrated in Figure 16.

![Fig. 16. 3D model of the sTBB for mechanical integration studies and developments](image)

6. Summary

Higher selectivity of the Level-1 calorimeter trigger, radiation tolerance and natural aging of the electronics are the driving motivations for an upgrade of the ATLAS LAr calorimeters readout electronics for HL-LHC. It also offers opportunity to apply modern technology and revise architecture. A new front-end readout architecture has been proposed and is being developed for the readout electronics upgrade which needs to meet many challenges. The upgrade R&D projects are progressing smoothly and more test results are expected in the near future.

An evolutionary scenario towards a digital calorimeter readout at HL-LHC has been proposed recently, which introduces a staged upgrade with hybrid demonstrators including both analog and digital trigger readout as an intermediate step. A well proven demonstrator will provide valuable information on reliabilities before sTBB is expanded to the full LAr calorimeters in Phase-I upgrade. The new architecture will provide digital trigger data that can be used by L1Calo for both Phase-I and HL-LHC upgrade.

References