



# FPGA as a tool for hardware realization of feedback control

Ján Cigánek\*, Michal Kocúr, Štefan Kozák

Faculty of Electrical Engineering and Information Technology, Slovak University of Technology in Bratislava, Ilkovičova 3, 841 04 Bratislava, Slovakia<sup>1</sup>

Available online 2 December 2015

## Abstract

The presented paper deals with the development of robust control algorithm based on reflection vectors methodology. This approach of controller design is guaranteeing stability, robustness and high performance. The presented method was successfully tested for stable, unstable and strong oscillating processes and for systems with parametrical model uncertainty. The proposed algorithm can be effectively realized using field-programmable gate array (FPGA) structure as it is shown in the case study – the hardware realization using FPGA technology for DC motor. All presented simulations and co-simulations were realized in MATLAB-Simulink.

© 2015 The Authors. Production and hosting by Elsevier B.V. on behalf of Electronics Research Institute (ERI). This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>).

**Keywords:** Robust control; Robust stability; Parametrical uncertainty; Quadratic programming; Reflection vectors; FPGA

## 1. Introduction

During last ten years, development of robust control elementary principles and evolution of new robust control methods for different model uncertainty types are visible. Based on theoretical assumptions, modeling and simulation methods, an effective approach to the control of processes with strong and undefined uncertainties is designed. Such uncertainties are typical for biotechnology processes, chemical plants, automobile industry, aviation, etc. For such processes, it is necessary to design robust and practical algorithms which ensure the high performance and robust stability using proposed mathematical techniques with respect the parametric and unmodeled uncertainties. Solution to such problems is possible using robust predictive methods and “soft-techniques” which include fuzzy sets, neuron networks and genetic algorithms.

Robust control is used to guarantee stability of plants with parameter changes. The robust controller design consists of two steps:

\* Corresponding author.

E-mail addresses: [jan.ciganek@stuba.sk](mailto:jan.ciganek@stuba.sk) (J. Cigánek), [michal.kocur@stuba.sk](mailto:michal.kocur@stuba.sk) (M. Kocúr), [stefan.kozak@stuba.sk](mailto:stefan.kozak@stuba.sk) (Š. Kozák).

<sup>1</sup> <http://www.fe.i.stuba.sk>.

Peer review under the responsibility of Electronics Research Institute (ERI).



<http://dx.doi.org/10.1016/j.jesit.2015.11.004>

2314-7172/© 2015 The Authors. Production and hosting by Elsevier B.V. on behalf of Electronics Research Institute (ERI). This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>).

- Analysis of parameter changes and their influence for closed-loop stability,
- Robust control synthesis.

There are two approaches for implementing control systems using digital technology. The first approach is based on software which implies a memory-processor interaction. The memory holds the application program while the processor fetches, decodes, and executes the program instructions. Programmable logic controllers (PLCs), microcontrollers, microprocessors, digital signal processors (DSPs) and general purpose computers are tools for software implementation. On the other hand, the second approach is based on hardware. Early hardware implementation is achieved by magnetic relays extensively used in old industry automation systems. Then, it became achievable by means of digital logic gates and medium scale integration (MSI) components. When the system size and complexity increases, application specific integrated circuits (ASICs) are utilized. The ASIC must be fabricated on a manufacturing line, a process that takes several months, before it can be used or even tested (Kozák, 2002; Kocúr, 2013). FPGAs are configurable ICs and used to implement logic functions.

Today’s high-end FPGAs can hold several millions gates and have some significant advantages over ASICs. They ensure ease of design, lower development costs, more product revenue and the opportunity to speed products to market (Viswanathan, 2005). At the same time, they are superior to software-based controllers as they are more compact, power-efficient, while adding high speed capabilities.

**2. Problem formulation**

Let us consider the robust control synthesis of a scalar discrete-time control loop. The transfer function of the original continuous-time system is described by the transfer function

$$G_P(s) = \frac{\bar{B}(s)}{\bar{A}(s)} e^{-Ds} = \frac{\bar{b}_m s^m + \bar{b}_{m-1} s^{m-1} + \dots + \bar{b}_0}{\bar{a}_n s^n + \bar{a}_{n-1} s^{n-1} + \dots + \bar{a}_0} e^{-Ds} \tag{1}$$

The transfer function of (1) can be converted to its discrete-time counterpart

$$G_P(z^{-1}) = \frac{b_0 + b_1 z^{-1} + \dots + b_n z^{-n}}{1 + a_1 z^{-1} + \dots + a_n z^{-n}} z^{-d} \tag{2}$$

For (2) a discrete-time controller is to be designed in form

$$G_R(z) = \frac{q_0 + q_1 z^{-1} + \dots + q_\nu z^{-\nu}}{1 + p_1 z^{-1} + \dots + p_\mu z^{-\mu}} = \frac{Q(z)}{P(z)} = \frac{U(z)}{E(z)} \tag{3}$$

The corresponding closed-loop characteristic equation is

$$1 + G_P(z^{-1})G_R(z^{-1}) = 0 \tag{4}$$

Substituting (3) and (2) in (4), after a simple manipulation yield the characteristic equation

$$1 + G_P G_R = (1 + p_1 z^{-1} + \dots + p_\mu z^{-\mu})(1 + a_1 z^{-1} + \dots + a_n z^{-n}) + (q_0 + q_1 z^{-1} + \dots + q_\nu z^{-\nu})(b_1 z^{-1} + \dots + b_n z^{-n}) z^{-d} = 0 \tag{5}$$

Unknown coefficients of the discrete controller can be designed using various methods. In this paper, a robust controller design method based on reflection vectors is used.

The pole assignment problem is as follows: find a controller  $G_R(z)$  such that  $C(z) = e(z)$  where  $e(z)$  is a given (target) polynomial of degree  $k$ . It is known (Keel and Bhattachayya, 1999) that, when  $\mu = n - 1$ , the above problem has a solution for arbitrary  $e(z)$  whenever the plant has no common pole-zero pairs. In general, for  $\mu < n - 1$  exact attainment of a desired target polynomial  $e(z)$  is impossible.

Let us relax the requirement of attaining the target polynomial  $e(z)$  exactly and enlarge the target region to a polytope  $V$  in the polynomial space containing the point  $e$  representing the desired closed-loop characteristic polynomial. Without any restriction we can assume that  $a_n = p_0 = 1$  and deal with monic polynomials  $C(z)$ , i.e.,  $\alpha = 1$ .

Let us introduce the stability measure as  $\rho = c^T c$ , where

$$c = S^{-1}C \quad (6)$$

and  $S$  is a matrix of dimensions  $(n + \mu + 1) \times (n + \mu + 1)$  representing vertices of the target polytope  $V$ . For monic polynomials holds

$$\sum_{i=1}^{k+1} c_i = 1 \quad (7)$$

where  $k = n + \mu$ . If all coefficients are positive, i.e.,  $c_i > 0, i = 1, \dots, k + 1$ , then the point  $C$  is placed inside the polytope  $V$ .

The minimum  $\rho$  is attained if

$$c_1 = c_2 = \dots = c_{k+1} = \frac{1}{k+1} \quad (8)$$

Then the point  $C$  is placed in center of the polytope  $V$ . In matrix form, we have

$$C = Gx \quad (9)$$

where  $G$  is the Sylvester matrix of the plant (Cigánek and Kozák, 2010) with dimensions  $(n + \mu + d + 1) \times (\mu + \nu + 2)$  and  $x$  is the  $(\mu + \nu + 2)$ -vector of controller parameters:  $x = [p_\mu, \dots, p_1, 1, q_\nu, \dots, q_0]^T$ .

Now, we can formulate the following control design problem: find a discrete controller, where the closed-loop characteristic polynomial  $C(z)$  is placed:

- In a stable target polytope  $V, C(z) \in V$  (to guarantee stability),
- As close as possible to a target polynomial  $e(z), e(z) \in V$  (to guarantee performance).

Let the polytope  $V$  denote the  $(k + 1) \times N$  matrix composed of coefficient vectors  $v_j, j = 1, \dots, N$  corresponding to vertices of the polytope  $V$  (Nurges, 2006).

Then we can formulate the above controller design problem as an optimization task: find  $x$  that minimizes the cost function

$$J_1 = \min_x x^T G^T Gx - 2e^T Gx = \min_x \|Gx - e\|^2 \quad (10)$$

subject to the linear constraints

$$Gx = Vw(x), \quad (11)$$

$$w_j(x) > 0, \quad j = 1, \dots, N, \quad (12)$$

$$\sum_j w_j(x) = 1. \quad (13)$$

Here,  $w(x)$  is the vector of weights of the polytope  $V$  vertices to obtain the point  $C = Gx$ . Fulfillment of the latter two constraints (12) and (13) guarantees that the point  $C$  is indeed located inside the polytope  $V$ . Then, finding the robust pole-placement controller coefficients represents an optimization problem that can be solved using the Matlab Toolbox OPTIM (quadprog) with constraints.

Generally  $J_1$  is a kind of distance to the center of the target polytope  $V$ . It is better to use another criterion  $J_2$ , which measures the distance to the Schur polynomial  $E(z)$ :

$$J_2 = (C - E)^T (C - E) = (Gx - E)^T (Gx - E). \quad (14)$$

It is possible to use the weighted combination of  $J_1$  and  $J_2$

$$J = (1 - \alpha)J_1 + \alpha J_2, \quad 0 \leq \alpha \leq 1 \quad (15)$$

and to solve the following quadratic programming task:

$$J = \min_x \{x^T G^T [(1 - \alpha)(SS^T)^{-1} + \alpha I_{k+1}] Gx - 2\alpha E^T Gx\}, \quad S^{-1} Gx < 0. \tag{16}$$

Assume the discrete robust controller design task with parametrical uncertainties in system description. Let us also assume that coefficients of the discrete-time system transfer functions  $a_n, \dots, a_1$  and  $b_n, \dots, b_1$  are placed in polytope  $W$  with the vertices  $d^j = [a_n^j, \dots, a_1^j, b_n^j, \dots, b_1^j]$ :

$$W = \text{conv}\{d^j, \quad j = 1, \dots, M\} \tag{17}$$

As (9) is linear in system parameters, it is possible to *claim* that for arbitrary vector of the controller coefficients  $x$  is the vector of the characteristic polynomial coefficients  $C(z)$  placed in the polytope  $A$  with vertices  $a^1, \dots, a^M$ :

$$A = \text{conv}\{a^j, \quad j = 1, \dots, M\} \tag{18}$$

where  $a^j = D^j x$  and  $D^j$  is the Sylvester matrix of dimensions  $(n + \mu + d + 1) \times (\mu + v + 2)$ , composed of vertices set  $d^j$ , as in case of the exact model (9).

### 2.1. Stable region computation via reflection coefficients

Polynomials are usually specified by their coefficients or roots. They can be characterized also by their reflection coefficients using Schur–Cohn recursion.

Let  $C_k(z^{-1})$  be a monic polynomial of degree  $k$  with real coefficients  $c_i \in R, i = 0, \dots, k$

$$C(z^{-1}) = 1 + c_1 z^{-1} + \dots + c_k z^{-k} \tag{19}$$

Reciprocal polynomial  $C_k^*(z^{-1})$  of the polynomial  $C_k(z^{-1})$  is defined in Diaz-Barrero and Egozcue (2004) as follows

$$C_k^*(z^{-1}) = c_k + c_{k-1} z^{-1} + \dots + c_1 z^{-k+1} + z^{-k} \tag{20}$$

Reflection coefficients  $r_i, i = 1, \dots, k$ , can be obtained from the polynomial  $C_k(z^{-1})$  using backward Levinson recursion (Picinbono and Bendir, 1986)

$$z^{-1} C_{i-1}(z^{-1}) = \frac{1}{1 - |r_i^2|} [C_i(z^{-1}) - r_i C_i^*(z^{-1})] \tag{21}$$

where  $r_i = -c_i$  and  $c_i$  is the last coefficient of  $C_i(z^{-1})$  of degree  $i$ . From (21) we obtain in a straightforward way:

$$C_i(z^{-1}) = z^{-1} C_{i-1}(z^{-1}) + r_i C_{i-1}^*(z^{-1}). \tag{22}$$

Expressions for polynomial coefficients  $C_{i-1}(z^{-1})$  and  $C_i(z^{-1})$  result from Eqs. (22) and (23):

$$C_{i-1}(z^{-1}) = \frac{1}{1 - |r_i^2|} \left[ \sum_{j=0}^{i-1} (c_{i,j+1} - r_i c_{i,i-j-1}) z^{-j} \right] \tag{23}$$

$$C_i(z^{-1}) = \sum_{j=0}^i (c_{i-1,j-1} + r_i c_{i-1,i-j-1}) z^{-j}. \tag{24}$$

The reflection coefficients  $r_i$  are also known as Schur–Szegő parameters (Diaz-Barrero and Egozcue, 2004), partial correlation coefficients (Kay, 1988) or  $k$ -parameters (Oppenheim and Schaffer, 1989). Presented forms and structures were effectively used in many applications of signal processing (Oppenheim and Schaffer, 1989) and system identification (Kay, 1988). A complete characterization and classification of polynomials using their reflection coefficients instead of roots (zeros) of polynomials is given in (Diaz-Barrero and Egozcue, 2004).

The main advantage of using reflection coefficients is that the transformation from reflection to polynomial coefficients is very simple. Indeed, according to (22) and (24), polynomial coefficients  $c_i$  depend multilinearly on the reflection coefficients  $r_i$ . If the coefficients  $c_i \in R$  are real, then also the reflection coefficients  $r_i \in R$  are real.

Transformation from reflection coefficients  $r_i, i = 1, \dots, k$ , to polynomial coefficients  $c_i, i = 1, \dots, k$ , is as follows

$$\begin{aligned} c_i &= c_i^{(k)}, \\ c_i^{(i)} &= -r_i, \\ c_j^{(i)} &= c_j^{(i-1)} - r_i c_{i-j}^{(i-1)} \\ i &= 1, \dots, k; \quad j = 1, \dots, i-1 \end{aligned} \quad (25)$$

**Lemma 1.** A linear discrete-time dynamic system is stable if its characteristic polynomial is Schur stable, i.e., if all its poles lie inside the unit circle.

The stability criterion in terms of reflection coefficients is as follows (Diaz-Barrero and Egozcue, 2004).

**Lemma 2.** A polynomial  $C(z^{-1})$  has all its roots inside the unit disk if and only if  $|r_i| < 1, i = 1, \dots, k$ .

A polynomial  $C(z^{-1})$  lies on the stability boundary if some  $r_i = \pm 1, i = 1, \dots, k$ . For monic Schur polynomials, there is a one-to-one correspondence between  $C = [c_k, \dots, c_1]^T$  and  $r = [r_1, \dots, r_k]^T$ .

Stability region in the reflection coefficient space is simply the  $k$ -dimensional unit hypercube  $R = \{r_i \in (-1, 1), i = 1, \dots, k\}$ . The stability region in the polynomial coefficient space can be found starting from the hypercube  $R$  (Nurges, 2005).

## 2.2. Stable polytope of reflection vectors

It will be shown that, for a family of polynomials the linear cover of the so-called reflection vectors is Schur stable.

**Definition 1.** The reflection vectors of a Schur stable monic polynomial  $C(z^{-1})$  are defined as the points on stability boundary in polynomial coefficient space generated by changing a single reflection coefficient  $r_i$  of the polynomial  $C(z^{-1})$ .

Let us denote the positive reflection vectors of  $C(z^{-1})$  as  $v_i^+(C) = (C | r_i = 1), i = 1, \dots, k$ , and the negative reflection vectors of  $C(z^{-1})$  as  $v_i^-(C) = (C | r_i = -1), i = 1, \dots, k$ .

The following assertions hold:

1. Every Schur polynomial has  $2k$  reflection vectors  $v_i^+(C)$  and  $v_i^-(C), i = 1, \dots, k$ ;
2. All reflection vectors lie on the stability boundary ( $r_i^v = \pm 1$ );
3. The line segments between reflection vectors  $v_i^+(C)$  and  $v_i^-(C)$  are Schur stable.

In the following theorem a family of stable polynomials is defined such that the polytope generated by reflection vectors of these polynomials is stable (Nurges, 2006).

**Theorem 1.** Consider  $r_1^C \in (-1, 1), r_k^C \in (-1, 1)$  and  $r_2^C = \dots = r_{k-1}^C = 0$ . Then the inner points of the polytope  $V(C)$  generated by the reflection vectors of the point  $C$

$$V(C) = \text{conv}\{v_i^\pm(C), \quad i = 1, \dots, k\} \quad (26)$$

are Schur stable.

## 2.3. Robust controller design

A robust controller is to be designed such that the closed-loop characteristic polynomial is placed in the stable polytope (linear cover) of reflection vectors. It means that the following problems have to be solved:

1. Choice of initial polynomial  $C(z^{-1})$  for generating the polytope  $V(C)$ ,
2. Choice of  $k + 1$  most suitable vertices of  $V(C)$  to build a target simplex  $S$ ,
3. Choice of a target polynomial  $E(z^{-1})$ .

In the following section some “thumb rules” are given for choosing a stable target simplex  $S$ .

To choose  $k + 1$  vertices of the target simplex  $S$  we use the well known fact that poles with positive real parts are preferred to those with negative ones (Ackermann, 1993). The positive reflection vectors  $v_i^+(C)$  with  $i$  odd and negative reflection vectors  $v_i^-(C)$  with  $i$  even are chosen yielding  $k$  vertices. The  $(k + 1)$ th vertex of the target simplex  $S$  is chosen as the mean of the remaining reflection vectors.

The target polynomial  $E(z^{-1})$  of order  $k$  is reasonable to be chosen inside the stable polytope of reflection vectors  $V(C)$ . A common choice is  $E(z^{-1}) = C(z^{-1})$ .

For higher-order polynomials, the size of the target simplex  $S$  is considerably less than the volume of the polytope of reflection vectors  $V$ . That is why the above quadratic programming method with a preselected target simplex  $S$  works only if uncertainties are sufficiently small. Otherwise, it is reasonable to use some search procedure to find a robust controller such that the polytope of closed-loop characteristic polynomial is placed inside the stable polytope of reflection vectors  $V(C)$ .

### 3. Implementation of control algorithm

The digital form of the controller can be obtained from (3). Recursive form of control algorithm is expressed by the following equation:

$$u(k) = q_1 e(k - 1) + q_2 e(k - 2) - p_1 u(k - 1) - p_2 u(k - 2) \quad (27)$$

For implementation of control algorithm (27) for FPGA is necessary to decompose equation into simple arithmetic operations:

$$\begin{aligned} e(k) &= w(k) - y(k) \\ q_1 e_{-1} &= q_1 * e(k - 1) \\ q_2 e_{-2} &= q_2 * e(k - 2) \\ p_1 u_{-1} &= p_1 * u(k - 1) \\ p_2 u_{-2} &= p_2 * u(k - 2) \\ s_1 &= q_1 e_{-1} + q_2 e_{-2} \\ s_2 &= p_1 u_{-1} + p_2 u_{-2} \\ s_3 &= s_1 - s_2 \end{aligned} \quad (28)$$

Control output  $u$  must be bounded in the range from  $u_{\min}$  to  $u_{\max}$ .

$$\begin{aligned} u_{\max} &\rightarrow \text{if}(s_3 > u_{\max}) \\ u(k) &= s_3 \rightarrow \text{if}(u_{\min} \leq s_3 \leq u_{\max}) \\ u_{\min} &\rightarrow \text{if}(s_3 < u_{\min}) \end{aligned} \quad (29)$$

In this case, the parallel design of control algorithm is used, which means that each of the operation has its own arithmetic unit, either accumulator or multiplier. Parallel design is shown in Fig. 1.

Each sampling period is loaded the motor system output  $y(k)$  from the input in. Control error  $e(k)$  is computed in sub block where the signal  $y(k)$  is subtracted from  $w(k)$ . Signal  $e(k)$  is held in the registry *REG1* for one sampling period. Register *REG1* output signal is thus  $e(k - 1)$ . In the same manner,  $e(k - 2)$ ,  $u(k - 1)$  and  $u(k - 2)$  are recorded at *REG2*, *REG3* and *REG4* by latching  $e(k - 1)$ ,  $u(k)$  and  $u(k - 1)$  respectively. For multiplication, they are using digital signal processor (DSP) cores in FPGA chip. Results of multiplications are counted in to control output. This control output is then bounded in the range from  $-12$  V to  $12$  V.

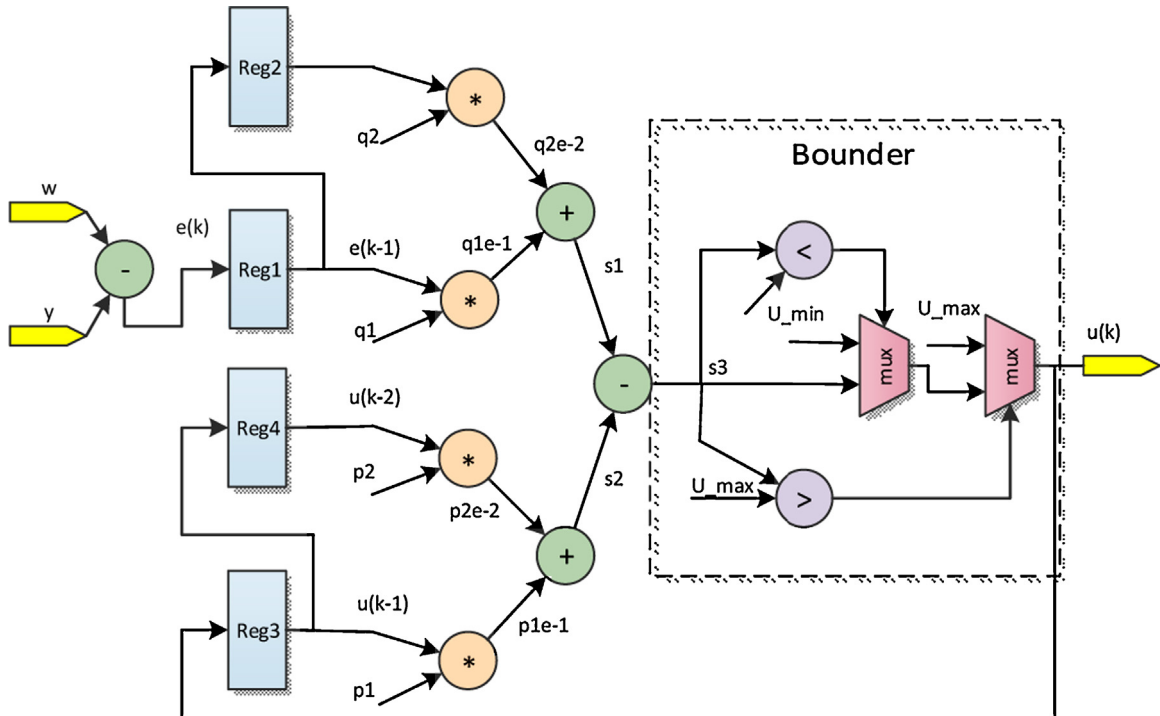


Fig. 1. Parallel design of the control algorithm.



Fig. 2. Fixed-point control output.

Inputs  $w$  and  $y$  are represented with rpm (revolutions per minute). Input range is  $-2048$  to  $2047$  rpm, because of the 12-bit signed data type. Output of the controller is represented with volts. In signed binary representations the maximum control output is  $12_{(10)} \text{ V} = 01100_{(2)}$  and the minimum is  $-12_{(10)} \text{ V} = 10100_{(2)}$ . We can write this range into 5 bits. Real numbers are useful for better quantization of the control output. For implementation of the real numbers it has been used fixed point arithmetic (Bishop, 2006). As we can see in Fig. 2 first (MSB) bit of output vectors is reserved for a sign. Next four bits are reserved for the integer part and last seven bits are used for the fractional part.

Fixed point arithmetic is applied throughout the control algorithm. In designing this algorithm, the fixed-point arithmetic range rules must be respected. The data widths in the fixed-point arithmetic were designed that there is no possibility of an overflow. For example, the result of summation or subtraction of two 12-bit vectors has range 13-bit.

In the case of parallel design of control algorithm, the control output after last summation (resp. subtraction) has range 40-bit (16-bit for fractional part). It must be used a bounder block to ensure of range ( $-12 \text{ V}$  to  $12 \text{ V}$ ) for 12-bit. Bounder is the value limitation logic that keeps the output in the defined range. Bounded signal is latched at register REG3, thus becomes  $u(k - 1)$  of next cycle. In this way the anti-windup protection is also ensured.

Before the hardware implementation the control algorithm is verified of software Matlab-Simulink. System generator toolbox ensures that between the blocks gateway in and gateway out algorithm performs as it was implemented on FPGA. We proposed decomposed control algorithm to be consisted of Xilinx blocks (Fig. 3). In this step we determined the minimum widths of the internal signals. For the implementation of decimals numbers it has been used fixed point arithmetic.

Based on the successful verification of the Xilinx blocks algorithm we created the VHDL code which is used in the resulting hardware solutions (Xilinx, 2012). The VHDL code we have developed in Xilinx ISE Design Suite. For the

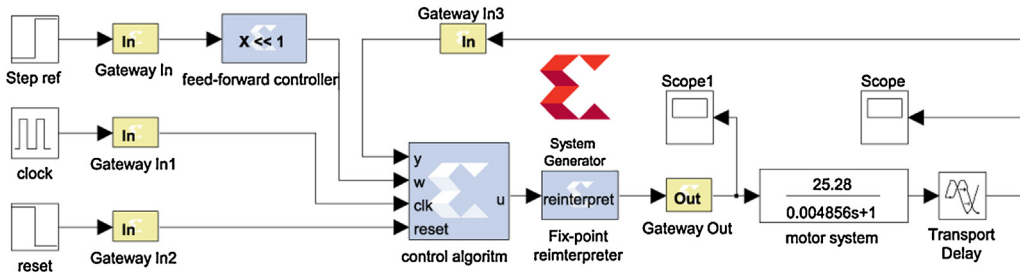


Fig. 3. Schematic of control circuit using Xilinx blocks.

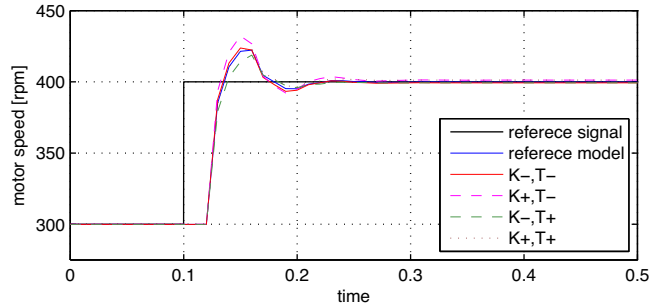


Fig. 4. Time response of outputs and reference variable under robust controller.

implementation of fixed point arithmetic in VHDL code there is used library (ieee\_proposed.fixed\_pkg). Simulation of VHDL code is possible using Xilinx black box block. Simulation results are in Fig. 4.

#### 4. Case study

Consider a DC system described by the first order nominal transfer function

$$G_p(s) = \frac{B(s)}{A(s)} e^{-Ds} = \frac{K}{T_1 s + 1} e^{-Ds} = \frac{153.4}{0.07392s + 1} e^{-0.01s} \quad (30)$$

where coefficients  $K, T_1$  are varying in uncertainty intervals  $K \in (150; 160), T_1 \in (0.070; 0.078)$

Consider the nominal continuous-time transfer function which is converted to the discrete-time form with the sampling period  $T = 0.01$  s:

$$G_p(z^{-1}) = \frac{19.41 \cdot z^{-2}}{1 - 0.8735z^{-1}} \quad (31)$$

The main task is to design a robust discrete-time controller (3), with polynomial degrees  $\nu = 1, \mu = 2$ .

From the transfer function (31) and matrix form of (9) we can obtain:

$$C = \begin{bmatrix} 0 & 0 & 0 & 19.4097 & 0 \\ -0.8735 & 0 & 0 & 0 & 19.4097 \\ 1 & -0.8735 & 0 & 0 & 0 \\ 0 & 1 & -0.8735 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} p_2 \\ p_1 \\ 1 \\ q_1 \\ q_0 \end{bmatrix}$$

Let us choose the initial polynomial  $C(z^{-1})$  for generating the polytope  $V(C)$  as follows

$$C(z) = 1 + 0.1z^{-1} \quad (32)$$

with reflection coefficients  $r_1 = -0.1, r_2 = r_3 = r_4 = 0$ .



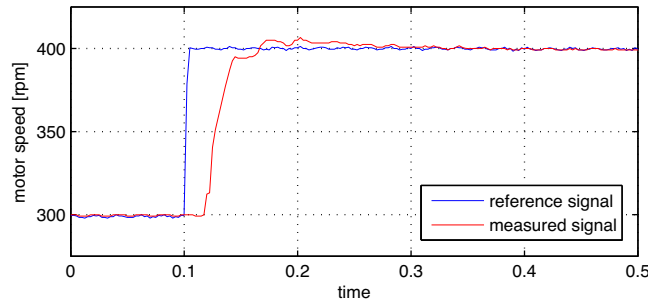


Fig. 5. Hardware realization of control algorithm.

Now, we can find the reflection vectors  $v_i(C)$  of the initial polynomial  $C(z^{-1})$  leading to the matrix form of the target simplex  $S$  (vertex polynomial coefficients)

$$S = \begin{bmatrix} -0.25 & 0 & 0.3 & 0.15 & 0.1 \\ 0 & -0.7 & -0.3 & 0.5 & 0 \\ -0.25 & 0.5 & 0 & -0.5 & 0.2 \\ 0.5 & 0 & 0.4 & -0.4 & 0 \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix} \quad (33)$$

The discrete-time controller design task for the nominal transfer function (30) has been solved via quadratic programming taking  $\alpha=0.05$  in the cost function  $J$  (16).

For the selected target simplex  $S$  we have obtained the following discrete-time feedback controller

$$G_{FB}(z^{-1}) = \frac{Q(z^{-1})}{P(z^{-1})} = \frac{0.03145 + 0.01117z^{-1}}{1 + 0.9311z^{-1} + 0.6679z^{-2}} \quad (34)$$

and the control law is expressed in recursive form

$$u_2(k) = -0.931u_2(k-1) - 0.668u_2(k-2) + 0.0315y(k) + 0.0112y(k-1) \quad (35)$$

Corresponding closed-loop step response under the feedback controller (34) and feed-forward controller  $G_{FF}(z^{-1})=S(z^{-1})/P(z^{-1})=2$  is in Fig. 5.

For verification of the FPGA implementation of the digital controller we realized a practical experiment. In simulation with Xilinx blocks we made step of reference signal at 0.01 s.

The same controller (31) was used also for hardware realization to control real DC-motor. The graphical results are shown in Fig. 5.

## 5. Conclusion

The presented paper deals with the new approach of robust controller design using the reflection vectors techniques. The control structure consists of feed-forward and feedback part. Proposed algorithm was tested using FPGA technology for DC motor. The illustrative example was solved using quadratic programming for suitably defined performance function. The obtained results demonstrate very effective applicability of the theoretical principles for process control with parametrical model uncertainty. Digital controller was successfully implemented and hardware realized on Artix-7 FPGA board. FPGA structure is very suitable for high speed processes.

In proposed paper were presented the basic necessary principles how to realize and to modify existing digital robust control algorithms. The option of co-simulation can be useful to accelerate simulation of advanced control algorithms. In results comparison of control simulation and hardware realization on DC motor were obtained following facts. The closed control loop in simulation offered higher quality, i.e. lower overshoot and shorter control time. One of the reasons of this difference could be non-accurate process identification by acceptance of the first order.

## Acknowledgment

This work was supported by the Scientific Grants APVV 0772-12 and KEGA 030STU-4/2015.

## References

- Ackermann, J., 1993. “Robust Control” Systems with Uncertain Physical Parameters. Springer-Verlag, London, UK.
- Bishop, D., 2006. Fixed Point Package User’s Guide. <http://www.vhdl.org>.
- Cigánek, J., Kozák, Š., 2010. Robust controller design techniques for unstable systems. In: Int. Conf. Cybernetics and Informatics, Vyšná Boca, Slovak Republic.
- Diaz-Barrero, J.L., Egozcue, J.J., 2004. Characterization of polynomials using reflection coefficients. Appl. Math. E-Notes 4, 114–121.
- Kay, S.M., 1988. Modern Spectral Estimation. Prentice Hall, New Jersey.
- Keel, L.H., Bhattachayya, S.P., 1999. A linear programming approach to controller design. Automatica 35, 1717–1724.
- Kocúr, M., 2013. HW realizácia PID algoritmov na báze FPGA štruktúr. Slovak University of Technology in Bratislava, Bratislava.
- Kozák, Š., 2002. Development of control engineering methods and their applications in industry. In: 5th Int. Scientific-Technical Conference Process Control 2002, Kouty nad Desnou, Czech Republic.
- Nurges, Ü., 2005. New stability conditions via reflection coefficients of polynomials. IEEE Trans. Autom. Control 50 (9), 1354–1360.
- Nurges, Ü., 2006. Robust pole assignment via reflection coefficients of polynomials. Automatica 42 (7), 1223–1230.
- Oppenheim, A.M., Schaffer, R.W., 1989. Discrete-Time Signal Processing. Prentice-Hall, Englewood Cliffs.
- Picinbono, B., Bendir, M., 1986. Some properties of lattice autoregressive filters. IEEE Trans. Acoust. Speech Signal Process. 34, 342–349.
- Viswanathan, V., 2005. Embedded Control Using FPGA. Indian Institute of Technology, Bombay.
- Xilinx, 2012. SP601 Hardware User Guide.