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The surface texturing of monocrystalline silicon with NH_4OH and ion implantation for applications in solar cells compatible with CMOS technology

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Abstract

This work presents the development of photovoltaic cells based on p+/n junction in Si substrates, aimed at compatibility with fabrication processes with CMOS technology. The compatible processes, which are developed in this study, are the techniques: i) Si surface texturing, with the textured surface reflection of 15% obtained by the formation of micro-pyramids (heights between 3 and 7 μm) using NH_4OH (ammonium hydroxide) alkaline solution, which is free of undesirable contamination by Na^+ and K^+ ions, when NaOH and KOH traditional solutions are used, respectively, and ii) of the ECR-CVD (Electron Cyclotron Resonance - Chemical Vapor Deposition) deposition of SiN_x (silicon nitride) anti-reflective coating (ARC), which is carried out at room temperature and can be performed after the end of cell fabrication without damage on metallic tracks and without variation of p+/n junction depth. The ARC coating characterization presented that the silicon nitride has a refractive index of 1.92 and a minimum reflectance of 1.03%, which is an excellent result for application in solar (or photovoltaic) cells. For the formation of the pn junction was used ion implantation process with $^{11}B^+$, E=20 KeV, dose of $1x10^{15}$ cm^2 and four rotations of 90º to get uniformity on texturized surfaces.

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1. Introduction

The solar cell efficiency is connected with device fabrication processes, such as silicon surface texturing, which increases the surface absorption area of incident radiation on the cell and, consequently, reduces the substrate reflectance and increase the efficiency [1].

These surfaces are obtained by anisotropic wet etching in KOH and NaOH alkaline solutions. As an advantage, using these alkaline solutions, the <111> planes of silicon substrate with (100) crystallographic orientation are exposed, resulting in groups of pyramid on silicon surface[2,3,4]. The pyramids induce many reflections and scatterings of the incident radiation, which increase the light absorption on the surface. This effect is defined as light trapping. The disadvantage of these solutions are K^+ and Na^+ ions from KOH and NaOH, which are mobile charges in Metal-Oxide-Silicon structures. Thus, these solutions are not compatible for CMOS technology, which is used for integration circuits and devices on silicon surface.

In this work, the silicon substrate texturing is carried out by an anisotropic wet etching, with an alkaline solution based on NH_4OH, because this solution can form pyramids on the surface, does not release alkaline products/reagents on the silicon surface and is viable with CMOS technology[5]. Another alternative for surface texturing is use TMAH (tetramethyl ammonium hydroxide $(CH_3)_4NOH$) solution, but this option was ruled out due to its high cost.

With the NH_4OH (concentration of 9% wt and four magnetic stirring velocities) the <111> planes of silicon substrate with (100) crystallographic orientation are exposed and theses planes can form some pyramids on surface. SEM (Scanning Electron Microscopy) analysis presents that these pyramids are observed randomly on the surface, indicating that the wet etching was all long on the substrate. Furthermore, the pyramid height values are between 3.5 and 7.2 μm, and the silicon etching wet rate was about of 0.7 μm/minute. The reflectance measurements show that the surfaces with and without texturing present reflectance values of about 16% and 38%, respectively. This result indicated that our texturing process based on NH_4OH can be used to fabricate Si-based solar cells. Photovoltaic cells were fabricated, using the NH_4OH solution texturing and the silicon nitride antireflective coating by ECR (Electron Cyclotron Resonance), which is carried out at room temperature and can be performed after the end of cell fabrication without damage on metallic tracks and without variation of junction depth [6]. The ARC coating characterization presented that the silicon nitride has a refractive index of 1.92 and a minimum reflectance of 1.03%, which is an excellent result for application in solar cells. For the formation of the pn junction was used ion implantation process with 11 B^+ , E=20 KeV, dose of $5x10^{15}$ cm^2 and four rotations of 90º to get uniformity on texturized surfaces.

2. Experimental Procedure

In this work, p-type Si (100) wafers were used. The samples were cleaned by standard RCA method. After the cleaning process, the samples were immersed in a reactor with a solution based on NH_4OH to perform the silicon surface texturing during 30 minutes. The solution temperature was between 75 and 85°C. These temperature values were measured by a thermometer. Four processes were carried out with different magnetic stirring speed. After the process, SEM (Scanning Electron Microscopy) analysis was used to verify the pyramid formation. Light reflection/absorption on the silicon surfaces with and without texturing process was measured by reflectance method with wave length between 300 and 800 nm. The thickness values of silicon substrates before and after the texturing process were measured using a micrometer. The etching silicon rate for NH_4OH solution was extracted by the ratio between the thickness values and the process time, which was fixed at 30 minutes. After the texturing process, the surface roughness was measured using a scan profiler.

Ion implantation was carried out with $^{11}B^+$ (20 KeV and dose of $1x10^{15}$ cm^2), with four rotations of 90º to get uniformity on texturized surfaces. The goal of the first implantation is p^+/n junction formation. A second ion implantation was carried out in the back side of the samples, with $^{31}P^+$ (50 KeV and dose of $1x10^{15}$ cm^2), for n^+ ohmic contact formation. After this steps, the wafers were cleaned by standard RCA method and annealed for 180 seconds, in N_2 environment and at 1000º C for the front side, and for 60 seconds, in N_2 environment and at 1000º C for back side, to active the dopants.

SiN_x anti-reflective coating (ARC) was deposited by ECR – CVD (Electron Cyclotron Resonance – Chemical

Vapor Deposition), using 2.5 sccm N_2, 5 sccm Ar and 125 sccm SiH_4 flow ratio. The substrate temperature, process pressure, 2.45 GHz ECR power and 13.56 MHz RF power were fixed at 20ºC, 3mTorr, 250 W and 0 W, respectively.

Formation of both electrodes were performed by Magnetron Sputtering, using Ti (20 nm) and Al (1 µm) layers for upper electrode and Al (1 µm) for substrate electrode. Sintering process was carried out in conventional furnace, at 450º C for 10 minutes with forming gas environment.

3. Results and Discussion

Four samples with different magnetic stirring velocities in NH_4OH solution were processed. Using a micrometer for the silicon substrate thickness measurements before and after the texturing processes, the etching rates were extracted and for four samples were about 0.7 µm per minute. Table 1 present the mean roughness and standard deviation values of those four samples, after the texturing process in related to solution stirring velocity. The surface roughness values were measured using a scan profiler. It was observed that: sample mean roughness values are reduced when solution stirring velocity is increased, indicating that with higher solution stirring velocity, the etching reagent has higher mobility on surface, reducing the micro-masking effect and, consequently, the surface roughness. Furthermore, higher solution mobility on surface can lead to a pyramid distribution all along the silicon surface.

Table 1: Surface roughness values

Sample	Solution stirring velocity	Roughness (nm)
Sample1		1000 ± 200
Sample 2		800 ±100
Sample 3	↓ Velocity is increased	650 ±150
Sample 4		640 ±70

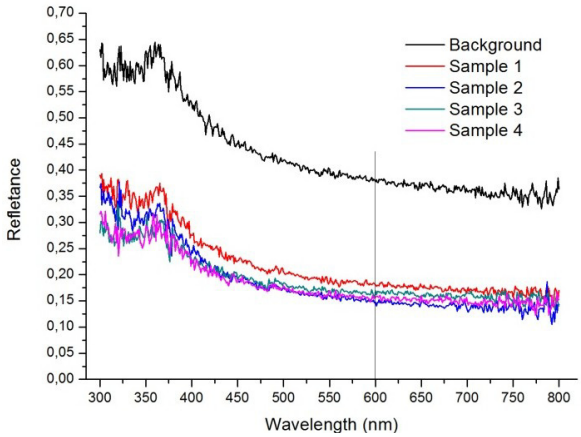

Fig. 1: *Curve of light reflection on the silicon surfaces with and without (background) texturing process versus wavelength.*

Figure 1 presents light reflection on the silicon surfaces with and without (background) texturing process, which was measured by reflectance method with wavelength between 300 and 800 nm. Reference 1 presented that the photons solar intensity is maximum with wavelength nearby 600 nm and the solar cell efficiency was increased with a decrease on reflectance for this wavelength. So, in Figure 1, the reflectance values were extracted to wavelength at 600 nm. The reflectance of background sample was about 37.8%. Samples with texturing surface process exhibited reflectance between 14.7% and 18.1%. For the sample 4, which presented the best pyramid uniform distribution on silicon surface, the reflectance value was 15.7%. These reflectance values are very similar

to obtained in the reference [8], but the used texturing. Therefore, the silicon surface texturing process using NH4OH solution presents a pyramid uniform distribution on silicon surface with reflectance of about 16%, which can increase the solar cell efficiency.

This is confirmed by SEM results in the Figures 2 (a) and (b), respectively, which present an overview and the pyramid details, such as pyramid height values, on silicon surface of sample 4. It was observed that: in (a), a pyramid distribution all along the silicon surface occurs. In (b), the pyramid height values are between 3.5 and 7.2 μm and a substantial portion of the wafer surface is covered with very small pyramids. One way of decrease the amount of these very small pyramids would be the deposition of a thin layer of silicon oxide and use of a mask for determine the uniformity these structures.

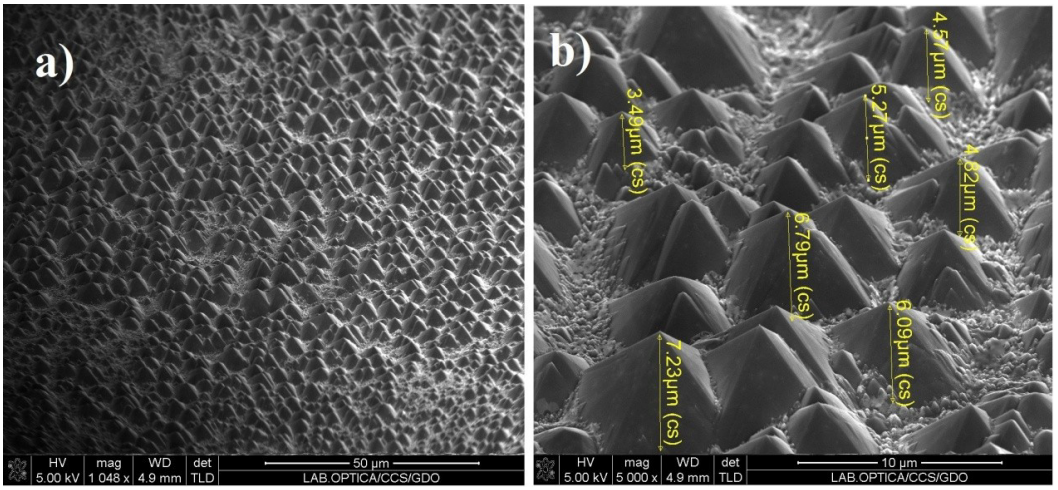

Fig. 2: a) *SEM analysis presents the pyramid formation,b) overview and the pyramid details, such as pyramid height values, on silicon surface of sample 4. All pictures were obtained by electron beam of FIB system.*

Using equation $\lambda/4 = n_1 d_1$ and the value of the refractive index of 1.9 for silicon nitride [1], enabled determine the thickness of ARC, which should be around 75 nm for minimizing the refection wavelength at around 600 nm (maximum incidence of the radiation photons to AM 1.5 [1,9]). Physical thickness of 76 nm and refractive index of 1.92 were determined by ellipsometry measurement. Figure 3 shows the reflectance spectra in the range between 300 and 1200 nm of silicon surfaces for three different thicknesses of silicon nitride and one sample without film, used as background.

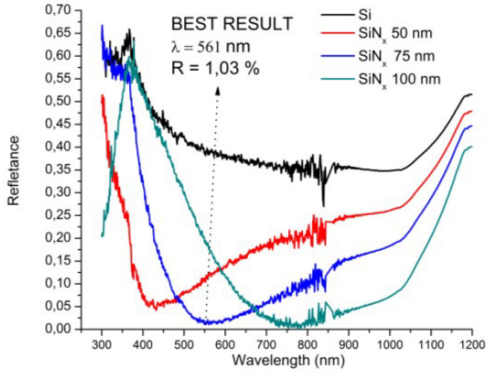

Fig. 3: *Curve of light reflection on the silicon surfaces with and without (background) anti-reflective coating versus wavelength.*

To analyze the efficiency and power of solar cells devices were extracted curves of current – voltage (I-V) using a solar simulator. The system consists of a tungsten-halogen lamp, a current source and an exhaust system. Contact is made by electrodes and a source KEITLHEY 2602 is responsible for generating a voltage signal (polarization). The electrical parameters were extracted and analyzed by software developed at Wolfram Mathematica. In Figura 4 are shown the I-V curves of cells with and without texturing. The measurements were made with spectrum AM 1.5 and in the dark, and the parameters obtained were: short circuit current (I_{SC}), open circuit voltage (V_{OC}), fill factor (FF) and efficiency (E_{ff}). The sample without texturing has an area four times smaller than the textured sample. Comparing the data obtained, it was observed that the cell without texturing presented better results because their V_{OC} is 14% higher and the I_{SC} showed almost the same value in both cases. The textured sample showed a lower efficiency for problems in ion implantation and contact resistance.

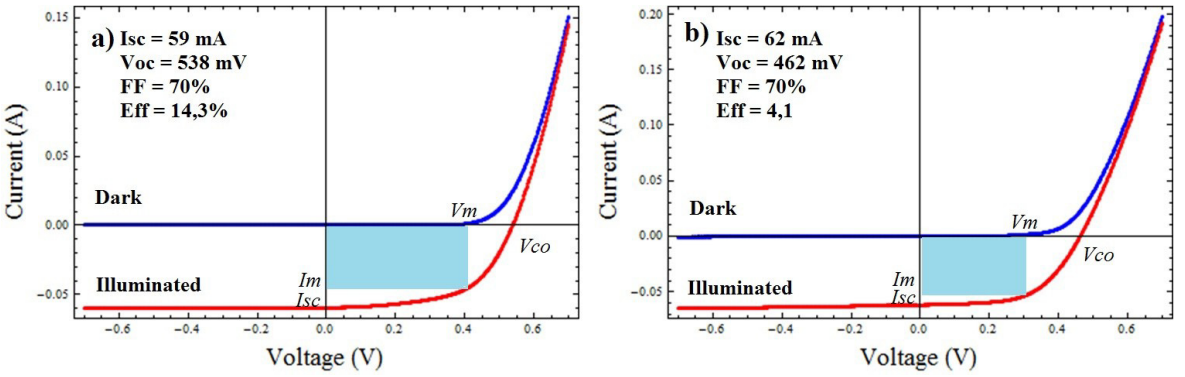

Fig. 4: Curves of current – voltage (I-V) using a solar simulator, a)Solar cell without texturing process, b) Solar cell with texturing process.

4. Conclusions

The results of texturing surface process using NH_4OH were presented in this work. This fact enables the integration and fabrication on the same layer solar cells and MOS devices. The most important results are from SEM analysis and reflectance measurements that indicated that the silicon surface texturing process using NH_4OH solution presents a pyramidal distribution all along the silicon surface, with reflectance of about 16%. The texturing process can be improved using a thin layer of silicon oxide and a mask to define the pyramids regions.

The low efficiency and Vco values lower than 5% and 500 mV, respectively, for solar cells fabricated with texturing process can be due to the non conformal electrode deposition on texturized surface. Thus, the diode series resistance is increased and Vco is reduced. The efficiency of the solar cells, with or without textured surface, can be improved by increasing the implanted dose to $1x10^{16}$ cm^2, which can reduce the series resistance.

Acknowledgements

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