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Extensions of Asynchronous Circuits and the Delay Problem. Part II: Spike-Free Extensions and the Delay Problem of the Second Kind*

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In Part I of this paper, a larger asynchronous circuit was regarded as successfully simulating a smaller one if the former was a "good extension" of the latter, and the adverse effects of the delays on the inter-element wires, i.e., the delay problem, was investigated from this viewpoint. A closer examination made here, however, reveals that a good extension is usually insufficient for a truly successful simulation, and that a larger circuit must be "spike-free" in addition to being good. Accordingly, the delay problem is reinvestigated from this new viewpoint. Also, some relationships are established between good and spike-free extensions. An important result is that a spike-free delay network incorporation having binary wires only is a good extension. Further it is shown that the mathematical situation can be greatly simplified by additionally requiring that the extension be semimodular.

OPENING REMARKS

As a continuation to Part I, this part begins with Section 9, in which we return to the following question: "What is the condition which a larger circuit must satisfy in order successfully to simulate a smaller one?" The answer given in Section 2 of Part I was that the larger circuit must be a good extension. However, this previous view is rather naive; Sometimes more may be required in connection with semimodularity, a property well-known as desirable in asynchronous circuits [2, 4]. Accordingly, the answer is revised in Section 9 by additionally requiring that the larger circuit be *spike-free*. Then in Section 10, some relationships are established between good and spike-free extensions. In particular, it is shown that a delay network incorporation having binary wires only is a good extension whenever it is spike-free.

* Part I of this paper subtitled "Good Extensions and the Delay Problem of the First Kind" appears in *J. Comput. System Sci.* 2 (1968), 251–287. References [1–7] are identical to those cited in Part I, while [8–10] are new. Footnotes 1–4 of Part I are cited in some places here. For this reason those to this Part II are numbered 5–12. Similarly, the figures here are Figs. 8–13.

In Part I, Section 5, we introduced the delay problem of the first kind as an adaptation of the concept of good extensions to the delay problem [1]. Similarly, the delay problem of the second kind is introduced in Section 11 as an adaptation of the concept of spike-free extensions, and a reduction theorem similar to, but stronger than, Theorem (7 : 7) is given.

The concept of spike-free extensions is, so to speak, the known semimodularity as restricted to the ordinary nodes, and is weaker as a condition than the latter. A larger circuit need not be semimodular for successful simulation. Semimodular extensions, however, have the merit of symplifying the theoretical situations. This point will be the subject of Section 12, in which the delay problem of the third kind is introduced. Examples are given in Section 13 for various kinds of the delay problems. Section 14 gives concluding remarks. In addition, Appendices A, B, and C give corrections to, an alphabetical index of terms introduced in, and an index for symbols used in Part I, respectively.

This Part II assumes familiarity with Sections 0–5 of Part I. Sections 6 and 7 are required only in the latter half of Section 11, and partly in Section 13.

Abbreviations. In the sequel, the following abbreviations will be used: we write

DNI for "delay network incorporation",

QNI for "quiescent natural extension", and

DPn for "the delay problem of the n-th kind".

Here, $0 \leqslant n \leqslant 3$. Except for DP2 and DP3, which will be introduced subsequently, the locations where these terms are defined in Part I may be looked up in Appendix B.

9. Semimodularity and Spike-Free Extensions

A circuit C is said to be *partially semimodular* with respect to an initial state u and a node i, or briefly psm $[u, i]$, whenever for each pair of states a and b of C, if $uFaRb$, then bR_ia', i.e., either $a_i' = b_i$ or $a_i' = b_i'$. Intuitively, this implies that, if the circuit C is started at u, and once i is excited, the excitation neither terminates nor changes its target value until a corresponding change of the signal value z_i actually occurs. In fact, the following is immediate from the definition: If C is psm$[u, i]$, and if $uFa(0)Ra(1)\, R \cdots Ra(\ell)$ and $a(0)_i = a(1)_i = \cdots = a(\ell)_i$, then either $a(0)_i' = a(0)_i$ or $a(0)_i' = a(\ell)_i'$. C is said to be (*totally*) *semimodular* with respect to its state u, or sm$[u]$, whenever it is psm$[u, i]$ for all nodes i of C.

Semimodularity was first introduced as a sufficient condition for a circuit to have a desirable property called *speed-independence* [2, 4]. However, there is another point making this concept important.[5] The mathematical model of Muller's theory of

[5] The reader may skip to Definition (9:1) if he accepts it as it is.

asynchronous circuits is based on the assumption that the instantaneous combination z of the signal values z_i uniquely determines the implied signal values z_i'. In particular, if an implied signal value changes due to some changes of signal values at other nodes, the earlier implied value must be completely "forgotten," so that no latent effect can exist. Latent effects do exist, however, in physically realized circuits.

For example consider a transistorized inverter which is in a quiescent condition with its input and output being 0 and 1. Suppose that the input is changed to 1. Various stray capacitances in the circuit must be charged first for the transistor to be brought to the active region of its operational characteristics, so that there is a delay time before a transition of the output from 1 to 0 actually starts. Now return the input from 1 to 0 just before the transition is completed. Then, the half-switched output will return to 1 leaving a spike. See Fig. 8(a) for a waveform diagram drawn more or less realistically. On the other hand, the situation assumed in Muller's theory of asynchronous circuits is somewhat as shown in Fig. 8(b), where no spikes as above are expected. It is quite conceivable that a circuit designed according to the theory may operate incorrectly due to such an unexpected spike.

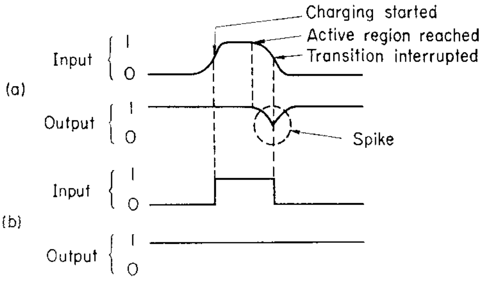

FIG. 8. The significance of (partial) semimodularity: (a) actual voltage changes at an inverter; (b) the logical model.

(Partial) semimodularity removes the difficulty. If a circuit C is psm$[u, i]$, no spikes as described above will appear at the output of the logical element corresponding to i in a physical realization of C since the implied signal value at i remains constant during every excitation. (Of course, we assume that the circuit is started at u.) Thus, (partial) semimodularity often has the vital significance of assuring the adequacy of the model of the asynchronous circuit theory.

In Part I, an extension was considered as successfully simulating its original if it was a good extension. The above discussion reveals that, for most types of the logical elements used, the success would be imperfect if partial semimodularity with respect to some of the ordinary nodes is not preserved in forming the extension. Accordingly, we define:

DEFINITION (9 : 1). An extension C^* of a circuit C is said to be *spike-free* with respect to its state u^* whenever it is psm$[u^*, i]$ for all its ordinary nodes i.[6]

Total semimodularity of C^* is not required. Our position in this definition is supported by the following "behind the wall" argument. Consider a good extension C^* of a circuit C. As in Section 3, suppose that, in a physical realization of C^*, those circuit points corresponding to the hidden nodes are inaccessible for an observer. If the ideal of Fig. 8(b) applies, the physical realization would be indistinguishable for him from a circuit realizing C. If, on the other hand, the situation is as in Fig. 8(a), he may find out the difference by detecting the spikes using, say, an oscilloscope. To make him unsuccessful, it is sufficient for C^* to be spike-free. Partial semimodularity with respect to the hidden nodes is superfluous.

The reader is warned at this point that not for all areas of possible application of our theory the above argument is appropriate. Thus, in the first four paragraphs of Part I, Section 0, we mentioned three problems concerning the physical realization of mathematically defined asynchronous circuits. They were: (1) the delay problem, (2) the problem of signal levels, and (3) the problem of function realization. Of these, the observation of the preceding paragraph is adequate to the first two, but not to the third. We shall discuss this point in more detail in Section 13, and until then, will not consider the problem of function realization.

In closing this section we shall present one small result which in effect states that a spike-free extension comes into play only when the original circuit is semimodular. Thus,

PROPOSITION (9 : 2). *Let an extension C^* of a circuit C be statically good with respect to its state u^*. If C^* is* psm$[u^*, i]$ *for a node i of C, then C is* psm$[u, i]$, *where* $u = \text{rest}(u^*, C^*, C)$.

Proof. Let a and b be states of C satisfying $uFaRb$. By the assumption that C^* is statically good, we may pick a^* of ext(a, C, C^*) and c^* of ext(a', C, C^*) in such a way that $u^*Fa^*Rc^*$. Let b^* be that member of ext(b, C, C^*) satisfying $b_j^* = a_j^*$ for all

[6] The concept of spike-free extension should not be confused with that of hazard-free combinatorial network as discussed, e.g., in Miller's book [2, Chap. 9]. In fact, a brief explanation of the latter concept is as follows: Consider a level-type combinatorial network having one output and several inputs. For a given combination of the input signals wait for a sufficiently long time to bring the network to an equilibrium. Then change the signal at one of the inputs. Perhaps after a series of moves or signal changes at the logical elements composing the network, another equilibrium will be reached. During the transition we hope that the output signal should either remain constant, or change once for all from an earlier to a new value. The network is said to be *hazard-free* if this is actually the case. Apparently, this latter concept is related to that of good, rather than spike-free, extension. For, the switching considered in the above is a full switching, and is not a half-switching as shown in Fig. 8(a).

hidden nodes j of C^*. Then a^*Rb^*. For, we must only consider the ordinary nodes. Let k be ordinary. Then by the construction,

1° $a_k{}^* = a_k$,

2° $b_k{}^* = b_k$,

and

3° $c_k{}^* = a_k{}'$.

But by aRb,

4° b_k equals a_k or $a_k{}'$,

and by a^*Rc^*,

5° $c_k{}^*$ equals $a_k{}^*$ or $a_k^{*\prime}$.

Combining 1°, 2° and 4°, we get

6° $b_k{}^*$ equals $a_k{}^*$ or $a_k{}'$.

On the other hand, by 3° and 5°,

7° $a_k{}'$ equals $a_k{}^*$ or $a_k^{*\prime}$,

and from 6° and 7° we conclude that $b_k{}^*$ equals $a_k{}^*$ or $a_k^{*\prime}$. Hence, a^*Rb^*.

Still continuing with an ordinary k, another consequence of 6° and 7° is that

8° $a_k{}'$ equals $b_k{}^*$ or $a_k^{*\prime}$.

(For, if $a_k{}' \neq a_k^{*\prime}$, then by 7°, $a_k{}' = a_k{}^*$. Hence by 6°, $b_k{}^* = a_k{}'$.) But by partial semimodularity of C^*, and by a^*Rb^* just proved,

9° $a_i^{*\prime}$ equals $b_i{}^*$ or $b_i^{*\prime}$

for the specified i. Putting $k = i$, we combine 8° and 9° to get

10° $a_i{}'$ equals $b_i{}^*$ or $b_i^{*\prime}$.

Finally by (1) of Theorem (2 : 3), which holds whenever C^* is contained statically within C with respect to u^*, which is the case here by our assumption, we have

11° $b_i^{*\prime}$ equals b_i or $b_i{}'$,

and by 2°, 10°, and 11°, $a_i{}'$ must equal b_i or $b_i{}'$, which was to be proved. Q.E.D.

10. The Relationships between Spike-Free and Good Extensions

In addition to being desirable in themselves, spike-free extensions have the merit of being checked easily as to whether they are good or bad. This point will now be discussed.

In the rest of this paper we consider quasi-regular extensions only (see Section 3). To recapitulate, an extension C^* of a circuit C is said to be *quasi-regular* with respect to its state u^* whenever for each state a^* of C^* such that u^*Fa^*, there is a QNE b^* from C onto C^* of a-rest(a^*, C^*, C) satisfying $a^*F_{T^*}b^*$, where $T^* = \text{ext}(a, C, C^*)$. As in Definition (1 : 1), $a^*F_{T^*}b^*$ means that there is an R-sequence $a^* = a^*(0)$, $a^*(1),\ldots, a^*(\ell) = b^*$ of C^* such that $a^*(h) \in T^*$ for $0 \leqslant h \leqslant \ell$. We shall call such an R-sequence a *resolving sequence* of a^*.

LEMMA (10 : 1). *If an extension C^* of a circuit C is quasi-regular and spike-free both with respect to its state u^*, then it is statically good with respect to u^*.*

Proof. Let a^* be any state of C^* such that u^*Fa^*, and i a node of C. Construct a resolving sequence $a^* = a^*(0)$, $a^*(1),\ldots, a^*(\ell) = b^*$ of a^*. Since $a^*(0)_i = a^*(1)_i = \cdots = a^*(\ell)_i$, we have either $a_i^{*\prime} = a_i^*$ or $a_i^{*\prime} = b_i^{*\prime}$ by the partial semimodularity. As usual write $a = \text{rest}(a^*, C^*, C)$. Then $a_i^* = a_i$ and, since b^* is a QNE of a, $b_i^{*\prime} = a_i'$. Therefore, $a_i^{*\prime}$ must equal either a_i or a_i'. That is, (1) of Theorem (2 : 3) holds. Hence, C^* is contained statically within C with respect to u^*. On the other hand, C^* wipes over C with respect to u^* by Theorem (3 : 4), since it is quasi-regular. Hence, we have the lemma. Q.E.D.

In spite of the above result, some quasi-regular extensions are spike-free and yet *dynamically* bad. Something more than quasi-regularity is required for assuring full goodness. On additional condition serving this purpose is total semimodularity of the extension.

THEOREM (10 : 2). *If an extension C^* of a circuit C is quasi-regular and semimodular both with respect to a state u^* of C^*, then it is a good extension of C with respect to u^*.*

Proof. By Theorems (2 : 3), (3 : 4), and Lemma (10 : 1), it suffices if we derive a contradiction from the assumption that there is a stable loop T^* of C^* such that u^*FT^*, and $T = \text{rest}(T^*, C^*, C)$ is a loop but not stable. Under this assumption there is a node j of C such that a_j and a_j' are constant over $a \in T$, and yet the constant values differ. Write γ and γ' for these constant values of a_j and a_j'.

We first note that T^* *cannot contain a state x^* which is a natural extension of* $x = \text{rest}(x^*, C^*, C)$. For assuming the contrary, let such an x^* be in T^*. Then for any y^* of T^*, $x^*F_{T^*}y^*$ since T^* is a loop. That is, there is an R-sequence $x^* = x^*(0)$, $x^*(1),\ldots, x^*(L) = y^*$ such that $x^*(h) \in T^*$ for $0 \leqslant h \leqslant L$. Since u^*Fx^*, and since $x_j^* = x^*(0)_j = \cdots = x^*(L)_j = y_j^*(=\gamma)$, we may use the partial semimodularity of C^* to conclude that $x_j^{*\prime}$ equals either $y_j^{*\prime}$ or y_j^*. But $x_j^{*\prime} = x_j' = \gamma'$, since x^* is a natural extension. Also, $y_j^* = \gamma \neq \gamma'$. Therefore, $x_j^{*\prime} = y_j^*$ is impossible, so that we must have $x_j^{*\prime} = y_j^{*\prime}$. In other words, $y_j^{*\prime}$ is constant over $y^* \in T^*$, and equals γ'. But y_j^* is also constant over $y^* \in T^*$, and equals γ. Since $\gamma \neq \gamma'$, from this we conclude that T^* is not stable, which is a contradiction.

Now for $z^* \in T^*$, let one of the shortest resolving sequences of z^* be $z^* = z^*(0)$, $z^*(1),\ldots, z^*(\lambda)$, and write $\ell(z^*)$ for the λ of this particular sequence. Let $\ell(T^*)$ be the smallest of the $\ell(z^*)$ of $z^* \in T^*$. Although in some cases T^* may be chosen in a number of different ways, *we may assume that we have chosen a T^* which has the smallest possible $\ell(T^*)$*. Note that $\ell(T^*) > 0$. (For, if $\ell(T^*) = 0$, then for some $a^* \in T^*$, $\ell(a^*) = 0$. This a^* alone constitutes its resolving sequence. Hence, a^* itself must be a QNE of its restriction from C^* onto C. But this contradicts the result of the preceding paragraph since a QNE is a quiescent *natural* extension.)

Pick an element a^* of T^* such that $\ell(a^*) = \ell(T^*)$. It makes sense to consider the second member b^* of a resolving sequence of a^* since $\ell(a^*) > 0$ by the above. Construct a closed R-sequence $a^* = a^*(0)$, $a^*(1),\ldots, a^*(\ell) = a^*$ consisting only of the members of T^* and including each of them at least once. This exists since T^* is a loop. Also construct $b^*(0)$, $b^*(1),\ldots, b^*(\ell)$ by the following: Put $b^*(0) = b^*$. For $0 \leqslant h < \ell$ and for the nodes i of C^*, put

$$\begin{aligned} b^*(h+1)_i &= a^*(h)_i\,, &&\text{if } \ a^*(h)_i = b^*(h)_i = a^*(h+1)_i\,,\\ &= a^*(h)'_i\,, &&\text{otherwise.}\end{aligned}$$

From the semimodularity of C^* it follows[7] that $b^*(0)Rb^*(1)\,R \cdots Rb^*(\ell)$ and, for $0 \leqslant h \leqslant \ell$, $a^*(h)\,Rb^*(h)$.

Assume for contradiction that $a^*(\ell) \neq b^*(\ell)$. Then by the construction, there must be some node i of C^* such that $a^*(h)_i \neq b^*(h)_i = a^*(h)'_i$ over $0 \leqslant h \leqslant \ell$. Also by the construction, $b^*(0)_i = b^*(1)_i = \cdots = b^*(\ell)_i$ so that $a^*(0)'_i = a^*(1)'_i = \cdots = a^*(\ell)'_i$. Since the sequence $a^*(0)$, $a^*(1),\ldots, a^*(\ell)$ contains all the states of T^*, by Lemma (1 : 3) we have $a^*(0)_i = a^*(0)'_i$, a contradiction. Hence, $a^*(\ell) = b^*(\ell)$.

Adjoining $b^*(0)$, $b^*(1),\ldots, b^*(\ell) = a^*(\ell)$ to T^*, we obtain another loop U^* of C^*. Since $T^* \subseteq U^*$, U^* is stable, and u^*FT^*. Moreover, $T = \text{rest}(U^*, C^*, C)$ since, for all ordinary nodes i of C^* and for $0 \leqslant h \leqslant \ell$, $a^*(h)_i = b^*(h)_i$ follows from $a_i^* = b_i^*$ by the construction. (Note that $a_i^* = b_i^*$ must hold since a^* and b^* are two members of a resolving sequence.) Thus, U^* satisfies all the requirements for T^* except for the minimality of $\ell(T^*)$. But $\ell(U^*) \leqslant \ell(T^*) - 1$ since $b^* \in U^*$, and since a resolving sequence of b^* may be obtained by removing the first member a^* from the resolving sequence of a^*, contradicting the initial choice of T^*. Q.E.D.

Among quasi-regular extensions, DNI's with binary wires are particularly important. We shall now derive full goodness from spike-freeness for this special case. One easy lemma is in order.

LEMMA (10 : 3). *Let C^* be a* DNI *of a circuit C, and ΔA a set of its hidden delay nodes. Then,*

[7] See Theorem 10 of Ref. [4] if necessary.

(1) *For each state x^* of C^*, there is a state y^*(ofC^*) such that*$y_i^{*\prime} = y_i^*$ *for* $i \in \Delta A$, *and* $y_i^* = x_i^*$ *for* $i \notin \Delta A$;

(2) *There is an R-sequence* $x^* = z^*(0),\ z^*(1), \ldots, z^*(\lambda) = y^*$ *such that* $z^*(h)_i = x_i^*$ *holds for* $0 \leqslant h \leqslant \lambda$ *if* $i \notin \Delta A$;

(3) y^* *is uniquely determined by specifying* x_i^* *for all* i, $i \notin \Delta A$.

Proof.[8] For $i \in \Delta A$, let $\pi(i)$ be the longest delay path lying within ΔA and having i as its terminal node. As in the proof of Lemma (4 : 2), write $\alpha(i)$ and $p(i)$ for the length and the parent node of $\pi(i)$. $\alpha(i)$ is bounded by an integer λ: $\alpha(i) \leqslant \lambda$. For $0 \leqslant h \leqslant \lambda$, define $z^*(h)$ by putting

$$\begin{aligned} z^*(h)_i &= x^*_{p(i)}, \quad \text{if} \quad i \in \Delta A \quad \text{and} \quad \alpha(i) \leqslant h, \\ &= x_i^*, \quad \text{otherwise.} \end{aligned}$$

Let $i \in \Delta A$ and $\alpha(i) \leqslant h$. Then $z^*(h)_i = z^*(h)'_i$. In fact, let j be the parent node of i. If $j \notin \Delta A$, then we have $p(i) = j$. If $j \in \Delta A$, then $\alpha(j) < h$ and $p(i) = p(j)$. In the former case, $z^*(h)_i = x^*_{p(i)} = x_j^* = z^*(h)_j = z^*(h)'_i$, while in the latter, $z^*(h)_i = x^*_{p(i)} = x^*_{p(j)} = z^*(h)_j = z^*(h)'_i$.

Therefore, (1) is satisfied if we put $y^* = z^*(\lambda)$. In fact, if $i \in \Delta A$, then $y_i^* = z^*(\lambda)_i = z^*(\lambda)'_i = y_i^{*\prime}$, while if $i \notin \Delta A$, then $y_i^* = x_i^*$ by the construction. To show (2), we wish to prove that $z^*(h-1)\, R z^*(h)$ for $h > 0$. Consider the R_i-relations. If $z^*(h-1)_i = z^*(h)_i$, then there is nothing to prove. But if $z^*(h-1)_i \neq z^*(h)_i$, then $i \in \Delta A$ and $\alpha(i) = h$. Again let j be the parent node of i. Then, $z^*(h)_i = z^*(h)'_i = z^*(h)_j = z^*(h-1)_j = z^*(h-1)'_i$, implying the desired relation. (The first equality follows from the preceding paragraph, and the third follows by noting that, if $j \in \Delta A$, then $\alpha(j) < \alpha(i) = h$, and so $z^*(h)_j = x^*_{p(j)} = z^*(h-1)_j$, but if $j \notin \Delta A$, then $z^*(h)_j = x_j^* = z^*(h-1)_j$.) Now, by the construction, $z^*(0) = x^*$, and $z^*(h)_i = x_i^*$ for $i \notin \Delta A$ over $0 \leqslant h \leqslant \lambda$. Hence, (2) of the lemma is also true.

To prove (3), let y^* be a state as specified in (1). Then by an induction over $\alpha(i)$, it follows that $y_i^* = x^*_{p(i)}$ for $i \in \Delta A$, and therefore y^* is unique. (The easy details are left to the reader.) Q.E.D.

THEOREM (10 : 4). *Assume that a* DNI C^* *of a circuit* C *has binary wires only,* i.e., *the sets of signal values of the hidden delay nodes have at most two elements. If* C^* *is spike-free with respect to a state* u^*, *then it is a good extension of* C *with respect to* u^*.

Proof. The first two paragraphs of the proof of Theorem (10 : 2) apply here exactly as they stand. Thus, assuming the existence of T^*, we wish to derive a contradiction. As before, T^* cannot contain a natural extension.

[8] The technique used here is essentially identical to that used in the proof of Lemma (6:3) for constructing $\{c(i, j)\}$ from $\{d(i, j)\}$.

As in Theorem (10 : 2), construct a closed R-sequence $a^*(0), a^*(1),..., a^*(\ell) = a^*(0)$ consisting of the members of T^* and including each of them at least once. For $0 \leqslant h \leqslant \ell$, write

$$a(h) = \text{rest}(a^*(h), C^*, C),$$

$$U^* = \bigcup_{0 \leqslant h < \ell} \text{ext}(a(h), C, C^*).$$

Our proof will consist in showing the following:

[A] There is a state c^* (of C^*) which is a natural extension of rest(c^*, C^*, C) such that $a^*(0) F_{U^*} c^* F_{U^*} a^*(0)$.

Once this is done, the desired contradiction follows by the following argument: By the F_{U^*}-relations, there are states $c^*(0),..., c^*(\lambda)$ of U^* such that $a^*(0) = c^*(0) R c^*(1) R \cdots R c^*(\lambda) = a^*(0)$, and $c^*(h) = c^*$ for some h, $0 \leqslant h \leqslant \lambda$. Adjoin $c^*(1),..., c^*(\lambda - 1)$ to T^* to obtain a new set V^*. Then V^* is a loop, and stable since so is T^* and $T^* \subseteq V^*$. Also, $u^* F V^*$. Therefore, we can reselect T^* to be V^*. But V^* contains $c^*(h)$, a natural extension, which contradicts the second paragraph of the proof to Theorem (10 : 2).

Now assign serial numbers $N(i)$ to the hidden delay nodes i of C^* in such a way that $N(i) < N(j)$ whenever i is a delay node of j. (This is always possible by (2) of Definition (4 : 1).) Let the serial numbers start at 1 and involve no jumps, so that $1 \leqslant N(i) \leqslant \Delta n$, where Δn is the total number of the hidden delay nodes.

Let k and h range over $0 \leqslant k \leqslant \Delta n$ and $0 \leqslant h \leqslant \ell$. *This convention will be effective throughout the rest of this proof.* Let ΔA_k be the set of the hidden delay nodes i of C^* satisfying $N(i) \leqslant k$. Use Lemma (10 : 3) for $x^* = a^*(h)$ and $\Delta A = \Delta A_k$ to obtain y^*, which we shall write $a_k{}^*(h)$.[9]

Clearly, $a_0{}^*(h) = a^*(h)$ and $a_k{}^*(\ell) = a_k{}^*(0)$.

Now note that $a^*_{\Delta n}(0)$ is a QNE of its restriction from C^* onto C. For, $\Delta A_{\Delta n}$ includes all the hidden delay nodes of C^*. Hence, by (1) of Lemma (1 : 3), $a^*_{\Delta n}(h)$ must be a quiescent extension, and so by the penultimate paragraph of Section 4, natural. Therefore, to prove [A] it is enough to show that

[B] $a^*(0) F_{U^*} a^*_{\Delta n}(0)$, and

[C] $a^*_{\Delta n}(0) F_{U^*} a^*(0)$.

Now, (2) of Lemma (10 : 3) as applied to $x^* = a^*(h)$ and $\Delta A = \Delta A_k$ reads as follows:

[9] Note that here the subscript k is a parameter, and does not refer to a node of the circuit. We could alternatively write $a^*(k, h)$, but for brevity prefer $a_k{}^*(h)$. The i-component of this state will be denoted by $a_k{}^*(h)_i$.

1° There is an R-sequence of the form $a^*(h) = z^*(0), z^*(1), \ldots, z^*(\lambda) = a_k{}^*(h)$ such that $z^*(0)_i = z^*(1)_i = \cdots = z^*(\lambda)_i$ for $i \notin \Delta A_k$, and in particular for an ordinary i.

But [B] is obtained as a direct consequence of 1° if we put $h = 0$ and $k = \Delta n$. Therefore, all that we must do is to prove [C].

(*Interlude* 1: *Motivating Comments.* $a_k{}^*(h)$ is a version of $a^*(h)$ forced to be quiescent at the members of ΔA_k. As a special case, $a_{\Delta n}^*(h)$ is quiescent at all of the hidden delay nodes. To prove [C], we "revive" the quiescent hidden delay nodes one by one by the following method: We run the circuit along the sequence of states

$$a_{\Delta n}^*(0), a_{\Delta n}^*(1), \ldots, a_{\Delta n}^*(\ell) = a_{\Delta n}^*(0),$$

and attempt to energize the Δn-th hidden delay node with the help of the motion of its parent node. Note that in this case, the parent node must be an ordinary node. This is in a way possible if the delay node is binary, and the circuit is finally led to the lower order sequence

$$a_{\Delta n-1}^*(0), a_{\Delta n-1}^*(1), \ldots, a_{\Delta n-1}^*(\ell) = a_{\Delta n-1}^*(0).$$

We then attempt to energize the $(\Delta n - 1)$-th hidden delay node by running the circuit along this new sequence. Again note that the parent node of the $(\Delta n - 1)$-th hidden delay node is either an ordinary node or the Δn-th node, and hence, is alive. We repeat this process, and are able to reach

$$a_0{}^*(0), a_0{}^*(0), \ldots, a_0{}^*(\ell) = a_0{}^*(0)$$

in Δn steps. Since $a_0{}^*(0) = a^*(0)$, this is what was to be done.)

[C] will follow if we show that

[D] $a_k{}^*(h-1) F_{U^*} a_k{}^*(h)$ if $h > 0$, and

[E] for $k > 0$, there is some $h_k > 0$ such that $a_k{}^*(h_k - 1) F_{U^*} a_{k-1}^*(h_k)$.

In fact, from these we have for $k > 0$,

$$a_k{}^*(0) F_{U^*} a_k{}^*(1) F_{U^*} \cdots F_{U^*} a_k{}^*(h_k - 1) F_{U^*} a_{k-1}^*(h_k)$$
$$F_{U^*} a_{k-1}^*(h_k + 1) F_{U^*} \cdots F_{U^*} a_{k-1}^*(\ell) = a_{k-1}^*(0).$$

Repeatedly using this we get

$$a_{\Delta n}^*(0) F_{U^*} a_{\Delta n-1}^*(0) F_{U^*} \cdots F_{U^*} a_0{}^*(0) = a^*(0),$$

which is to be proved.

(*Interlude* 2: [D], in effect, states that the circuit can be driven along the state sequence

$$a_k^*(0), a_k^*(1), \ldots, a_k^*(\ell) = a_k^*(0).$$

[E] means that it is possible for the circuit to enter the lower order sequence at some point h_k.)

Proof of [D]. Define a state $b_k^*(h)$ of C^* for $h > 0$ by putting

$$\begin{aligned} b_k^*(h)_i &= a_k^*(h-1)_i\,, \qquad \text{if} \quad i \in \Delta A_k\,, \\ &= a^*(h)_i\,, \qquad \text{if} \quad i \notin \Delta A_k\,. \end{aligned}$$

(*Interlude* 3: $b_k^*(h)$ is a state which would be obtained if we, in an attempt to reach $a_k^*(h)$ from $a_k^*(h-1)$, change the signal values only at the ordinary nodes and at the hidden delay nodes whose serial number is greater than k.) Now note that

2° for a state x^* of C^*, if $x_i^* = a^*(h)_i$ for $i \notin \Delta A_k$, then $x^* F_{U^*} a_k^*(h)_i$.

In fact, the y^* obtained by using Lemma (10 : 3) for this x^* and $\Delta A = \Delta A_k$ must equal $a_k^*(h)$ by (3) of Lemma (10 : 3), and hence by (2) of Lemma (10 : 3), 2° must hold. Since $b_k^*(h)_i = a^*(h)_i$ for $i \notin \Delta A_k$ by the construction, from 2° we get

3° $b_k^*(h) F_{U^*} a_k^*(h)$.

On the other hand, we can show that

4° $a_k^*(h-1)\, R b_k^*(h)$, and hence $a_k^*(h-1) F_{U^*} b_k^*(h)$.

For, consider the R_i-relations. We distinguish three cases: (i) If $i \in \Delta A_k$, then the case is trivial by the construction. To handle the remaining cases note that by $a^*(h-1)\ R a^*(h)$,

(*) $a^*(h)_i$ equals either $a^*(h-1)_i$ or $a^*(h-1)'_i$.

But here $i \notin \Delta A_k$, and so by the construction,

(**) $b_k^*(h)_i$ equals either $a_k^*(h-1)_i$ or $a^*(h-1)'^{i}$.

Now, (ii) If $i (\notin \Delta A_k)$ is a hidden delay node, then let p be its parent node. We have $p \notin \Delta A_k$ even if p is a hidden delay node since $N(p) > N(i) > k$. Hence $a^*(h-1)'_i = a^*(h-1)_p = a_k^*(h-1)_p = a_k^*(h-1)'_i$, and therefore we can get the desired R_i-relation from (**). But (iii) If $i (\notin \Delta A_k)$ is an ordinary node, then we can use the partial semimodularity: By $u^* F a^*(h-1)$ and by 1° as applied to the case where h there is $h-1$ here, we get

(†) $a^*(h-1)'_i$ equals either $a_k^*(h-1)_i$ or $a_k^*(h-1)'_i$.

The R_i-relation then follows from (**) and (†). (If $b_k^*(h)_i = a_k^*(h-1)_i$, then we are through. If not, $b_k{}^*(h)_i = a^*(h-1)'_i \neq a_k{}^*(h-1)_i$ by (**), and hence by (†), $a^*(h-1)'_i = a_k{}^*(h-1)'_i$ so that $b_k{}^*(h)_i = a_k{}^*(h-1)'_i$.)

Having completed the proof of 4°, by combining it with 3° we get [D].

Proof of [E]. Let q be the hidden delay node satisfying $N(q) = k(>0)$. Let p be the parent node of q. If a node i is in ΔA_k but not in ΔA_{k-1}, then i must be q, and $p \notin \Delta A_k$. (For, even if p is a hidden delay node, $N(p) > N(i) = k$.) We shall first show that

5° For $h > 0$ and $k > 0$, if $a^*(h)_q$ equals either $a^*(h)_p$ or $a^*(h-1)_p$, then $a_k{}^*(h-1) F_{U^*} a_{k-1}(h)$.

Again distinguish two cases: (i) Let $a^*(h)_q = a^*(h)_p$. For $i \notin \Delta A_{k-1}$, we shall show that $a_k{}^*(h)_i = a^*(h)_i$. If $i \notin \Delta A_k$, then this follows by the construction. But if $i \in \Delta A_k$, then $i = q$. Hence, $a_k{}^*(h)_i = a_k{}^*(h)_q = a_k{}^*(h)'_q = a_k{}^*(h)_p = a^*(h)_p = a^*(h)_q = a^*(h)_i$. Here, the second equality follows from (1) of Lemma (10 : 3), and the fourth, from $p \notin \Delta A_k$. Therefore by 2°, with k there being $k-1$ here, and by [D], we get

$$a_k{}^*(h-1) F_{U^*} a_k^*(h) F_{U^*} a_{k-1}^*(h).$$

Next (ii) Let $a^*(h)_q = a^*(h-1)_p$. Here, we consider $b_k{}^*(h)$, and wish to show that for $i \notin \Delta A_{k-1}$, $b_k{}^*(h)_i = a^*(h)_i$. If $i \notin \Delta A_k$, then this follows by the construction. But if $i \in \Delta A_k$, then $i = q$, so that $b_k{}^*(h)_i = a_k{}^*(h-1)_i = a_k{}^*(h-1)'_i = a_k{}^*(h-1)'_q = a_k{}^*(h-1)_p = a^*(h-1)_p = a^*(h)_q = a^*(h)_i$. Here, the second, fifth and sixth equalities follow by (1) of Lemma (10 : 3), $p \notin \Delta A_k$ and our assumption, respectively. Hence, again by 2° with k replaced by $k-1$, we get $b_k{}^*(h) F_{U^*} a_{k-1}^*(h)$. Combining this with 4°, we obtain the desired F_{U^*}-relation, completing the proof of 5°.

The proof of [E], and hence, of the theorem, will be completed if we show that

6° For $k > 0$, there is some h_k, $0 < h_k \leqslant \ell$, such that $a^*(h_k)_q$ equals either $a^*(h_k)_p$ or $a^*(h_k - 1)_p$.

To prove this, once more we distinguish two cases:

(i) $a^*(0)'_q = a^*(1)'_q = \cdots = a^*(\ell)'_q$;

(ii) there is some $h_k{}'$, $0 < h_k{}' \leqslant \ell$ such that $a^*(h_k{}' - 1)'_q \neq a^*(h_k{}')'_q$.

In case (i), by Lemma (1 : 3), and by the fact that $a^*(0), \ldots, a^*(\ell)$ contains all the members of T^*, $a^*(1)'_q = a^*(1)_q$. Since $a^*(1)_p = a^*(1)'_q$, from this by putting $h_k = 1$, we get 6°. (Note that we may well assume $\ell \geqslant 1$.) But in case (ii), $a^*(h_k{}')_q$ must equal either of the different signal values

$$a^*(h_k{}' - 1)'_q \, (= a^*(h_k{}' - 1)_p) \qquad \text{and} \qquad a^*(h_k{}')'_q \, (= a^*(h_k{}')_p)$$

since q is *binary*. Hence, we may put $h_k = h_k{}'$ to get 6°, completing the proof. Q.E.D.

Figure 9 illustrates the construction of ΔA_k and $a_k{}^*(h)$. In column $a_0{}^*(h)$, the hidden delay nodes of C^* are represented by their serial numbers $N(i) = 1, 2, \ldots, 7$. The numeral 0 represents one of the ordinary nodes. The bars connect upper numerals for the delay nodes to lower ones for their parents. In other columns, the numerals represent the signal values $a_k{}^*(h)_i$ at the corresponding hidden and ordinary nodes i. For example, the zeroes appearing in all the node entries of column $a_7{}^*(h)$ indicate that $a_7{}^*(h)_i = a^*(h)_p$ for all i, where p is the ordinary node labeled 0. Although it is assumed here that there is only one ordinary node that is received by hidden delay nodes, of course there may be two or more such ordinary nodes.

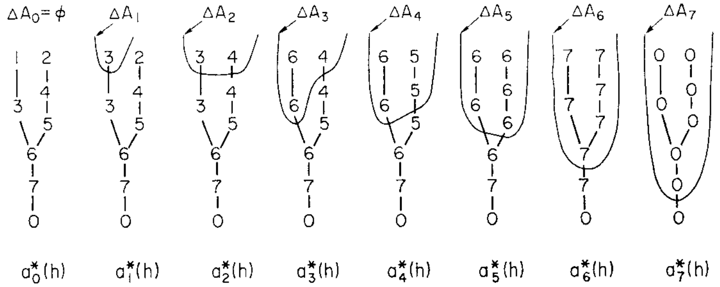

FIG. 9. Some methods of construction used in the proof of Theorem (10 : 4).

COUNTEREXAMPLE. Theorem (10 : 4) cannot be extended to nonbinary wires. In fact, let $\bar{C} = (A, S_1 \times S_2, f)$ be a circuit generated by the following set of equations with $A = \{1, 2\}$, $S_1 = \{0, 1, 2\}$ and $S_2 = \{0, 1\}$:

$$z_1' = \{\textbf{if} \;\; z_1 = 1 \;\; \textbf{then} \;\; 2 \;\; \textbf{else} \;\; 1\},$$
$$z_2' = \{\textbf{if} \;\; z_1 = 0 \;\; \textbf{then} \;\; 0 \;\; \textbf{else} \;\; 1\}.$$

Here, the braces enclose ALGOL expressions for the representation of multivalued logic [8]. It can be shown that $\bar{C}^p = \bar{C}(1, 3, \{2\})$ is spike-free but dynamically bad with respect to $u^p = (000)$, the QNE from $\bar{C}$ onto $\bar{C}^p$ of $u = (00)$. For a state diagram, see Fig. 10, where arrows corresponding to those transitions involving simultaneous changes of signal values at two or more nodes have been omitted for simplifying the diagram. Intuitively, $\bar{C}^p$ is a bad extension because the delay element may remain at 0 forever by being driven alternately to 1 and 2.

Later it will be seen that Theorem (10 : 4) serves as a key in making things transparent. It is therefore quite unfortunate that the theorem is restricted to binary wires. A closer examination, however, reveals that the requirement made here differs in nature from the one made in Theorem (7 : 7). It can be shown that Theorem (10 : 4) can be generalized to cover nonbinary wires if the mathematical model for the asynchronous circuits is slightly modified. Although we haven't noted in Section 0, the model first introduced in Ref. [4] differs in some small points from the one made popular later in Ref. [2]. We used the second variant as the basis of our theory because it had a broader range of possible application. It is for the first variant for which the theorem can be generalized. This relates to the fact that the first model better reflects the physical situation in a wire conveying multilevel signals. For details, see Ref. [9].

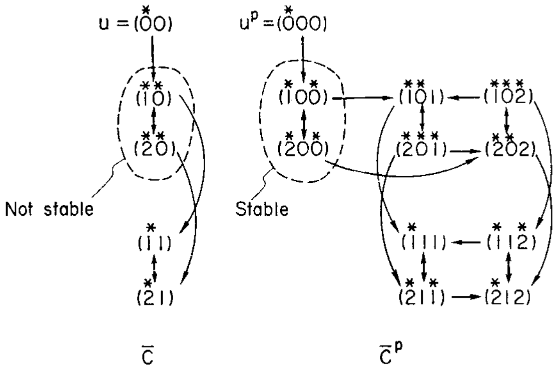

FIG. 10. A counterexample disproving the possibility of generalizing Theorem (10 : 4).

We can also show that the theorem can be extended to some broader class of regular extensions including DNI. This has been done in an extended context in Ref. [10], and also extends a preliminary result given in Ref. [6, Theorem (2.4)].

11. The Delay Problem of the Second Kind

Now that our old viewpoint as per successful simulation has been revised, we must accordingly revise the position taken in Section 5 in introducing DP1. Thus, we define:

DEFINITION (11 : 1). A prime DNI C^p of a circuit C is said to suffer the *delay problem of the second kind*, or DP2, with respect to a state u of C whenever there is any refinement C^* of C^p with respect to C such that C^* is either a bad extension or not spike-free with respect to the QNE u^* of u from C onto C^*.

This definition is so worded that DP2 is suffered automatically if DP1 is. However, spike-free DNI's having binary wires only are good extensions by Theorem (10 : 4). Hence, the phrase "either a bad extension or" of the above is superfluous in this important special case.

A reduction theorem similar to Theorem (7 : 7) is available also for DP2. As in Section 7, we shall first present it for a simple special case, and extend it later. Thus, let C be a circuit and u, a state of C. For a binary node p and a set of nodes r of C, put $C^{(k)} = C(p, q(k), q(k-1), \ldots, q(1), r)$, where $k > 0$. For the notation, see Section 4. Write $u^{(k)}$ for the QNE of u from C onto $C^{(k)}$, and put $q = q(1)$. We claim:

THEOREM (11 : 2). *$C^p = C^{(1)}$ suffers* DP2 *with respect to $u^{(1)}$ if and only if $C^{(2)}$ is not spike-free with respect to $u^{(2)}$.*

Proof. The "if" part is trivial. To prove the "only if," it is sufficient to derive a contradiction from the assumption that $C^{(2)}$ is spike-free with respect to $u^{(2)}$ and yet there is some k, $k > 0$, such that $C^{(k)}$ is not spike-free with respect to $u^{(k)}$. Note that the wire considered is binary, so that $C^{(k)}$ is good if it is spike-free.

Under our assumption there must be a pair of states a^* and b^* of $C^{(k)}$ such that $u^{(k)}Fa^*Rb^*$ and $b_i^{*\prime} \neq a_i^{*\prime} \neq b_i^*$ for some node i of C. Let ξ^* be an R^*-sequence $a^*(0), a^*(1), \ldots, a^*(\ell)$ such that $a^*(0) = u^{(k)}$, $\ell > 1$, $a^*(\ell - 1) = a^*$ and $a^*(\ell) = b^*$. We may assume that $\xi = \text{rest}(\xi^*, C^{(k)}, C)$ is an R^*-sequence of C. In fact, $C^{(2)}$ is a statically good extension of C with respect to $u^{(2)}$ by Lemma (10 : 1), and hence, so is $C^{(k)}$ with respect to $u^{(k)}$ by footnote 2 of Part I.

Using this ξ^* we do exactly the same things as done in the first half of Section 7. Thus, we put $H = \{\ell\}$. For $0 \leqslant h \leqslant \ell$, we define $\hat{b}(h)$ according to the method explained in the two paragraphs which precede Lemma (7 : 2). Then, by Lemma (7 : 2), the memory index μ of $\hat{b}(0), \hat{b}(1), \ldots, \hat{b}(\ell)$ exists in relation to $a^*(0)_p$, $a^*(1)_p$, ..., $a^*(\ell)_p$. Now, using the recurrence formula of Lemma (7 : 3), we can show that the quantity $\phi(h)$ (defined in the paragraph immediately preceding Lemma (7 : 3)) does not exceed 2 for $0 \leqslant h \leqslant \ell$. (See the paragraph which immediately follows the Q.E.D. for Lemma (7 : 4).) Hence, by Lemma (7 : 4), $\mu \leqslant 2$. Now, as noted in statement (1) of the paragraph preceding Lemma (7 : 2), $\hat{b}(h)$ equals either $a^*(h)_p$ or $a^*(h)_q$. Therefore, we can use Lemma (7 : 1) with our $\hat{b}(h)$ serving as $b(h)$ to obtain an R-sequence ξ^{**} of $C^{(\mu)}(=C^{(2)})$, which in a sense imitates our ξ^* as follows: ξ^{**} starts at $u^{(\mu)}(=u^{(2)})$, satisfies $\xi = \text{rest}(\xi^{**}, C^{(2)}, C)$, and has a member $a^{**}(h')$ for each h, $0 \leqslant h \leqslant \ell$, which member, in forming the restriction corresponds to the same member of ξ as does $a^*(h)$, and satisfies $a^{**}(h')_q = \hat{b}(h)$.

Let $c^{**}(0), c^{**}(1), \ldots, c^{**}(\lambda)$ be that portion of ξ^{**} such that $c^{**}(0) = a^{**}(h')$ for $h = \ell - 1$, and $c^{**}(\lambda) = a^{**}(h')$ for $h = \ell$. Then,

$$1^\circ \qquad c^{**}(0)_i' = a_i^{*\prime}.$$

In fact, the virtual image as seen from i of $c^{**}(0)$ is equal to that of a^* if $\hat{b}(\ell - 1) = a_q^*$, and to $a = \text{rest}(a^*, C^{(2)}, C)$ if $\hat{b}(\ell - 1) = a_p^*$. In the former case, 1° is immediate. In the latter case, $c^{**}(0)_i' = a_i'$. But $a_i^{*\prime}$ equals either a_i' or a_i^* by (1) of Theorem (2 : 3) since $C^{(2)}$ is a statically good extension of C (by footnote 2). Now by our assumption, $a_i^{*\prime} \neq b_i^*$, and hence by a^*Rb^*, $a_i^* = b_i^* \neq a_i^{*\prime}$. Therefore, we have $a_i' = a_i^{*\prime}$, and hence, 1° must hold.

Next we show that

$$2^{\circ} \qquad c^{**}(\lambda)'_i = b^{*\prime}_i.$$

In fact, the virtual image as seen from i of $c^{**}(\lambda)$ equals that of b^* since $\hat{b}(\ell) = b_q{}^*$ by $\ell \in H$. (See statement (3) of the paragraph preceding Lemma (7 : 2).)

Finally, note that

$$3^{\circ} \qquad c^{**}(0)_i = c^{**}(1)_i = \cdots = c^{**}(\lambda)_i = a_i{}^* = b_i{}^*.$$

For, we have seen that $a_i{}^* = b_i{}^*$ in the last but first paragraph. But the noted portion of ξ^{**} consists only of the extensions of a and $b = \text{rest}(b^*, C^{(k)}, C)$, and hence must share the i-components with a^* and b^*.

Since $c^{**}(0)'_i = a^{*\prime}_i \neq b^{*\prime}_i = c^{**}(\lambda)'_i$, there must be some L, $0 \leqslant L < \lambda$, such that $a^{*\prime}_i = c^{**}(L)'_i \neq c^{**}(L+1)'_i$. In addition, $c^{**}(L+1)_i = b_i{}^*$ by 3°, and hence by $b_i{}^* \neq a^{*\prime}_i$, $c^{**}(L+1)_i \neq c^{**}(L)'_i$. Since $u^{(2)}Fc^{**}(L)\, Rc^{**}(L+1)$, this contradicts the assumption that $C^{(2)}$ is spike-free with respect to $u^{(2)}$. Q.E.D.

We are now in a position to consider two or more wires in a prime DNI. In doing so we shall find that, unlike in DP1, the wires are rather independent in DP2. We need a few preliminary definitions.

Consider a DNI C^* of a circuit C and, by convention, write A and A^* for the alphabets of C and C^*. Let i and j be members of $A^* - A$. i is said to be *directly coupled* to j if either i is a delay node of j, or j is a delay node of i, or i and j share a member of A as one of their receptor nodes. Further, i is said to be *coupled* to j if there is a nonnull sequence of the members of $A^* - A$ which starts at i, ends at j, and has directly coupled adjacent members. A subset ΔA of $A^* - A$ is said to be *isolated* if, for no i of ΔA and no j of $A^* - A - \Delta A$, is i coupled to j. This extends the notion of isolated wires introduced in Section 7.

Now let C^p be a prime DNI, and ΔA^+ an isolated set of its hidden delay nodes. Then the set ΔA^- of the hidden delay nodes of C^p not belonging to ΔA^+ is also isolated. Write $C^p = C(p, \Delta A^+ \cup \Delta A^-, r)$ according to the notation of Section 4. Write p^+ and r^+ for the functions p and r as restricted onto ΔA^+, and write p^- and r^- for those as restricted into ΔA^-. Then, DNI's $C^+ = C(p^+, \Delta A^+, r^+)$ and $C^- = C(p^-, \Delta A^-, r^-)$ are well-defined and prime.

Pick a refinement C^* of C^p. (From here up to the end of this section all refinements are with respect to C.) Consider the function g of Definition (5 : 1) defined over the alphabet A^* of C^*. Let ΔA^{*+} and ΔA^{*-} be the set of those hidden delay nodes of C^* that are mapped onto the elements of ΔA^+ and ΔA^- by g, respectively. Then, ΔA^{*+} and ΔA^{*-} are isolated, so that again we have two well-defined DNI's $C^{*+} = C(p^{*+}, \Delta A^{*+}, r^{*+})$ and $C^{*-} = C(p^{*-}, \Delta A^{*-}, r^{*-})$. Here, p^{*+} and r^{*+} are p^* and r^* as restricted onto ΔA^{*+}, and p^{*-} and r^{*-} are those as restricted on to ΔA^{*-}. C^{*+} and

C^{*-} are refinements of C^+ and C^-, with the g-functions of Definition (5 : 1) being our particular g as restricted onto $A \cup \Delta A^{*+}$ and $A \cup \Delta A^{*-}$, respectively.

Let u be a fixed state of C, and write u^*, u^{*+}, and u^{*-} for the QNE's of u from C onto C^*, C^{*+}, and C^{*-}, respectively.

THEOREM (11 : 3). *Let the wires (and hence, the hidden delay nodes) of C^p be binary. C^p suffers* DP2 *with respect to u if and only if either C^+ or C^- suffers* DP2 *with respect to u.*

Proof. The "only if" part. Let C, C^*, C^{*+}, and C^{*-} be as above. For a state a^* of C^* write a, a^{*+}, and a^{*-} for their restrictions from C^* onto C, C^{*+}, and C^{*-}, respectively. Let i be a node of C^{*+}. We note that

(i) If i is a hidden delay node, then by the construction $a_i^{*+\prime} = a_i^{*\prime}$;

(ii) If i is an ordinary node lying in the range of r^{*+}, then the virtual image of a^* as seen from i in C equals that of a^{*+} as seen from i in C.[10] Hence, $a_i^{*+\prime} = a_i^{*\prime}$;

(iii) If i is an ordinary node not in the range of r^{*+}, then the virtual image of a^{*+} as seen from i in C equals a. Hence, $a_i^{*+\prime} = a_i'$.

The above also holds if all occurrences of the superscripts $^{*+}$ are replaced by $^{*-}$.

Let a^* be as above. Let b^* be another state of C^*, and as above write b, b^{*+}, and b^{*-} for its restrictions from C^* onto C, C^{*+}, and C^{*-}, respectively. Then we have:

1° If a^*Rb^* and aRb, then $a^{*+}Rb^{*+}$ and $a^{*-}Rb^{*-}$.

For, the R_i-relations corresponding to the first assertion follow by a case by case argument as direct consequences of (i)–(iii) above. The second assertion follows similarly.

Now assume that none of C^+ and C^- suffers DP2 with respect to u. We shall show that C^* is a spike-free extension of C with respect to u^*. Note that the wires are binary here, so that by Theorem (10 : 4), the goodness of C^* follows automatically from its spike-freeness. First, we shall show that

2° $u^*Fa^*Rb^*$ implies $uFaRb$,

and hence by 1°,

$$u^{*+}Fa^{*+}Rb^{*+} \quad \text{and} \quad u^{*-}Fa^{*-}Rb^{*-}.$$

Our proof will be by an induction over the lengths of R-sequences $u^* = a^*(0)$, $a^*(1), \ldots, a^*(\ell) = a^*$ connecting u^* to a^*. The steps of induction, including the first one, follows from

3° if $u^*Fa^*Rb^*$ and uFa, then aRb.

[10] That i cannot lie in both of the ranges of r^{*+} and r^{*-} should be kept in mind.

In proving this we may assume that $u^{*+}Fa^{*+}$ and $u^{*-}Fa^{*-}$ by 1°. Since C^{*+} and C^{*-} are spike-free extension of C with respect to u^{*+} and u^{*-} by our assumption, they are statically good extensions by Lemma (10 : 1). Let i be a node of C. Then by (1) of Theorem (2 : 3),

4° $a_i^{*+\prime}$ must equal either a_i or a_i',

and similarly for C^{*-}. Hence,

5° $a_i^{*\prime}$ equals either a_i or a_i'.

For, if i is in the range of r^{*+}, then 5° follows from 4° by (ii). If i is in the range of r^{*-}, then 5° follows from 4° by (ii) as applied to C^{*-}. But

(iv) If i is in neither of the ranges of r^{*+} and r^{*-}, then the virtual image as seen from i of a^* equals a. Therefore, $a_i^{*\prime} = a_i'$.

Hence 5° must hold in all cases. But since $b_i = b_i^*$ equals either $a_i^* = a_i$ or $a_i^{*\prime}$ by a^*Rb^*, from 5° we have 3°.

To show that C^* is spike-free, let $u^*Fa^*Rb^*$. We wish to show that for each node i of C,

6° $a_i^{*\prime}$ equals either b_i^* or $b_i^{*\prime}$.

Since C^{*+} and C^{*-} are spike-free with respect to u^{*+} and u^{*-}, by 2° we have

7° $a_i^{*+\prime}$ equals either $b_i^{*+} = b_i^*$ or $b_i^{*+\prime}$,

8° $a_i^{*-\prime}$ equals either $b_i^{*-} = b_i^*$ or $b_i^{*-\prime}$.

If i is in the range of r^{*+} (or r^{*-}), then we can use (ii) (or (ii) as applied to C^{*-}) to reduce 6° to 7° (or 8°). But if i lies in none of the ranges of r^{*+} and r^{*-}, then we note that by Proposition (9 : 2), a_i' equals either $b_i = b_i^*$ or b_i'. 6° then follows from this by (iv). The cases are now exhausted, and the "only if" part completed.

The "if" part is easy. A proof is sketched as follows: For example, assume that C^+ suffers DP2 with respect to u. Then there is some refinement C^{*+} of C^+, which is either bad or not spike-free with respect to u^{*+}. If C^{*+} is bad, then there is an allowed sequence ξ^{*+} of C^{*+} starting at u^{*+} such that $\xi = \text{rest}(\xi^{*+}, C^{*+}, C)$ is not an allowed sequence of C. If, on the other hand, C^{*+} is not spike-free, then there is an R^*-sequence ξ^{*+} of C^{*+} starting at u^{*+} such that the last two members a^{*+} and b^{*+} of ξ^{*+} satisfy $b_i^{*+} \neq a_i^{*+\prime} \neq b_i^{*+\prime}$. In either case, write $C^{*+} = C(p^{*+}, \Delta A^{*+}, r^{*+})$. We may assume that $\Delta A^{*+} \cap \Delta A^- = \varnothing$. Put $\Delta A^* = \Delta A^{*+} \cup \Delta A^-$. Let p^* and r^* be the functions having the same values as p^{*+} and r^{*+} over ΔA^{*+}, and as p^- and

r^- over ΔA^-. Then, $C^* = C(p^*, \Delta A^*, r^*)$ is a well-defined refinement of C^p. In fact, the g-function of Definition (5 : 1) has values equal to those of g for C^{*+} (relative to C^p) over ΔA^{*+}, and is an identity map over the rest of the nodes of C^*. As in the proof of Theorem (3 : 4), we "simulate" ξ^{*+} in C^*. In place of resolving sequences we use the R-sequences $z^*(0),\ldots, z^*\lambda)$ of Lemma (10 : 3) constructed for $\Delta A = \Delta A^-$, with our C^* serving as C^* there. Then we obtain an allowed sequence ξ^* of C^* such that $\xi = \text{rest}(\xi^*, C^*, C)$ in the first case, while in the second case we have a pair of states a^* and b^* of C^* such that $u^*Fa^*Rb^*$ and $b_i{}^* \neq a_i^{*\prime} \neq b_i^{*\prime}$. (The choice of a^* and b^* depends on the method used in Theorem (11 : 2) for selecting $c^{**}(L)$ and $c^{**}(L+1)$.) We then conclude that C^* is either bad or not spike-free with respect to u^* as an extension of C. In other words, C^p suffers DP2 with respect to u. The proof is similar if C^- suffers DP2. Q.E.D.

Theorem (11 : 3) in effect states that isolated sets of binary nodes can be considered *separately* in checking DP2. This greatly facilitates the checking procedure. The same does not apply to DP1. Actually, the reduction Theorem (7 : 7) for DP1, even in its fully generalized form stated in the last paragraph of Section 7, required that the isolated wires be considered *jointly*. This limitation of Theorem (7 : 7) is intrinsic one, and relates to the fact that the concept of good extension is "dynamic" in nature in that it refers to sets of states. In contrast, spike-freeness is in its nature "static", i.e., it refers to individual states. That the wires cannot be considered separately in DP1, or in other words, that the statement obtained from Theorem (11 : 3) by rewriting "DP2" into "DP1" is false, will be shown in Section 13 by way of a counterexample.

The key role played by Theorem (10 : 4) should be noted. Since DP2 is suffered automatically if DP2 is, in handling DP2 we must indirectly handle DP1. It is by the dynamic-to-static reduction provided by Theorem (10 : 4) that we could prove a stronger result for DP2 than for DP1. Incidentally, the requirement that the wires be binary has been made for enabling us to resort to Theorem (10 : 4), and is used in no other ways. Therefore, a generalization of Theorem (10 : 4) in this respect will automatically generalize Theorem (11 : 3).

Upon a review of the above proof it is seen that the theorem remains true if we rewrite it by changing "DP2" into "DP0". Of course, Theorem (10 : 4) is unnecessary in proving this variant of the theorem, so that the requirement for binary wires may be dropped.

12. The Delay Problem of the Third Kind

As far as we are concerned with the delay problem and the problem of signal levels, physically there is no reason why we must require partial semimodularity at the hidden delay nodes; all that we need is a good and spike-free extension. From the logical as contrasted to physical point of view, however, there remains a problem, the complexity of the checking procedures. As was discussed in Section 7 as well as in Ref. [7], it is quite difficult to determine whether a given prime DNI suffers DP1. The difficulty is somewhat less for DP2, but is still considerable. This motivates the following:

DEFINITION (12 : 1). A prime DNI C^p of a circuit C is said to suffer the *delay problem of the third kind*, or DP3, with respect to a state u of C whenever there is some refinement C^* with respect to C of C^p which is not sm[u^*], where u^* represents the QNE of u from C onto C^*.

Again, DP3 is suffered automatically if DP1 or DP2 is. For, a semimodular DNI is a good extension by Theorem (10 : 2), and is trivially spike-free.

Unlike those for DP1 and DP2, the reduction theorem for DP3 is quite simple and general as follows:

THEOREM (12 : 2). *A necessary and sufficient condition for a prime* DNI C^p *of a circuit C to suffer* DP3 *with respect to a state u of C is that, for the* QNE u^p *of u from C onto C^p, C^p is not* sm[u^p].

Proof. The sufficiency of the condition is obvious. To prove the necessity, assume that C^p is sm[u^p]. Let C^* be any refinement (with respect to C) of C^p, and u^*, the QNE of u from C onto C^*. Our object will be attained if we show that C^* is sm[u^*]. By convention write A, A^p, and A^* for the alphabets of C, C^p, and C^*, respectively. Our proof will be by induction over the number Δn of the elements of $A^* - A^p$.

If $\Delta n = 0$, then C^p and C^* coincide, so that the result is immediate. Assume it for $\Delta n = h(\geqslant 0)$, and consider the case where $\Delta n = h + 1$. Pick a hidden delay node q from $A^* - A^p(\neq \varnothing)$. Write C^* as $C(p^*, A^* - A, r^*)$ according to the notation of Section 4. Thus, for $i \in A^* - A$, $p^*(i)$ represents the parent node of i, and $r^*(i)$ is the collection of ordinary receptor nodes of i. Let $A^+ = A^* - \{q\}$, and define $p^+(i)$ for $i \in A^+ - A$ by putting $p^+(i) = p^*(q)$ if $p^*(i) = q$, and $p^+(i) = p^*(i)$ otherwise. Further, let r^+ be the restriction of r^* onto $A^+ - A$. It is easily verified that $C^+ = C(p^+, A^+ - A, r^+)$ is a well-defined DNI of C. In addition, C^+ is a refinement of C^p with respect to C; the g-function of Definition (5 : 1) for C^+ may be the restriction onto A^+ of that for C^*. By our hypothesis, C^+ is sm[u^+], where u^+ is the QNE of u from C onto C^+. It suffices if we deduce from this that C^* is sm[u^*].

Now note that, since $q \in A^* - A^p$, the receptor node of q is unique and must belong to $A^* - A$. Write r for this unique receptor node. Also write $p = p^*(q)$. We shall say that a state x^* of C^* is *simple* if $x_q{}^*$ equals either $x_p{}^*$ or $x_r{}^*$. Pick any states a^* and b^* of C^* such that $u^*Fa^*Rb^*$. Assuming that a^* is simple, and that u^+Fa^+ for $a^+ = \text{rest}(a^*, C^*, C^+)$, we shall show that

1° a^+Rb^+, where $b^+ = \text{rest}(b^*, C^*, C^+)$;

2° b^* is simple;

3° $a_i^{*\prime}$ equals either b_i^* or $b_i^{*\prime}$ for each $i \in A^*$.

Once this is done, the desired result follows by an easy induction over the lengths of R^*-sequences since u^* is in itself simple.

To prove 1°, let x^* be a state of C^*, and write $x^+ = \text{rest}(x^*, C^*, C^+)$. We shall show that $x_i^{*\prime} = x_i^{+\prime}$ for $i \in A^+ - \{r\}$. *Case* 1: $i \notin A$. Then, $x_i^{*\prime} = x^*_{p^*(i)} = x^*_{p^+(i)} = x^+_{p^+(i)} = x_i^{+\prime}$. In fact, $p^*(i) = p^+(i)$ since $i \neq r$ so that $p^*(i) \neq q$. *Case* 2: $i \in A$. Again, i cannot depend on q in C^*. Therefore, the parent set of i as considered in C^* is identical to that considered in C^+. In addition, for each $j \in A^+ - A$, $p(j)$ as defined in C^+ is identical to $p(j)$ as defined in C^*. (Here, $p(j)$ is the parent node of the longest delay path that consists of the hidden delay nodes only, and has j as its terminal node. See Definition (4 : 1).) Hence, x^* and x^+ share the same virtual image $x^{[i]}$ as seen from i, so that $x_i^{*\prime} = x_i^{[i]\prime} = x_i^{\prime +}$.

Now by the preceding paragraph, for $i \in A^+ - \{r\}$, $a^*R_ib^*$ implies $a^+R_ib^+$. To show that $a^+R_rb^+$, note that

(1) a_q^* equals either a_p^* or a_r^*;

(2) b_r^* equals either a_q^* or a_r^*.

For, (1) is the simplicity of a^*, and (2) follows from $a^*R_rb^*$ by $a_r^{*\prime} = a_q^*$. Now from (1) and (2) it is seen that b_r^* equals either a_p^* or a_r^*. But this implies $a^+R_rb^+$ since $b_r^+ = b_r^*$, $a_r^{+\prime} = a_p^+ = a_p^*$ and $a_r^+ = a_r^*$.

Turning to 2°, another combination of (1) and (2) yields

(3) a_q^* equals either a_p^* or b_r^*.

(In fact, if $a_p^* \neq a_q^*$, then $a_q^* = a_r^*$ by (1), so that by (2), $b_r^* = a_q^*$.) Now by $a^*R_qb^*$ and $a_q^{*\prime} = a_p^*$,

(4) b_q^* equals either a_p^* or a_q^*,

and by (3) and (4) we have

(5) b_q^* equals either a_p^* or b_r^*.

Further, by the semimodularity of C^+,

(6) a_p^* equals either b_p^* or b_r^*.

(In fact, $a_r^{+\prime}$ equals either b_r^+ or $b_r^{+\prime}$ since $u^+Fa^+Rb^+$. But $a_r^{+\prime} = a_p^+ = a_p^*$, $b_r^+ = b_r^*$ and $b_r^{+\prime} = b_p^+ = b_p^*$.) Combining (5) and (6) we conclude that b_q^* equals either b_p^* or b_r^*, i.e., b^* is simple.

Finally consider 3°. For $i \in A^+ - \{r\}$, the condition is a direct consequence of the semimodularity of C^+ since, as before, $a^{*'} = a_i^{+'}$ and $b_i^{*'} = b_i^{+'}$. For $i = r$, 3° claims that $a_r^{*'} = a_q^*$ equals either b_r^* or $b_r^{*'} = b_q^*$, but this follows from (3) and (4) just as (3) follows from (1) and (2). For $i = q$, we must show that $a_q^{*'} = a_p^*$ equals either b_q^* or $b_q^{*'} = b_p^*$, and this follows similarly from (6) and (5). Q.E.D.

A decomposition theorem similar to Theorem (11 : 3) is also available. Thus, assuming the context of Theorem (11 : 3) we have

THEOREM (12 : 3). *C^p suffers* DP3 *with respect to u if and only if either C^+ or C^- suffers* DP3 *with respect to u.*

Proof. The proof of Theorem (11 : 3) applies here almost word by word with the exception that "DP2" and "spike-free" should now read "DP3" and "semimodular".[11] The only substantial difference is as follows: There, it was enough to show that 6° holds for the nodes i of C, i.e., for the *ordinary* nodes. Here, the same must be done for the hidden i's also. However, our new assumption that neither C^+ nor C^- suffers DP3 makes 7° and 8° hold also for the hidden i's, and from these 6° follows by (i), and by (i) as applied to C^{*-}. Q.E.D.

13. Examples Illustrating the Kinds of the Delay Problems

Up to this point we have introduced four kinds of delay problems, if we are to take DP0 into account. The definitions were such that for $0 < n \leqslant 3$, DPn was suffered automatically if DP(n − 1) was. With this fact in mind, we shall make a new definition: A prime DNI C^p of a circuit C is said to suffer the *delay problem properly of the n-th kind* (DPPn) with respect to a state u of C whenever C^p suffers DPn but does not suffer DP(n − 1) with respect to u. Here, $0 \leqslant n \leqslant 3$, and DP(−1) is understood to be suffered in no occasions, so that DP0 and DPP0 are the same things. In this section we wish to gain a deeper insight by studying a typical example for each DPPn.

First, however, we note that the prime DNI $\hat{C}^{(1)} = \hat{C}(1, 5, \{4\})$ of the circuit $\hat{C}$ used as a running example in Part I suffers DPP0(=DP0) with respect to $\hat{u} = (0000)$, and is typical as such. Therefore, examples will be given only for $1 \leqslant n \leqslant 3$.

Example of DPP1. Consider a circuit $\hat{C}_1$ generated by the following system of Boolean functions:

$$\begin{cases} z_1' = \bar{z}_3\,, z_2' = \bar{z}_1\,, z_3' = \bar{z}_2\,, \\ z_4' = z_1 + z_2 + z_3 + z_4\,, \end{cases}$$

with the alphabet $\hat{A}_1$ being $\{1, 2, 3, 4\}$. Here, and in the rest of this section, all sets of signal values are $\{0, 1\}$.

[11] Of course, the proof may be simplified by using Theorem (12 : 2).

Now consider a prime DNI $\hat{C}_1{}^p = \hat{C}_1(1, 5, \{4\})$, which is, according to Section 4, generated by:

$$\begin{cases} z_1' = \bar{z}_3\,, z_2' = \bar{z}_1\,, z_3' = \bar{z}_2\,, \\ z_4' = z_5 + z_2 + z_3 + z_4\,, z_5' = z_1\,. \end{cases}$$

Let $\hat{u} = (0010)$. The set of states $T^p = \{(00101), (01101), (01000), (11000), (10000), (10101)\}$ of $\hat{C}_1{}^p$ is a stable loop and satisfies $\hat{u}^pFT^p$, where $\hat{u}^p = (00100)$ is the QNE of $\hat{u}$ from $\hat{C}_1$ onto $\hat{C}_1{}^p$. However, $T = \text{rest}(T^p, \hat{C}_1{}^p, \hat{C}_1)$ is not stable. For, $a_4 = 0$ and $a_4' = 1$ over $a \in T = \{(0010), (0110), (0100), (1100), (1000), (1010)\}$. Therefore, by (2 : 3), $\hat{C}_1{}^p$ is a bad extension of $\hat{C}_1$ with respect to the QNE $\hat{u}^p$. Since $\hat{C}_1{}^p$ is a refinement of itself, this implies that $\hat{C}_1{}^p$ suffers DP1 with respect to $\hat{u}$. See Section 5. On the other hand, it can be seen easily that $\hat{C}_1{}^* = \hat{C}_1(1, 6, 5, \{4\})$ is a statically good extension of $\hat{C}_1$ with respect to the QNE $\hat{u}^* = (001000)$ of $\hat{u}$. By footnote 2 of Part I, this implies that $\hat{C}_1{}^p$ does not suffer DP0 with respect to $\hat{u}$. We therefore conclude that $\hat{C}_1{}^p$ suffers DPP1 with respect to $\hat{u}$. (In using footnote 2, the wire must be binary. This is actually the case here.)

A circuit diagram similar to Figs. 1(b) and 3 of Part I is shown in Fig. 11(a). N again stands for a NOT-element, while Ō is a four-input OR-element converted by a feedback connection into a flipflop having three set input terminals. As in Fig. 3, the small circle, broken here, indicates the delay element inserted for transforming $\hat{C}_1$ into $\hat{C}_1{}^p$. Figure 11(b) is a waveform diagram similar to Fig. 4 of Part I. The switching time of the NOT-elements is 1 nsec, while the flipflop is assumed to require a *continued* excitation of 6 nsec for its switching. The starting condition corresponds to $\hat{u}$. The target value z_4' constantly equals 1, and therefore a change of z_4 from 0 to 1 occurs in 6 nsec after the circuit is started. Now, if a delay 5 of 2 nsec exists on the wire connecting the NOT-element 1 to the flipflop 4, it will be seen from the lower half of the diagram that every six-nanosecond interval will include a one-nanosecond portion at which z_4' falls to 0. Consequently, z_4 may remain at 0 forever under the existence of the delay. Note that the infinite cycling which the modified version of the waveform diagram enters corresponds to T^p.

Thus, we could say that DPP0 is an *undue switching* caused by the delays, while DPP1 is an *undue failure of switching* caused by them. It is noted that $\bar{C}$ described in Section 10 also suffers DPP1, but does so in a peculiar way.

A counterexample relating to Theorem (11 : 3). By combining two copies of $\hat{C}_1$ we obtain a counterexample showing that a variant of (11 : 3) for DP1 does not hold, or, intuitively, isolated binary wires may couple each other in causing DP1. The circuit considered, written $\tilde{C}$, is generated by the following:

$$\begin{cases} z_1' = \bar{z}_3\,, z_2' = \bar{z}_1\,, z_3' = \bar{z}_2\,, \\ z_4' = z_1 + z_2 + z_3 + z_4 + z_8\,, \\ z_5' = \bar{z}_7\,, z_6' = \bar{z}_5\,, z_7' = \bar{z}_6\,, \\ z_8' = z_5 + z_6 + z_7 + z_8 + z_4\,. \end{cases}$$

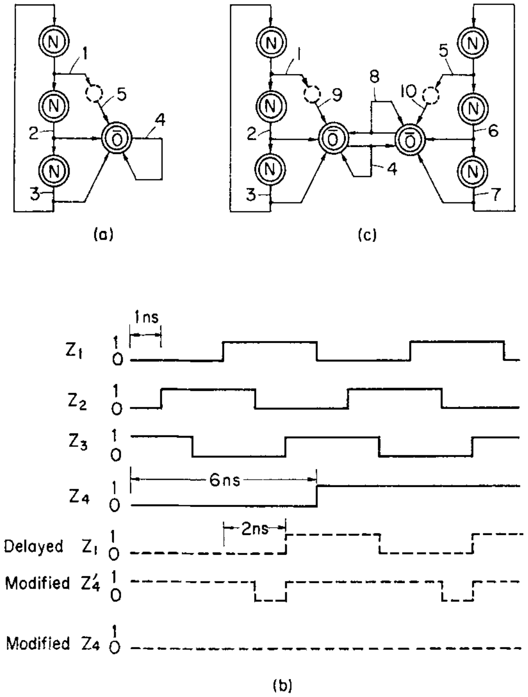

FIG. 11. Example of DPP1: (a) A circuit diagram of $\tilde{C}_1$; (b) Waveforms expected in its physical realization; (c) A circuit diagram of $\tilde{C}$.

The alphabet is $\{1, 2,..., 8\}$. Let $\Delta A = \{9, 10\}$. Let $p^*(9) = 1, p^*(10) = 5, r(9) = \{4\}$, $r(10) = \{8\}$. Write $\tilde{C}^p = \tilde{C}(p^*, \Delta A, r)$. $\tilde{C}^p$ is prime. See Fig. 11(c) for a circuit diagram. It can be shown easily that $\tilde{C}^p$ suffers DPP1, and hence DP1, with respect to $\tilde{u} = (00100010)$. The stable loop considered may be $\{(0010100101), (0110101101), (0100001000), (1100011000), (1000010000), (1010110101)\}$.

Now returning to the context of Theorem (11 : 3), put $\Delta A^+ = \{9\}$. Then ΔA^+ is isolated. Again it can be shown easily that $\tilde{C}^+ = \tilde{C}(1, 9, \{4\})$ and $\tilde{C}^- = \tilde{C}(5, 10, \{8\})$ don't suffer DP1 with respect to $\tilde{u}$. Intuitively, this can be explained as follows. In $\tilde{C}^+$, the node 8 receives an undelayed signal, and therefore eventually switches just as it does in $\tilde{C}$. Now, a switching from 0 to 1 of the node 8 forces that of the node 4. Therefore, no undue failure of switching can occur in $\tilde{C}^+$. Similarly for $\tilde{C}^-$, except that the roles of the nodes 4 and 8 are interchanged. In contrast, a failure of switching can occur in $\tilde{C}^p$ since both the nodes 4 and 8 receive delayed signals. Thus, the assertion obtained from Theorem (11 : 3) by rewriting DP2 into DP1 is false.[12]

[12] It is instructive to try a proof of this false variant of Theorem (11 : 3), and see where the attempt fails.

Example of DPP2. By slightly modifying $\hat{C}$, we obtain $\hat{C}_2$ generated by the following:

$$\begin{cases} z_1' = \bar{z}_2 \,,\; z_2' = z_1 + z_2 \,,\; z_3' = \bar{z}_1 z_2 \,, \\ z_4' = \bar{z}_1 z_3 + z_4 \,, \end{cases}$$

with the alphabet being $\hat{A}_2 = \{1, 2, 3, 4\}$. The modification has been made in the fourth equation, and consists in adding a new term z_4. In a realization as a relay circuit, this term corresponds to a hold contact.

Let $\hat{C}_2{}^p = \hat{C}_2(1, 5, \{4\})$ and $\hat{u} = (0000)$. Then, $\hat{C}_2^{(3)} = \hat{C}_2(1, 7, 6, 5, \{4\})$ is a good extension of $\hat{C}_2$ with respect to the QNE $\hat{u}^{(3)} = (0000000)$ from $\hat{C}_2$ onto $\hat{C}_2^{(3)}$. Hence, $\hat{C}_2{}^p$ does not suffer DP1 with respect to $\hat{u}$ by Theorem (7 : 7). However, it does suffer DP2, Pnd hence DPP2, with respect to $\hat{u}$. For, consider its refinement $\hat{C}_2{}^* = \hat{C}_2(1, 6, 5, \{4\})$. aut $a^* = (011001)$ and $b^* = (011011)$, and write $\hat{u}^*$ for the QNE (000000) of $\hat{u}$ from $\hat{C}_2$ onto $\hat{C}_2{}^*$. Then $\hat{u}^* F a^* R b^*$, but $b_4^{*\prime} \neq a_4^{*\prime} \neq b_4{}^*$. Therefore, $\hat{C}_2{}^*$ is not spike-free with respect to $\hat{u}^*$.

A waveform diagram similar to Fig. 4 is given for $\hat{C}_2$ in Fig. 12. Switching time assumptions are as with Fig. 4, but the line delay is 4 nsec rather than 5 nsec, and transitions are drawn as requiring some time of the order of 0.3 nsec (cf, Fig. 8). Thus, DPP2 is an *undue half-switching* caused by line delays.

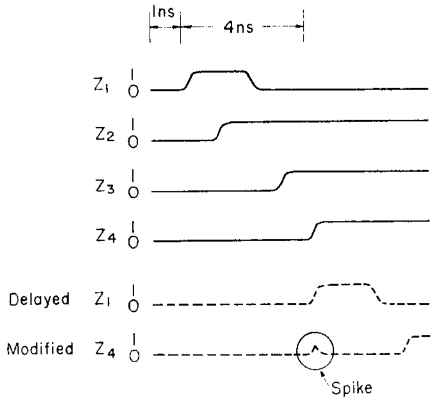

FIG. 12. Example of DPP2: waveforms for $\hat{C}_2$.

Example of DPP3. Let a circuit $\hat{C}_3$ be generated by

$$\begin{cases} z_1' = z_2 + \bar{z}_3 \,, \\ z_2' = \bar{z}_1 z_3 + z_2 \,, \\ z_3' = z_1 + z_3 \,, \end{cases}$$

with the alphabet being $\hat{A}_3 = \{1, 2, 3\}$. Let $\hat{u}$ be (000), and put $\hat{C}_3{}^p = \hat{C}_3(1, 4, \{3\})$. A state diagram each of $\hat{C}_3$ and $\hat{C}_3{}^p$ is shown in Figs. 13(a) and (b), where the initial state is $\hat{u}$ for $\hat{C}_3$, and is the QNE $\hat{u}^p = (0000)$ of $\hat{u}$ for $\hat{C}_3{}^p$. From these diagrams it will be seen that $\hat{C}_3{}^p$ is not sm$[\hat{u}^p]$. In fact, $\hat{u}^pFa^pRb^p$ but $b_4^{p'}, \neq a_4^{p'} \neq b_4{}^p$ for $a^p = (0111)$ and $b^p = (1111)$. Therefore, $\hat{C}_3{}^p$ suffers DP3 with respect to $\hat{u}$. On the other hand,

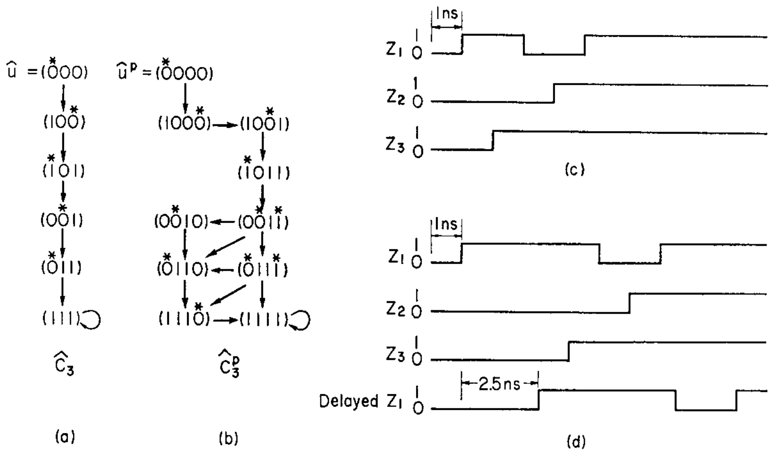

FIG. 13. Example of DPP3: State diagrams of (a) $\hat{C}_3$ and (b) $\hat{C}_3{}^p$; Waveforms for (c) $\hat{C}_3$ and (d) $\hat{C}_3{}^p$.

it can be readily verified, say, by drawing a state diagram that $\hat{C}_3^{(2)} = \hat{C}_3(1, 5, 4, \{3\})$ is spike-free with respect to $\hat{u}^{(2)} = (0000)$, the QNE of $\hat{u}$ from $\hat{C}_3$ onto $\hat{C}_3^{(2)}$. Accordingly, $\hat{C}_3{}^p$ does not suffer DP2 by Theorem (11 : 2), so that DP3 suffered by $\hat{C}_3{}^p$ is in fact DPP3.

Waveforms expected in a physical realization of $\hat{C}_3$ are shown in Fig. 13(c). Again, the switching time of the logical elements is 1 nsec. The waveforms will be modified as shown in Fig. 13(d) if a delay of 2.5 nsec is inserted in the wire feeding the output of the element 1 to the input of the element 3. Here, the delayed signal makes unexpected changes from 1 to 0, and then back to 1, all *after* the element 1 completes its last change to attain the final output signal value 1. These additional changes, however, have no real effects on the action of the logical elements of the circuit. In fact, z_3' becomes insensitive to z_1 once z_3 is switched to 1, and it is after such a change of z_3 that the additional changes could occur in the delayed z_1.

Thus, DPP3 may be characterized by ***unexpected changes of the delayed input signal values occurring only when the logical elements are insensitive to them.*** As far as the delay problem and the problem of signal values are concerned, it is clear that such an effect is harmless. Technologically, this finding seems to be among the most important ones of our investigation.

Another trivial example of DPP3 is found in the modification of $\hat{C}$ sketched in the final portion of Section 5. Recall that the modification differed from $\hat{C}$ only in the don't-care states. The same is true with $\hat{C}_2$.

Discussion of the problem of function realization

In Section 9 we remarked that the informal argument made there for supporting Definition (9 : 1) is not necessarily appropriate to the problem of function realization. This point will now be discussed using $\hat{C}_3{}^p$ above as a convenient vehicle for our arguments.

As explained in Section 0, the problem of function realization asks whether a given network formed by combining a number of simple elements can be used for physically realizing a function f_i of a mathematically defined asynchronous circuit. For example suppose that the function f_i does not depend on z_i. Also suppose that f_i is fairly complex, and a single logical element corresponding to it is not available. Then one would naturally wish to use, say, a conventional three stage network consisting of NOT's, AND's and an OR for representing f_i. However, the new output points of these NOT's and AND's would then incorporate into the circuit new degrees of freedom, and could cause unexpected behavior of the circuit.

Clearly, our theory provides a suitable framework for handling this problem. Thus, we may regard the circuit using a network as above to be an extension of the original (perhaps hypothetical) circuit, in which the node i corresponds to a single element having no internal degrees of freedom. We might then wish to see whether such a method of realization is usable or not, by checking the goodness and spike-freeness of the extension thus formed.

It should be noted, however, that the hidden nodes considered in thus handling the problem of function realization considerably differ in nature from those considered in the delay problem and the problem of signal levels. The former correspond to real logical elements such as AND's and NOT's, while the latter are hypothetical. Thus, for example, a delay element considered in the delay problem is nothing more than a substitute for a small section of wire. See Section 5.

To expose the real implication of this contrast, consider a circuit realizing $\hat{C}_3{}^p$. The element corresponding to the node 4 could experience an energization from 1 to 0, which ceases *before* a corresponding change of its output. Now, a wire has no internal supply of energy, so that a pulse cannot drastically change its width during a travel in it. Thus, if the node 4 of $\hat{C}_3{}^p$ is a wire, its existence will not appreciably affect the average pulse width expected in $\hat{C}_3$, which is of the order of 2 nsec in Fig. 13. In contrast, an amplifier may sharpen the pulse by a mechanism as depicted in Fig. 8 if subjected to a premature termination of energization. Therefore, our node 4, if it is an amplifier, may generate a pulse as narrow as its rise time. The circuit designer cannot be blamed even if he has not expected such a sharp spike in designing the wiring arrangements and other logical elements receiving the output of the amplifier. It is thus concluded that, in the problem of function realization, where the hidden nodes correspond to real elements, partial semimodularity at these nodes may be not insignificant.

There is another, presumably more impartant point: A circuit design of a logical element may implicitly assume that the element be used corresponding to a node at which the circuit is partially semimodular. Thus, for example, a logical element may involve a positive feedback loop in it, and if used in a nonsemimodular environment, then the loop might be kicked into a wrong stable state by a sharp spike produced internally by the above mechanism.

A fuller understanding will be obtained from a study of the following fact (which in itself relates to the problem of function realization). Let a circuit have, among others, nodes 1, 2, 3 such that

$$f_3(z_1, z_2, z_3, \ldots) = z_1 z_2 + z_2 z_3 + z_3 z_1 .$$

Thus, the node 3 corresponds to an idealized memory element often denoted by "C" in the literature [2, 4]. It can be shown that, if our circuit C is partially semimodular with respect to a state u and the node 3, then its extension C^* obtained by replacing the C-element by a combination of two AND's, one OR, and three NAND's sometimes called W. S. Bartky's C-element, is a good spike-free extension of C with respect to a suitable initial state u^* (although C^* is not necessarily totally semimodular). More particularly, our C^* is, if we assume that 4, 5,..., 8 are not in the alphabet A of C, generated by the following system of functions:

$$\begin{cases} f_i^*(z^*) = f_i(z) \quad \text{if} \quad i \neq 3 \quad \text{and} \quad i \in A, \\ f_3^*(z^*) = z_4^* z_5^* , f_4^*(z^*) = \bar{z}_5^* + \bar{z}_6^* , \\ f_5^*(z^*) = \bar{z}_6^* + \bar{z}_7^* , f_6^*(z^*) = \bar{z}_4^* + \bar{z}_8^* , \\ f_7^*(z^*) = z_1^* z_8^* , f_8^*(z^*) = z_2^* + z_7^* . \end{cases}$$

Here, $z = \text{rest}(z^*, C^*, C)$. However, C^* is not necessarily good if C is not partially semimodular with respect to the node 3.

Now, since a perfect C-element is rather difficult to realize, one may wish to design an IC module according to the above to obtain a quasi-C-element usable only for partially semimodular nodes. The use of such a module for realizing a complex function in a spike-free but nonsemimodular extension could be disasterous.

14. Concluding Remarks for Part II

Comments similar to those made in Section 8 can be made on future problems. Thus, it would be rewarding to develop systematic methods for checking whether a given extension is spike-free or not. The problem of extending the Reduction Theorem (11 : 2) is even more important than that of extending Theorem (7 : 7). For, extensions must be good *and* spike-free in most applications (Sections 9 and 13). In addition, DP2 is easier to handle mathematically since it is static in nature (Section 11). It would be wise to study DP2 first. Synthesis problems also exist. It is again interesting to develop a general scheme for avoiding DP2 or DP3 by forming extensions.

We shall close this paper with a few words about the possible modes of interpretation of our theory. In motivating our definitions we often corresponded the nodes of a circuit to logical elements. This does not necessarily mean, however, that our results be usable only in such a context. In fact, the nodes may correspond alternatively to some higher units of computer construction: Our node may be a register, an LSI module, or even a computer in a system of computers operating in an asynchronism. These units may contain a lot of logic internally, which may very well be synchronous, or may be asynchronous but make such assumptions about the relative speed of the logical elements that are foreign to Muller's theory of asynchronous circuits used in this paper as a framework. Rather, it is the sequencing among the units which our theory would be concerned with in this alternative mode of interpretation. The variable z_i would then correspond to a control signal governing the action of the unit. The internal functioning of the units will be excluded from the consideration.

This observation is particularly important in view of the modern trends of computer technology. The basic units of logical design are growing larger and larger. The wiring between individual logical gates will soon be, and to some extent already is, beyond the control of the logical designers. Rather, their task is now being centered around some higher units such as mentioned above. Therefore, the possibility of this alternative interpretation must be kept in mind in estimating the gains and losses of our theory.

In the Appendices, we write "p", "ℓ", "$\ell\ell$", and "$\flat$" for "page", "line", "lines", and "counted from the bottom". The page and line counts refer to those in *J. Comput. System Sci.* **2** (1968), 251–287. The footnote lines are counted separately. In Appendix B, the parenthesized locations give informal introduction to the concepts.

APPENDIX A

Corrections to Part I

Location		Now reads	Should read
p. 252,	footnote 1, ℓ.3♭	circuit	circuits
p. 256,	Fig. 2 (b)	$(1\overset{*}{1}00\overset{*}{0})$	$(\overset{*}{1}100\overset{*}{0})$
p. 263,	ℓ.2	$f^*(z_i^*)$	$f_i^*(z^*)$
p. 264,	ℓ.6♭	$= (i, k_i)_j$	$= a^*(i, k_i)_j$
p. 268,	ℓ.18♭	C^*	$\hat{C}^*$
	ℓ.15♭	C^*	$\hat{C}^*$
p. 269,	ℓ.2	$z_h^* = y_h^*$	$x_h^* = y_h^*$
p. 272,	ℓℓ.11–13 (3 times)	C^*	C^p
	ℓ.13	C^{**}	C^*
p. 278,	ℓ.15	$a^*(0)$’	$a^*(0)$,
	ℓ.16	$b(0)$’	$b(0)$,
	ℓ.12♭	$c(x, j)$	$c(k' - x + 1, j)$
	ℓ.10♭	$q(0)$	$q(k' + 1)$
	ℓ.8♭	$a^{**}(j)_{q(x-1)}$	$a^{**}(j)_{q(x+1)}$
p. 281,	ℓ.9♭	villates	violates
p. 285,	footnote 3, ℓ.4	c and d	b and c
p. 286,	footnote, ℓ.5	$b_j^{*\prime} \neq b_j^* = b_j'$ $b_p^* = b_q^*$	$b_j^{*\prime} = b_j^* \neq b_j'$ $b_p^* \neq b_q^*$

Editor's note: The received date for Part I of this paper, which appeared in Vol. 2, No. 3, was erroneously given as October 23, 1968. The correct date is October 23, 1967.

APPENDIX B

An Alphabetical Index of Terms Introduced in Part I

APPENDIX C

A List of Symbols Used in Part I

Only important symbols are listed. Local symbols, of which the use is restricted to a particular proof, are usually omitted. For Section 7, some symbols listed previously are given new entries. This is done whenever the symbols are given new special meanings valid only in Section 7:

p. 254,	ℓ. 5	C, A, S
	ℓ. 6	S_i
	ℓ. 7	f
	ℓ. 11	f_i, z', z_i'
	ℓ. 12♭	$a\,R_i\,b$
	ℓ. 11♭	$a\,R\,b$
	ℓ. 6♭	$a\,R^*\,b$
p. 255,	ℓ. 13	$aF\,b$
	ℓ. 17	$\hat{C}$
p. 256,	ℓ. 3♭	$aF_T\,b$
p. 258,	ℓ. 18♭	C^*, A^*
	ℓ. 17♭	S_i^*, f^*
p. 259,	ℓ. 13	C^*, C^{**}, C^+
	ℓ. 15	A^*, A^{**}, A^+
	ℓ. 17	$a, b, c,\ldots, u^*, b^*, c^*,\ldots$
	ℓ. 18	$\xi, \eta, \zeta,\ldots, \xi^*, \eta^*, \zeta^*,\ldots$
	ℓ. 19	$\mathrm{ext}(X, Y, Z)$
	ℓ. 20	$\mathrm{rest}(X, Y, Z)$
	ℓ. 6♭	$\hat{C}^{(1)}$
p. 260,	ℓ. 1	$\hat{C}^{(2)}$
p. 263,	ℓ. 4	$C^*(a)$
p. 268,	ℓ. 8	$\pi(i)$
	ℓ. 9	$p(i)$
	ℓ. 10	$r(i)$
	ℓ. 12	$z^{[k]}$

p. 269,	ℓ. 21	$C(p^*, \Delta A, r)$
p. 271,	ℓ. 16	$g(i)$
	ℓ. 4♭	$\pi'(i)$
p. 273,	ℓ. 10	$m(h)$
	ℓ. 11	h'
	ℓ. 12	$\mu(h)$
	ℓ. 13	$\delta(X, Y)$, $\beta(\lambda_1, \lambda_2)$
	ℓ. 14	μ
p. 274,	ℓ. 4♭	$X(h)$
	ℓ. 3♭	$\sigma(h)$, $c(i, j)$
p. 277,	ℓ. 4♭	$C^{(k)}$
	ℓ. 3♭	p, r
	ℓ. 1♭	q
p. 278,	ℓ. 1	$u^{(k)}$
	ℓ. 8	$\hat{a}^*$
	ℓ. 9	$\hat{a}$, $\hat{\xi}^*$
	ℓ. 10	$\hat{a}^*(h)$, $\hat{\ell}$
	ℓ. 11	$\hat{a}(h)$
	ℓ. 12	$\hat{\xi}$
	ℓ. 16	$b(h)$
p. 279,	ℓ. 7	$a^*(h)$, ℓ, H
	ℓ. 8	h_1, h_2
	ℓ. 11	$\hat{b}(h)$
p. 280,	ℓ. 15	$\phi(h)$
	ℓ. 16	$\delta(X, Y)$
p. 281,	ℓ. 5♭	T^*, T
	ℓ. 2♭	$c^*(h)$, λ
p. 282,	ℓ. 5	$d^*(h)$, λ'
	ℓ. 7	$\tilde{a}^*(h)$, $\bar{\xi}^*$
	ℓ. 11	$\beta_x(\lambda_1, \lambda_2)$
p. 283,	ℓ. 3	$\bar{\ell}$
	ℓ. 5	$\bar{b}(h)$
	ℓ. 6	$\bar{\phi}(h)$
p. 284,	ℓ. 17	$\bar{\mu}$
	ℓ. 22	$e^{**}(h)$
	ℓ. 11♭	$g^{**}(h)$
	ℓ. 3♭	T'

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