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Estimation of leakage power and delay in CMOS circuits using parametric variation☆

Preeti Verma[a,*], **Ajay K. Sharma**[a], **Vinay Shankar Pandey**[a], **Arti Noor**[b], **Anand Tanwar**[a]

[a] *National Institute of Technology, Delhi, India*
[b] *Centre for Development of Advance Computing, Noida, U.P., India*

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Summary With the advent of deep-submicron technologies, leakage power dissipation is a major concern for scaling down portable devices that have burst-mode type integrated circuits. In this paper leakage reduction technique HTLCT (High Threshold Leakage Control Transistor) is discussed. Using high threshold transistors at the place of low threshold leakage control transistors, result in more leakage power reduction as compared to LCT (leakage control transistor) technique but at the scarifies of area and delay. Further, analysis of effect of parametric variation on leakage current and propagation delay in CMOS circuits is performed. It is found that the leakage power dissipation increases with increasing temperature, supply voltage and aspect ratio. However, opposite pattern is noticed for the propagation delay. Leakage power dissipation for LCT NAND gate increases up to 14.32%, 6.43% and 36.21% and delay decreases by 22.5%, 42% and 9% for variation of temperature, supply voltage and aspect ratio. Maximum peak of equivalent output noise is obtained as 127.531 nV/Sqrt(Hz) at 400 mHz.

Introduction

To limit the power consumption, it is necessary to reduce the power consumption. This force the innovative developments in low power design. Leakage power dissipation is eventually becoming comparable to dynamic power dissipation in many high performance designs. The very large level of integration results in complication of heat removal, this in turn increases the cost of cooling and packaging. Several researchers have proposed several methods to control the leakage power consumption. Kao and Chandrakasan (2000) used power gating with Multi-Threshold transistors. Ye et al. (1998) show that ''stacking'' of two *off* devices significantly reduces subthreshold leakage compared to a single *off* device. Kumar and Kursun (2006) presented a design methodology based on optimizing the supply voltage

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* Corresponding author. Tel.: +91 9717063730.
E-mail address: preetiverma@nitdelhi.ac.in (P. Verma).

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for temperature variation insensitive circuit. Self Controlled Stacked Transistor (SCST) or Leakage Control Transistor (LCT) technique (Hanchate and Ranganathan, 2004) is the technique to reduce leakage power consumption in CMOS gates without affecting the dynamic power of the circuit. In its 'off' state leakage control transistors acts as dynamic switch to reduce current flow, the operation of the switch is controlled by the current flowing in the branch of switch. stack effect and operation of the Self-Bias transistor is explained in section II, the HTLCT design is explained in section III, while section IV comprise of circuit behaviour with parametric variation. Simulation results and conclusions related to the study about leakage and delay for various cases is discussed in section V.

Stack effect and self bias transistor

In deep submicron technology MOS transistor's subthreshold current varies exponentially with gate-source voltage of the transistor. In CMOS circuits, very small current flows even with zero gate to source voltage (Vgs) and is termed as leakage current. Most of the CMOS logic circuits are designed with series-parallel network of p-channel and n-channel transistors. To measure the DC power consumption, it is essential to analyse the standby current of stacked transistors with zero gate-source voltage. Standby current decreases as the number of stacked transistors in supply to ground path increases. The standby current is negligibly small for more than three transistors in a single stack (Gu and Elmasry, 1999).

$$I_{s1} : I_{s2} : I_{s3} = 1.8 \exp\left(\frac{\eta V_{DD}}{nV_T}\right) : 1.8 : 1$$

where I_{si} ($i = 1, 2, 3$) is leakage current for stacked MOS transistors and i is the number of stacked transistors. The above relation shows that as the number of stacked transistors are increasing, leakage current is decreasing. Self biased transistors have their gate and their drain terminal tied together as a single node. Thus no external control circuitry is required, signal is generated in the circuit itself (Gopalakrishnan and Shiue, 2004).

High Threshold Leakage Control Transistor (HTLCT)

Dual threshold transistors are used to reduce the leakage power consumption within given delay constraints. Leakage control transistors used in self-controlled stacked transistor technique are replaced by transistors having high threshold voltage (Verma and Mishra, 2012). Fig. 1(a) shows the LCT based two input NAND gate circuit having Mt1 and Mt2 as leakage control self bias stack transistors. Gate of p-channel and n-channel MOSFET is connected to the drain terminal of n-channel and p-channel MOSFET respectively. Voltage at drain terminal controls the operation the these leakage control transistors (LCTs) (Hanchate and Ranganathan, 2004). Fig. 1(b) represents the application of high threshold transistor technique on NAND gate circuit. Here Mt1 and Mt2 are the high threshold transistors, one of these two transistors always operates in its cutoff region. This results in an increase of number of OFF transistor from supply voltage to ground path and thus increasing stack effect. The advantage of both high threshold and stack effect is utilized to reduce power consumption.

Circuit behaviour under variation of parameters

Temperature fluctuation

Delay of any path in the circuit depends on the delay of cells and nets. Path delay of digital circuit defines the performance of circuit. It is consistently assumed that the cell delay of digital circuits increases with decreasing

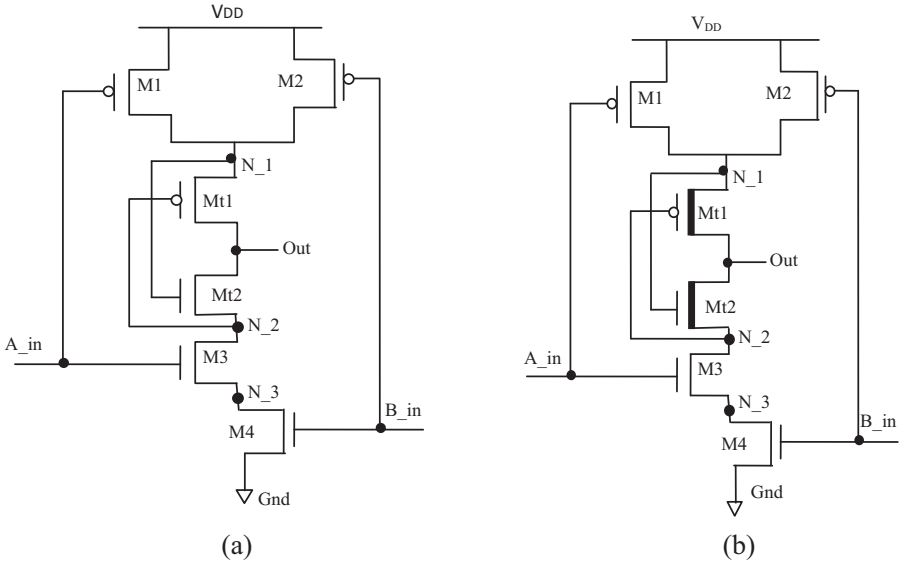

Figure 1 (a) LCT NAND gate and (b) HTLCT based NAND gate.

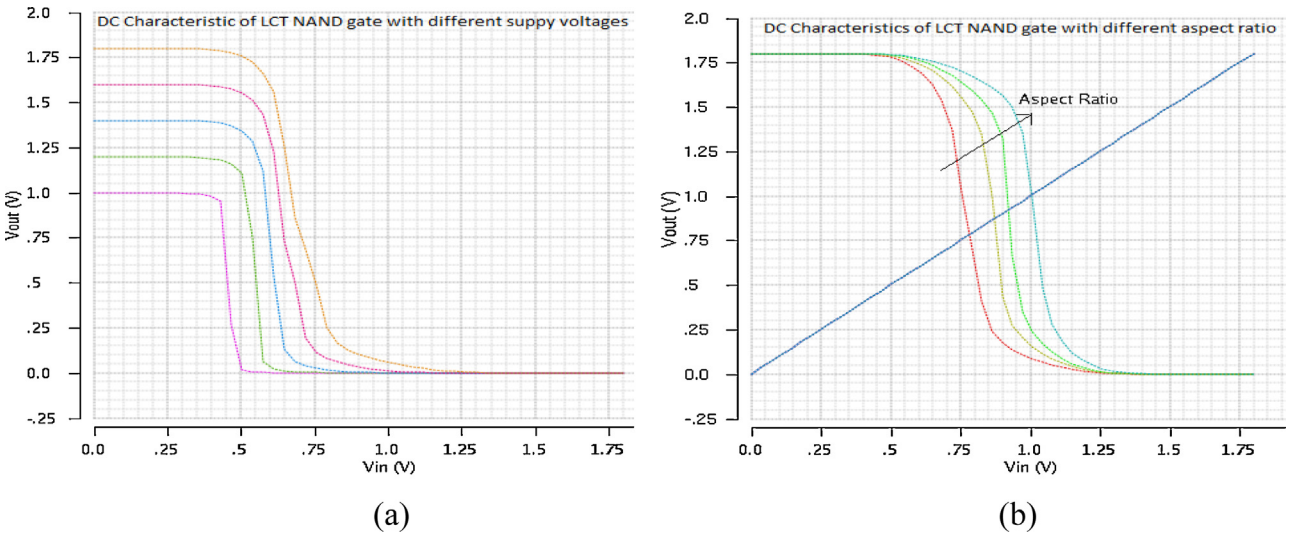

Figure 2 Voltage transfer characteristics of LCT NAND gate (a) with different supply voltages and (b) with varying aspect ratio.

voltage and increasing temperature. But this assumption does not holds for low voltage applications, because increasing temperature may decrease the cell delay. This is due to combativeness of mobility and supply voltage to govern the cell delay. This aberration is termed as inverted temperature dependence (dasdan and hom, 2006). Propagation delay is measured by temperature dependent device parameters and for CMOS circuits it is a function of drain current of active transistor. Low temperature operation results in many advantages like improvement of sub-threshold swing, higher saturation velocity and operation speed, increase of carrier mobility, reduced leakage current, refines electro-migration and heat dissipation (Su et al., 1994).

Effect of supply voltage scaling

Supply voltage scaling was initially adopted for switching power reduction. It is proved to be an effective method for switching power reduction because switching power is quadratically dependent on the supply voltage.

Dynamic Power $P = \alpha C_L V_{DD}^2 f_{clk}$ and

Leakage Power $P = V_{DD}\, I_{sub}$

where α is the activity factor, C_L is the total load capacitance, V_{DD} is supply voltage, and f_{clk} is the clock frequency. Along with switching power consumption, supply voltage scaling also helps in reduction of leakage power consumption, since the subthreshold leakage due to drain induced barrier lowering decreases with the scaling of supply voltage (Fallah and Pedram, 2005).

Effect of aspect ratio

Aspect ratio is defined as the width to length ratio of a transistor. It is an important design parameter. In deep submicron VLSI both width and length are of the order of micrometres. Since the maximum current through transistor is determined by aspect ratio (W/L). Reducing L, allows us to reduce W while maintaining the same aspect ratio. These FET dimensions are combined with the process parameters to get the electrical characteristics of the transistor (Bhavnagarwala et al., 2000).

The channel resistance is given as $R_{channel} = \dfrac{V_{ds}}{I_{ds}}$ and

$$I_{ds} = \mu_0 C_{ox} \left(\frac{W}{L}\right) V_T^2 \exp\left\{\frac{(V_{gs} - V_{th})}{nV_T}\right\}\left\{1 - \exp\left(\frac{-V_{ds}}{VT}\right)\right\}$$

I_{ds} is the drain—source current and is proportional to width of the transistor, thus $R_{channel}$ varies inversely with the width of the transistor.

The area of the gate is defined as A_g

$= LW$ and the gate capacitance is defined as $C_g = C_{ox}WL$

Thus gate capacitance is proportional to the width of the channel. Where C_{ox} is the oxide capacitance per unit area. The channel dimension thus establishes the resistance and capacitance of a FET. The equation of I_{ds} shows that leakage current depends upon width, oxide capacitance and other parameters also. Width of the transistor is directly proportional to the leakage current. This indicates that if the width of the device is increased the leakage current will increase in direct proportion. High speed digital system design deals with the ability to perform calculations very fast (Uyemura, 2009; Chandrakasan and Brodersen, 1999).

Simulation results and conclusion

Leakage power consumption is measured by exciting the circuits with the same set of input vectors.180-nm process technology parameters are taken for the analysis of the circuits. Power is measured and average is done for all the input vectors to obtain the average leakage power dissipations. Fig. 2(a) and (b) shows the voltage transfer characteristics

Table 1 Leakage power and delay of LCT NAND gate and basic NAND GATE.

Process technology 180 nm, supply voltage = 1.8 V					
Parameters		Leakage power (W)		Delay (ps)	
		Basic NAND gate	LCT NAND gate	Basic NAND gate	LCT NAND gate
Temperature variation (°C) at supply voltage = 1.8 V	7	5.29E−08	1.21E−08	23.68	31.84
	27	1.86E−07	6.88E−08	22.61	29.18
	47	2.71E−07	6.96E−08	22.02	28.40
	67	4.15E−07	7.70E−08	21.37	25.28
	87	5.93E−07	8.50E−08	20.89	24.68
Supply voltage variation (V) at temperature = 25 °C	1	5.39E−08	4.42E−09	35.89	51.07
	1.2	6.52E−08	6.01E−09	30.02	41.69
	1.4	6.62E−08	1.61E−08	25.98	36.42
	1.6	1.06E−07	1.79E−08	23.78	32.88
	1.8	1.22E−07	6.88E−08	22.64	29.32
Aspect ratio variation at 1.8 V & 25 °C temperature	η	1.23E−07	6.88E−08	22.64	29.32
	2η	6.87E−07	6.96E−08	21.23	28.76
	4η	9.15E−07	1.90E−07	19.15	26.98

(VTC) of LCT NAND gate with different supply voltages and with varying aspect ratio respectively. Maximum value of output voltage is limited to supply voltage.

Table 1, shows the delay and leakage power dissipation of LCT NAND gate and basic NAND gate with different parameter variations. Temperature is varied from 7 °C to 87 °C, Supply voltage from 1 V to 1.8 V and aspect ratio $\eta = W/L$, $1 \leq \eta \leq 4$. It is found that the leakage power dissipation increases with increasing temperature, supply voltage and aspect ratio. We get an average saving of 34.17% in case of LCT NAND gate and 41.50% for HTLCT NAND gate as compared to standard two input NAND gate. It is also seen that LCT based circuits have less power consumption but more delay as compared to conventional design. Leakage power dissipation for LCT NAND gate increases by 14.32%, 6.43% and 36.21% corresponding to the temperature variation of 7—87 °C, supply voltage from 1 V to 1.8 V and aspect ratio variation from W/L to 4 W/L respectively. The delay of the LCT NAND gate decreases by 22.5%, 42% and 9%, for same parametric variation. For equivalent output noise of LCT NAND gate, maximum peak is obtained as 127.531 nV/Sqrt(Hz) at 400 mHz.

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