ELECTRICAL ENGINEERING

A ZVT–ZCT PWM synchronous buck converter with a simple passive auxiliary circuit for reduction of losses and efficiency enhancement

CrossMark

S. Shiva Kumar *, A.K. Panda, Tejavathu Ramesh

Department of Electrical Engineering, National Institute of Technology, Rourkela, Orissa, India

Abstract In this paper, a Zero-Voltage-Transition (ZVT)–Zero-Current Transition (ZCT) Pulse-width Modulated (PWM) synchronous buck converter (SBC), with a simple passive auxiliary circuit is proposed, which reduces the stresses and improves the efficiency by pacifying the conduction losses compared to a traditional PWM converter, typically suitable for photovoltaic applications. The important design feature of ZVT–ZCT PWM SBC converters is placement of resonant components that mollifies the conduction losses. Due to the ZVT–ZCT, the resonant components with low values are used, thereby resulting in the increase of switching frequency. The ZVT–ZCT operation of the proposed converter is presented through theoretical analysis. The characteristics of the proposed converter are verified with the simulation in the PSIM co-simulated with MATLAB/SIM-ULINK environment and implemented experimentally.

1. Introduction

Nowadays, the DC–DC converters are vastly applied modules, and demand is increasing for high-power density and high-efficiency modules by minimizing the conduction and switching losses. These modules in general the day to day are observed in applications such as laptops, desktop processors for the enhancement of the battery lifetime. Apart from these applications, solar and spacecraft applications demand increase progressively for stressless and more efficient DC–DC modules for maximizing the storage capacity thereby enhancing the power density to improve the battery life to supply in the uneven times.

In 1980, N.R.M. Rao exploited and developed the concept of conventional PWM converter, using the PWM technology to have a control over power switches and to produce step-up or step-down output voltage. The PWM control principle is to control the width of the pulse of a particular switch, switching ON by fixing the switching frequency of a power switch [1]. In the recent years, the synchronous rectifiers are playing the prominent role in reducing the conduction losses,

* Corresponding author at: Dept. of Electrical Engineering, National Institute of Technology Rourkela, Rourkela, Orissa 769008, India. Tel.: +91 9778303525.
E-mail addresses: 512ee1014@nitrkl.ac.in (S. Shiva Kumar), akpanda.ee@gmail.com (A.K. Panda).

as MOSFETs are employed for low-voltage applications [2–4]. In earlier days it was difficult to operate the converter above 1 MHz, but with the advent of resonant switching, the dominant switching frequency loss is reduced. The inclusion of passive auxiliary circuits in synchronous rectifiers for reduction of switching losses implicates tolerable voltage and current stresses on the power switches and also allays the problem of EMI in the converter.

Abundant research has been done using passive snubber circuitry in many DC–DC topologies for improving the efficiency, reduction of switching and conduction losses to recuperate the energy [5–9]. With the advent of passive circuits the converters tend to shrink in terms of cost, size, and also they are proving to be consistent modules having an eminent performance ratio than the active circuits [10–17].

The proposed circuit greatly pacifies the reverse recovery peak current through the diode and turn ON loss of the switch. The demand of higher input voltage, lower output voltages, in turn higher output currents leads to very low duty cycles and mounting the switching losses, thereby resulting in falling off the conversion efficiency. Thus, the efficiency of SBC is optimized by annihilating the switching losses using a soft-switching technique with the assistance of a passive snubber. Because of its low additional conduction losses and its operation which almost replicates as of PWM converters, the soft-switching techniques have allured the attention in the recent times [18–20]. In ZVT–ZCT converters [19–24] generally the auxiliary switch actuates just before the main switch is made active and culminates after it is executed.

The proposed auxiliary circuit has reduced ratings than the main power circuitry as it is activated for a small segment of time during the switching cycle, which provokes least switching losses in the auxiliary circuit thereby improving the converter efficiency as switching losses get diminished. Many other topologies are presented among them; the inclusion of the high-frequency transformers in DC–DC converters has also proved to be well known topologies. However, in these converters by the inclusion of high-frequency isolation transformer, the usage of number of power switches increases usually between four to nine, which accompany to high switching and also conduction losses.

Lowering the switching losses for a low-voltage high-current application with the assistance of a simple passive auxiliary circuit as a snubber with low values of components was not present in the literature [1–27]. The converter that is proposed is mostly suitable in many applications, especially for photovoltaic and spacecraft applications where lossless DC–DC converters with low voltage high current are in much demand. Thus, this paper presents a novel ZVT–ZCT PWM SBC in which by the addition

of resonant auxiliary circuit in the proposed converter that exhibits ZVT, ZCT curtails voltage and current stresses on the main switch and the synchronous switch.

The paper is organized as follows: Section 2 describes about the proposed circuit and its operating modes with theoretical waveforms and equivalent circuits in each mode; Section 3 provides the design procedure of magnetic elements used; Section 4 points out the features of the proposed converter; Section 5 includes the simulation and experimental results that expose the features of the proposed converter; and Section 6 presents the conclusion.

2. Operating principle

2.1. Configuration of proposed circuit and conditions that are assumed to simplify the analysis

Fig. 1 shows the proposed schematic circuit. The proposed converter is the embodiment of the traditional

PWM synchronous buck converter and auxiliary snubber circuit proposed. Proposed auxiliary circuit is comprised of a resonant inductor L_r, a resonant capacitor C_r, a buffer capacitor C_b, a buffer inductor L_b and auxiliary Schottky diodes D_1, D_2. The utilization of body diodes of S_1, S_2 is also done in the proposed converter.

To simplify the analysis of steady-state operations of the proposed converter, the following conditions are assumed in a switching cycle.

1. Constant input voltage V_{in}.
2. Output capacitor C_o and output inductor L_o are large.
3. Diode's reverse recovery time is negligible.
4. Energy storage components or elements are lossless.
5. L_o is very large than resonant inductor L_r.
6. The resonant components or circuits are ideal.

2.2. Modes of operation

In this section, the operating modes of the proposed converter are distinguished into six, considering the different current paths of the elements and switch voltages. The waveforms are presented in Fig. 2, and the operating mode analysis is explained by the current paths shown in Fig. 3.

Mode 1 (t_0–t_1): In this mode 1, main switch, S_1 is switched ON. The current path is as shown in figure. At this stage, as the main switch is ON, it experiences zero current turn ON as it is in the series with resonant inductor L_r, the i_{Lr} current rises and i_{Ds2} current through the body diode of the switch S_2 falls concurrently at the same instant of time. This mode ends at $t = t_1$, i_{Ds2} becomes zero and i_{Lr} reaches $I_{o(avg)}$.

$$i_s(t - t_0) = i_{Lr}(t - t_0) = \frac{V_{in}}{L_r}(t - t_o) \tag{1}$$

$$i_{Ds2}(t - t_0) = I_{o(avg)} - i_{Lr} = I_{o(avg)} - \frac{V_{in}}{L_r}(t - t_o) \tag{2}$$

$$t_{01} = \frac{L_r}{V_{in}} * I_{o(avg)} \tag{3}$$

Mode 2 (t_1–t_2): At the instant when the body diode is OFF, the current passes through the resonant circuit forming L_r, C_r and buffer capacitor C_b. At $t = t_1$, $i_s = i_{Lr} = I_{o(avg)}$, $i_{D2} = 0$, $V_{cr} = 0$ and $V_{cb} = 0$.
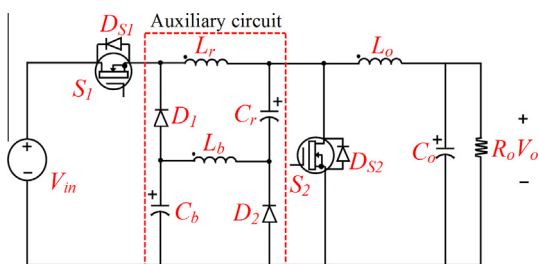

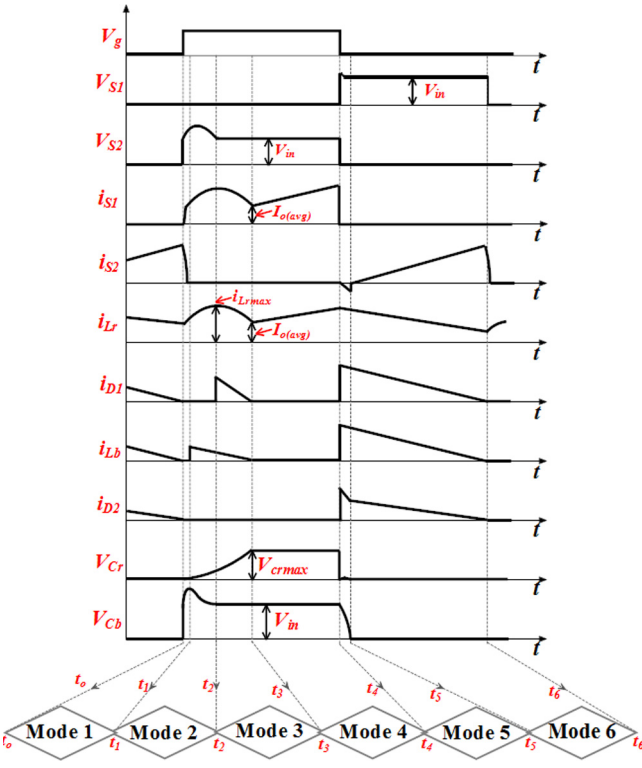**Figure 1**   Proposed ZVT-PWM synchronous buck converter.

Figure 2 Essential theoretical waveforms of proposed converter.

In this interval of time, resonance takes place with the inductors L_r, L_b and C_r, C_b. This mode ends with the C_b charged up to the input voltage.

$$i_{Lr}(t - t_1) = I_{o(avg)} + \frac{V_{in}}{Z_x} \sin \omega_x (t - t_1) \tag{4}$$

$$i_{Lb}(t - t_1) = i_{Lr} - I_{o(avg)} = \frac{V_{in}}{Z_x} \sin \omega_x (t - t_1) \tag{5}$$

$$V_{cr}(t - t_1) = \frac{C_e}{C_r}[-V_{in} \cos \omega_x (t - t_1) + V_{in}] \tag{6}$$

$$V_{cb}(t - t_1) = \frac{C_e}{C_b}[-V_{in} \cos \omega_x (t - t_1) + V_{in}] \tag{7}$$

where $C_e = \frac{C_r C_b}{C_r + C_b}$, $L_e = L_r + L_b$, $\omega_x = \frac{1}{\sqrt{L_e C_e}}$, $Z_x = \sqrt{\frac{L_e}{C_e}}$

Mode 3 (t_2–t_3): In this mode diode, D_1 gets conducted with ZVT at the instant, when V_{cb} equals to V_{in}. At $t = t_2$, $i_{S1} = i_{o(avg)}$, $i_{Lr} = i_{Lr\,max}$, $V_{cb} = V_{cb\,max} = V_{in}$, and $V_{cr} = V_{crx}$ when D_1 gets forward biased a new resonance takes place between L_r, L_b and C_r.

This stage ends when i_{Lr} reaches to load current $I_{o(avg)}$ and C_r is charged to its maximum voltage V_{crm}.

$$i_{Lr}(t - t_2) = (i_{Lr(max)} - I_{o(avg)}) \cos \omega_y (t - t_2)$$
$$- \frac{V_{crm}}{Z_y} \sin \omega_y (t - t_2) + I_{o(avg)} \tag{8}$$

$$i_{Lb}(t - t_2) = i_{Lr}(t - t_2) - I_{o(avg)} = (i_{Lr\,max} - I_{o(avg)}) \cos \omega_y (t - t_2)$$
$$- \frac{V_{crm}}{Z_y} \sin \omega_y (t - t_2) \tag{9}$$

$$V_{cr}(t - t_2) = (i_{Lr(max)} - I_{o(avg)}) Z_y \sin \omega_y (t - t_2)$$
$$+ V_{crm} \cos \omega_y (t - t_2) \tag{10}$$

$$t_{23} = \frac{1}{\omega_y} \tan^{-1} \left(\frac{i_{Lr(max)} - I_{o(avg)}}{V_{crm}} \right) \tag{11}$$

where $\omega_y = \frac{1}{\sqrt{(L_r + L_b) C_r}}$, $Z_y = \sqrt{\frac{L_r + L_b}{C_r}}$

Mode 4 (t_3–t_4): The diodes D_1 and D_2 are not in conduction mode, and only the main switch S_1 and resonant inductor L_r are in conduction. This depicts no resonance at this stage, and now the operational circuit is equivalent to the traditional PWM buck topology.
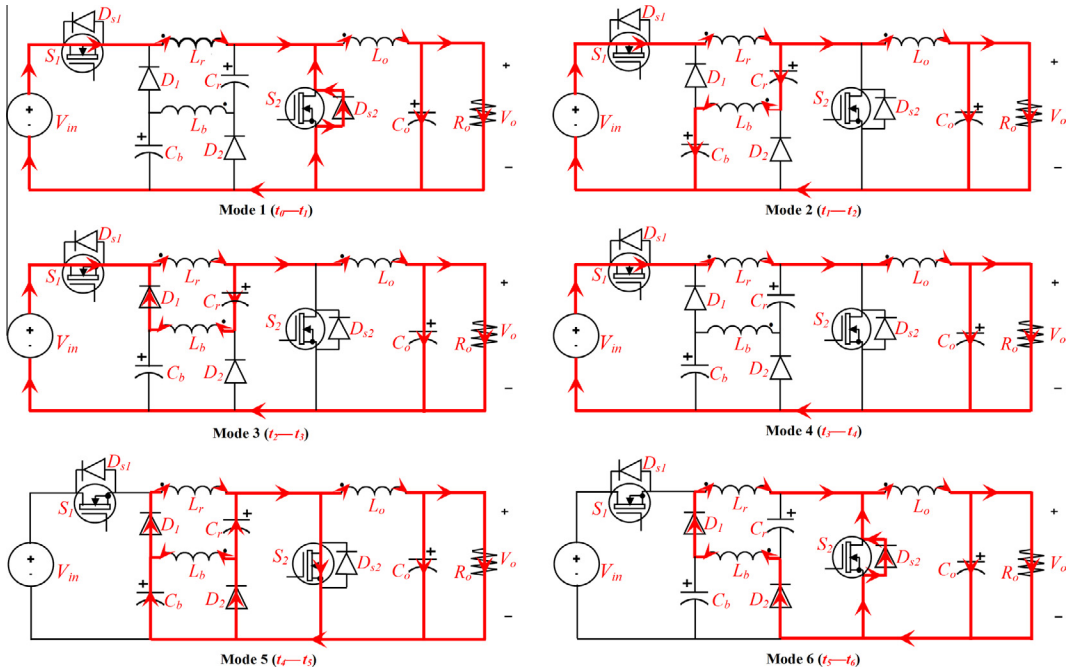
$$i_s = i_{Lr} = \frac{V_{in}}{L_r}(t - t_3) \tag{12}$$

Figure 3 Six operational modes of the proposed ZVT–ZCT PWM SBC converter.

Mode 5 (t_4–t_5): In this mode, main switch, S_1 is OFF under ZVT and at the same time synchronous switch S_2 is ON under ZCT. As S_2 is conducting, the voltage across capacitor C_r is clenched to zero, now the resonance takes place with parallel combination of L_r, L_b and C_b.

$$V_{cr}(t - t_4) = 0$$

$$i_{Lr}(t - t_4) = I_{o(avg)} \cos \omega_z(t - t_4) - \frac{V_{in}}{Z_z} \sin \omega_z(t - t_4) \tag{13}$$

$$V_{cb}(t - t_4) = \frac{V_{in}}{Z_z} \cos \omega_z(t - t_4) - I_{o(avg)}Z_z \sin \omega_z(t - t_4) \tag{14}$$

$$i_{Lb}(t - t_4) = I_{o(avg)} + i_{Lr} \tag{15}$$

where $\omega_z = \frac{1}{\sqrt{(L_r + L_b)C_b}}$, $Z_z = \sqrt{\frac{(L_r + L_b)}{C_b}}$

$$t_{45} = \frac{1}{\omega_z} \tan^{-1} \frac{V_{in}}{I_{o(avg)}Z_z} \tag{16}$$

Mode 6 (t_5–t_6): In this stage, $t = t_5, i_{S1} = 0, i_{Lr} = I_{o(avg)}$, $V_{cr} = 0$ and $V_{cb} = 0$ are the initial conditions for this mode. As i_{Lr} reaches $I_{o(avg)}$, the switch gets turned OFF under ZCT. The preserved energy of L_r and C_r is transferred to the load.

$$V_{cr}(t - t_5) = -\frac{I_o}{C_r}(t - t_5) \tag{17}$$

$$i_{Lr}(t - t_5) = -\frac{V_o}{L_r}(t - t_5) + I_{o(avg)} \tag{18}$$

In this mode, $i_{Lr} = i_{Lb}$.

This mode ends when the body diode of S_2 gets reverse biased and ceases the current through it. The current i_{Lr} reaches minimum value and thereby S_1 gets ON, and repetition of operation continues.

$$t_{56} = \frac{I_{o(avg)}L_r}{V_o} \tag{19}$$

2.3. Output voltage

The output voltage can be evaluated by balancing the volt-Second relationship or by equating the energy relation i.e.,

$$V_o\tau = V_{in}\left[\frac{1}{2}t_{01} + t_{12} + t_{23} + t_{34} + t_{45} + t_{56}\right]$$

$$V_o\tau = V_{in}\left(\frac{1}{2}\frac{I_{o(avg)}L_r}{V_{in}} + \frac{1}{\omega_x}\sin^{-1}\left(\frac{C_r}{C_e} - 1\right) + \frac{1}{\omega_y}\tan^{-1}\right.$$
$$\left. \times\left(\frac{i_{Lr(max)} - I_{o(avg)}}{V_{crm}}\right) + \frac{1}{\omega_z}\tan^{-1}\left(\frac{V_{crm}}{I_{o(avg)}Z_z}\right) + \frac{1}{2}\frac{I_{o(avg)}L_r}{V_o}\right) \tag{20}$$

where $t_{01}, t_{12}, t_{23}, t_{34}, t_{45}, t_{56}$—time periods of mode 1, mode 2, mode 3, mode 4, mode 5, mode 6.

The t_{01} and t_{56} of modes 1 and 6 contain least values compared to other terms in the preceding expression, so they are neglected for making analysis simple.

The voltage conversion ratio will be

$$\frac{V_o}{V_{in}} = \frac{1}{\tau}\left(\frac{1}{\omega_x}\sin^{-1}\left(\frac{C_r}{C_e} - 1\right) + \frac{1}{\omega_y}\sin^{-1}\left(\frac{i_{Lr\,max} - I_{o(avg)}}{V_{crm}}\right)\right.$$
$$\left. + \frac{1}{\omega_z}\tan^{-1}\left(\frac{V_{cr\,max}}{I_{o(avg)}Z_z}\right)\right) \tag{21}$$

where $\tau = \frac{1}{f_s}$ and f_s = switching frequency.

From the aforementioned expression, it is evident that voltage conversion ratio relies upon switching frequency irrespective of the duty ratio.

3. Design procedure

The traditional PWM converter's design is well-known and extensively presented in the literature. Now, it is time to focus on eloquent aspects of designing the auxiliary circuits. The resonant inductor and capacitor design is the most significant part of designing the auxiliary circuit. The auxiliary resonant circuit that is proposed entrusts soft-switching condition for the main switch. The design method is developed, by referring previous literature [18].

(1) Snubber inductor L_r is chosen to allow maximum output current within t_{rise} during the ON time of the main switch.

In this case from Eq. (1)

$$\frac{V_{in}}{L_r}t_{rise} \leqslant I_{o\,max} \tag{22}$$

$t_{rise} \rightarrow$ Rise time of the main switch

The aforementioned equations assist the main switch with ZCS turn-OFF, and ZVS turn-ON of the synchronous switch body diode.

(2) Snubber capacitor C_b is procured such that it discharges from V_{in} to zero with maximum current through it in the time period at the turn-OFF time of the main switch.

In this case, according to (14) and (16)

$$\frac{1}{I_{o\,max}Z_z}V_{in} \geqslant t_{fall} \tag{23}$$

where $Z_z = \sqrt{\frac{L_r}{C_b}}$

(3) Buffer capacitor C_r is selected such that it charges from zero to the value assumed as half of the input voltage. During the turn-OFF time, the buffer capacitor is fed by the energies that are preserved in the snubber inductor and the accumulated charge on snubber capacitor.

The energy balance can be given as

$$\frac{1}{2}C_bV_{in}^2 + \frac{1}{2}C_rV_{crm}^2 = \frac{1}{2}L_rI_{o\,max}^2 \tag{24}$$

The rate of charging of capacitor C_b is greater than the fall time of the main switch S_1, which is equal to the increase at the rate of change of current through inductor L_r.

$$\frac{C_rV_{in}}{I_{Lr\,max} - I_{o(avg)}} \geqslant t_{12} \tag{25}$$

From Eq. (7), t_{12} can be derived as

$$t_{12} = \frac{1}{\omega_x}\sin^{-1}\left(\frac{C_r}{C_e} - 1\right) \tag{26}$$

Solving the above two equations, C_r is derived as

$$\sin\left(\frac{\omega_xC_rV_{in}}{i_{Lr\,max} - I_{o(avg)}}\right) \geqslant \frac{C_r}{C_b} \tag{27}$$

From the aforementioned equations, it is clear that C_r is greater than C_b.

4. Converter postulates

The postulates of the soft switching converter which is proposed are listed as follows

(i) The main switch S_1 is turned ON under ZVT while synchronous switch S_2 is turned OFF under ZVT and turned ON under ZCT, due to the inclusion of L_r, C_r and C_b, L_b. In the circuit, all the diodes are turned ON under ZVT and turned OFF under ZCT.

(ii) The structure of a proposed converter is simple, very low-cost and has satisfactory control.

(iii) The proposed converter, in most of the switching cycles acts as a traditional PWM converter.

(iv) The converter has greater efficiency, and its load range is wider.

(v) The proposed snubber cell can also be placed into other basic PWM DC–DC converters.

5. Simulation and experimental results

The Proposed converter functions with an input voltage $V_{in} = 12$ V, an output voltage $V_o = 4$ V, a load current of 13 A and a switching frequency of 100 kHz. The functional characteristics of the proposed ZVT–ZCT SBC are executed by the simulation using PSIM 7.1 software co-simulated with MATLAB/SIMULINK. Figs. 4a–4c show the simulation results of the proposed converter. In Fig. 4a the voltages of main switch S_1 and synchronous switch S_2 have an overshoot value of 0.5 V compared to the traditional buck converter which is a minor increase in terms of performance point of view. The waveforms that are shown depict a time period of four switching cycles, which is 40 μs in this particular case.

The synchronous buck converter integrated with proposed passive auxiliary circuit has been built and substantiated with experimental results. However there is slight increase of voltage about 0.5 V of main switch S_1 and synchronous switch S_2 as compared to traditional buck converter. The experimental components used in the proposed ZVT–ZCT SBC converter are tabulated in Table 1. As shown in Figs. 5a–5c, the
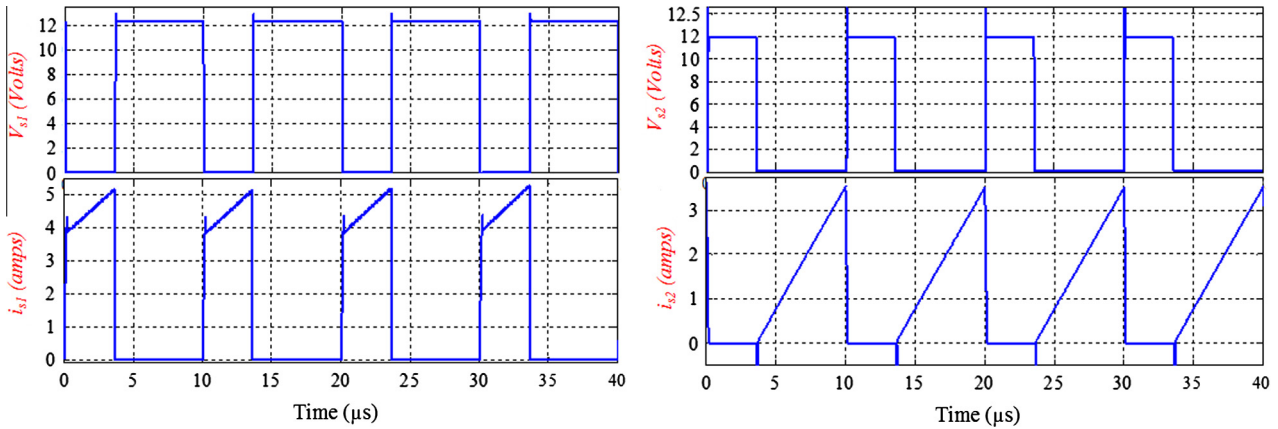

Figure 4a Simulated voltage and current waveforms of main switch S_1 and synchronous switch S_2: V_{s1} and i_{s1}, V_{s2} and i_{s2}.
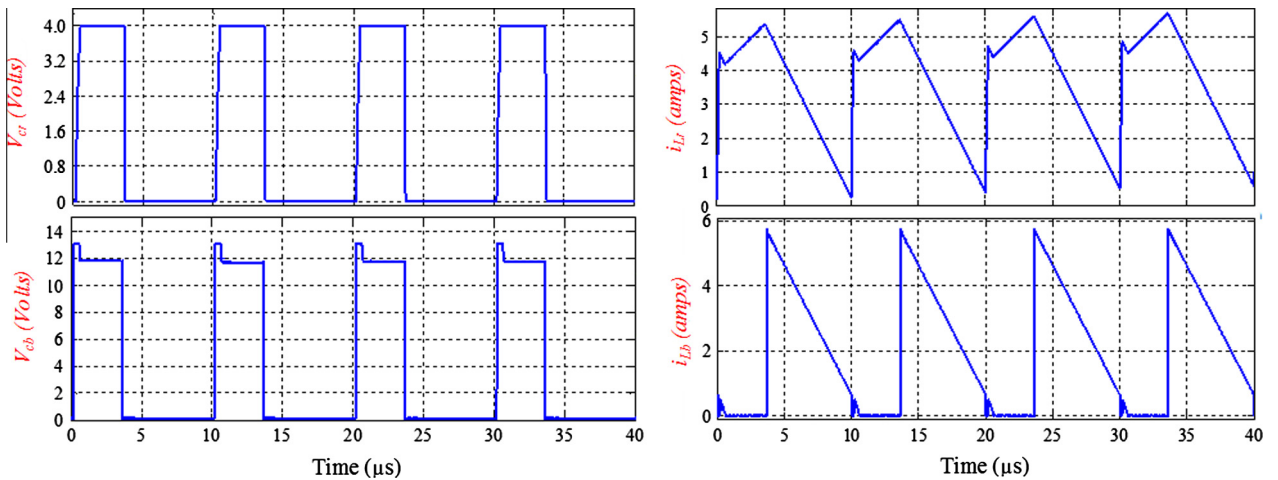

Figure 4b Voltage waveforms of resonant and buffer capacitors C_r, C_b and current waveforms of resonant inductor L_r and inductor L_b.
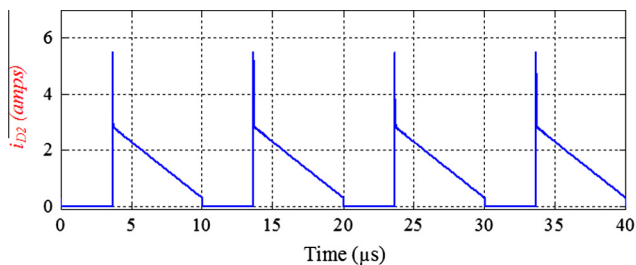
Figure 4c   Current waveform of diode D_2.

Table 1   Components used for proposed converter.

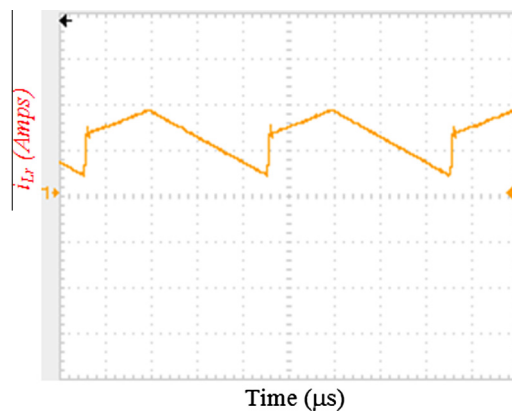| Component	Value/model
Main switch S_1	SUD50N02-04P
Synchronous switch S_2	SUD50N02-04P
Schottky diode, D_1	NXPS20H100C
Schottky diode, D_2	NXPS20H100C
Resonant inductor, L_r	10 nH
Buffer inductor, L_b	4 nH
Resonant capacitor, C_r	2 nF
Buffer capacitor, C_b	1 nF
Output inductor, L_0	10 μH
Output capacitor, C_0	15 μF

Figure 5c   Experimental current waveform of inductor currents i_{Lb}: [i_{Lb}: 3.5 A/Div; time: 2.5 μs/Div].

experimental results depicted are analogous to the obtained simulation results. Fig. 5a shows the voltage and current waveforms of main switch S_1 and synchronous switch S_2 depicting low stresses. However there is slight increase of voltage about 0.5 V of main switch S_1 and synchronous switch S_2 as compared to traditional buck converter. The experimental components employed in the proposed ZVT–ZCT SBC converter are tabulated in Table 1. Fig. 5b shows the voltage waveforms of resonant capacitor V_{cr}, buffer capacitor V_{cb} and current wave-
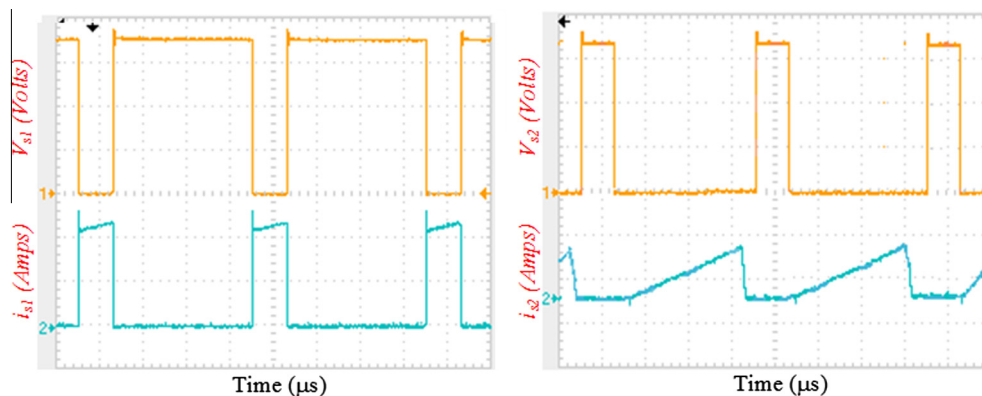

Figure 5a   Experimental voltage and current waveform of main switch S_1: [V_{s1} : 5 V/Div; i_{s1}: 3.5 A/Div; time: 50 μs/Div] and synchronous switch S_2: [V_{s2}: 5 V/Div; i_{s2}: 3.5 A/Div; time: 50 μs/Div].
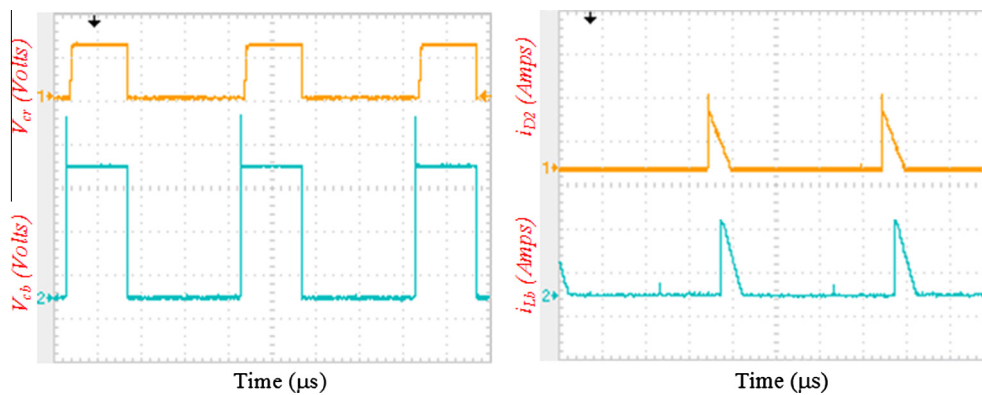

Figure 5b   Experimental voltage and current waveforms of capacitor voltages V_{cr}, V_{cb}: [V_{cr}: 3 V/Div; V_{cb}: 3 V/Div; time: 2.5 μs/Div] and inductor current i_{Lb}, diode current i_{D2}: [i_{Lb}: 3.5 A/Div; i_{D2}: 3.5 A/Div; time: 2.5 μs/Div].
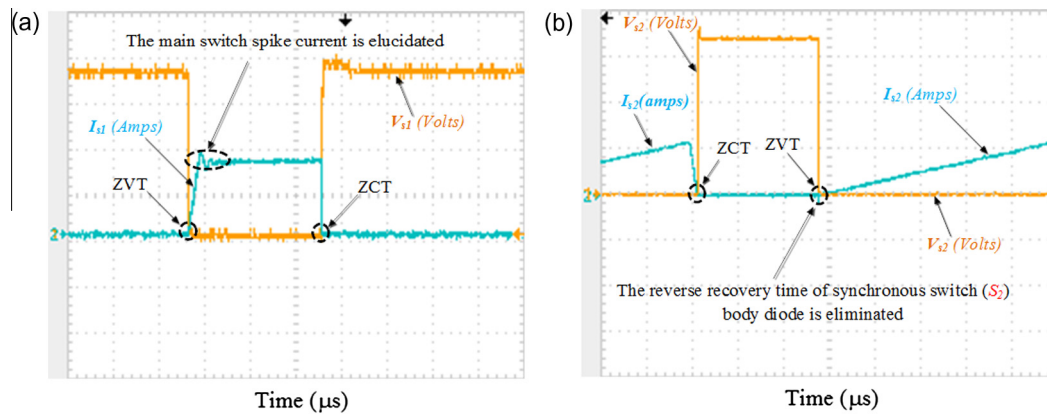
Figure 6 Experimental voltage and current waveforms of: (a) Experimental voltage and current waveform of main switch (S_1): [V_{s1}: 5 V/Div; i_{s1}: 3.5 A/Div; time: 1 μs/Div] exemplifying the ZVT turn ON and ZCT turn OFF of switch. (b) Experimental voltage and current waveform of synchronous switch (S_2): [V_{s2}: 5 V/Div; i_{s2}: 3.5 A/Div; time: 1 μs/Div] exemplifying the ZVT turn ON and ZCT turn OFF of switch.
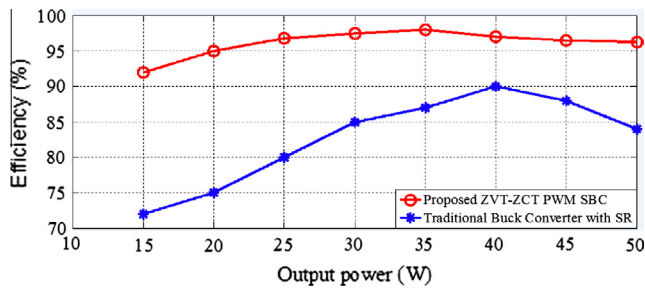

Figure 7 Efficiency curve.

forms of diode current i_{D2}, and buffer inductor i_{Lb}, whereas Fig. 5c shows the current waveform of resonant inductor i_{Lr}. Fig. 6a signifies that the main switch S_1 spike current is plummeted; the waveform is almost equivalent to the traditional buck converter. Consequently, the rating of the main switch required for the buck converter is economized by the introduction of ZVT–ZCT operation. The main switch is turned ON under ZVT and turned OFF with ZCT, due to which the main stream switching losses got diminished. Fig. 6b the synchronous switch S_2 is turned OFF under ZCT and turned ON with

ZVT operation. The reverse recovery (RR) effect due to the body diode of S_2 is almost attenuated.

5.1. Efficiency curve

From Fig. 7, it can be seen that efficiency values of the proposed converter are comparatively higher than the traditional converter with SR. The converter is designed for the maximum output current, and it is accustomed that toward minimum output power efficiency, values decrease. At nearly 70% of output power, the efficiency of the proposed converter rises to about 97% when compared to the counterpart traditional converter whose efficiency is about 87%. The high efficiency of the proposed converter proves the definiteness of the design values.

5.2. Contrast with contemporary topologies

Table 2 shows the comparison of recent topological circuits with the proposed circuit. As shown in the Table 2, the circuits are modern ZVT–ZCT PWM topologies [22–24] are prominent in curtailing the spike of the main switch and diminishing the reverse recovery (RR) problem of the synchronous switch

Table 2 Comparison with contemporary topologies.

|	[23]	[22]	[24]	Proposed converter
Stresses on main switch (spike current, spike voltage)	Low	Low	Low	Very low
Stresses on synchronous switch (spike current, spike voltage)	Low	Low	Low	Eliminated
Reverse recovery of main diode	Eliminated	Eliminated	Replaced by SR	Replaced by SR
Reverse recovery of SR diode	Eliminated	Eliminated	Eliminated	Eliminated
Overhead of ZVT auxiliary circuit				
Switch	1	1	1	0
Diode	2	4	3	2
Inductor	0	1	2	2
Capacitor	1	1	1	2
Coupled inductor	1	1	0	0
Maximum efficiency values at 70% of output power	92.5	94	93	97
Maximum efficiency improvement over hard switching circuit	4.5	5	4.7	5.5

Refs. [22–24].
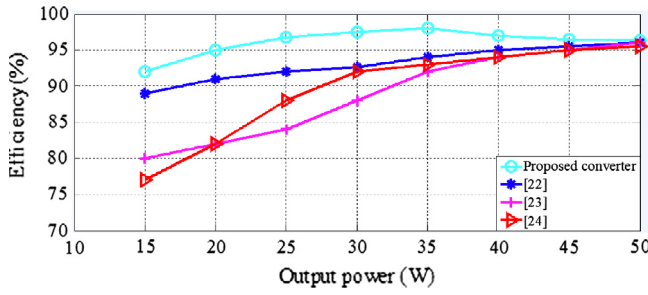
Figure 8 Efficiency curve with contemporary topologies.

body diode. The RR problem of main diode is eliminated. In [22,23] the coupled inductors are used in the auxiliary circuits which in turn expands the volume of the total circuit. The proposed auxiliary circuit not only exceeds the advantages of the contemporary circuits, but also obliges both switches to operate under soft-switching conditions. The RR problem compared to conventional circuits is largely enhanced, beside the efficiency is improved at maximum. Efficiency enhancement relative to the hard-switching converter is shown in Fig. 7. Table 2 and the results proclaim that the proposed auxiliary circuit has accomplished comparable efficiency enhancement over the hard switching circuit to a decent value. The proposed converter does not use the coupled inductors as [22,23] and also it has a simple design with ease of control.

5.3. Efficiency curve with contemporary topologies

From Fig. 8, it can be seen that the efficiency of the proposed ZVT–ZCT SBC is comparatively high, with reference to the contemporary topologies. The values of efficiency declined proceeding toward minimum output power as the design of the proposed converter is for the maximum output current. At 70% of output power, the total efficiency increases to 97% which is greater than other topologies.

6. Conclusion

In this paper, the switching and conduction losses in the SBC were eliminated with the employment of concept of ZVT–ZCT. Apart from the main switch which is turned OFF under ZCT and ON under ZVT, the same replicated on the synchronous switch which is also turned ON under ZVT and OFF under ZCT. The proposed auxiliary circuit integrated with SBC can also be applied to other contemporary circuits; it is proved that the proposed auxiliary circuit achieves ZVT-turn ON and ZCT-turn OFF to both the switches. Particularly, the RR effect of synchronous switch is diminished through the proposed auxiliary circuit, which in turn minimizes the switching losses as correlated with contemporary topologies. Therefore, the switching and conduction losses are diminished; the newly proposed ZVT–ZCT SBC is the most suitable converter for medium and high power than the traditional converter, as it has been observed from the efficiency curve and also contrasted with the contemporary topologies. In addition to this, current and voltage stresses on the main power circuit are reduced immensely, and the auxiliary elements designed such that they deal with permissible voltage and current

values. Furthermore, the proposed converter structure is simple, low-cost and easily controllable.

Appendix A

Derivation of Eqs. (4)–(11), (13)–(16).
    Eqs. (4)–(7):
    As per the equivalent circuit diagram of mode 2 (t_1–t_2) from Fig. 2, the elements L_r, C_r, C_b are in resonance, so the circuit is similar to series-resonant circuit with a capacitor—parallel load. The mode 2 equivalent circuit is redrawn as
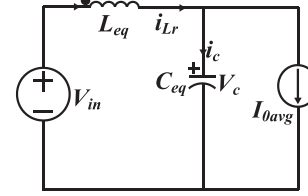
    From the above circuit, $V_c = V_{in} - L_{eq}\frac{di_{Lr}}{dt}$ (i) and $i_{Lr} - i_c = I_{0(avg)}$ (ii).
    Differentiating the above equations yields $i_c = C_{eq}\frac{dv_c}{dt} = -L_{eq}C_{eq}\frac{d^2 i_{Lr}}{dt^2}$. Substituting i_c in equation (ii) yields $\frac{d^2 i_{Lr}}{dt^2} + \omega_x^2 i_{Lr} = \omega_x^2 I_{0avg}$ (iii).
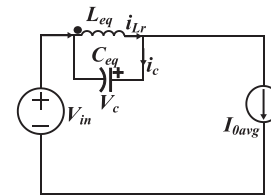   Now the solution of equation (iii) is as follows: $i_{Lr}(t - t_1) = I_{o(avg)} + \frac{V_{in}}{Z_x}\sin\omega_x(t - t_1)$ Eq. (4) and $V_c = \frac{1}{C_{eq}}\int i_c dt$ (iii). Substituting i_c in (iii) yields $V_{cr}(t - t_1) = \frac{C_e}{C_r}[-V_{in}\cos\omega_x(t - t_1) + V_{in}]$ Eq. (6).
    Similarly $V_{cb}(t - t_1) = \frac{C_e}{C_b}[-V_{in}\cos\omega_x(t - t_1) + V_{in}]$ Eq. (7) and from mode 2 equivalent circuit $i_{Lb}(t - t_1) = i_{Lr} - I_{o(avg)}$, which yields $i_{Lb}(t - t_1) = i_{Lr} - I_{o(avg)} = \frac{V_{in}}{Z_x}\sin\omega_x(t - t_1)$ Eq. (5).
    Eqs. (8)–(11):
    As per the equivalent circuit diagram of mode 3(t_1–t_2) from Fig. 2, the elements L_r, L_b, C_r are in resonance and the mode 3 equivalent circuit is redrawn as

    From the above circuit, $i_L + C_{eq}\frac{dV_c}{dt} = I_{0(avg)}$ (i) and $V_c = L_{eq}\frac{di_{Lr}}{dt}$ (ii). The solution for foregoing set of equations is as follows:

$$i_{Lr}(t - t_2) = (i_{Lr(\max)} - I_{o(avg)})\cos\omega_y(t - t_2) - \frac{V_{crm}}{Z_y}\sin\omega_y(t - t_2) + I_{o(avg)} \text{ Eq. (8)}.$$
$$V_{cr}(t - t_2) = (i_{Lr(\max)} - I_{o(avg)})Z_y \sin\omega_y(t - t_2) + V_{crm}\cos\omega_y(t - t_2) \text{ Eq. (10)}.$$
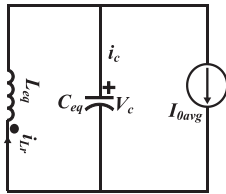$$i_{Lb}(t - t_2) = i_{Lr}(t - t_2) - I_{o(avg)} = (i_{Lr\max} - I_{o(avg)})\cos\omega_y(t - t_2) - \frac{V_{crm}}{Z_y}\sin\omega_y(t - t_2) \text{ Eq. (9)}.$$

At $t = t_3, i_{Lb} = 0$ substituting in Eq. (9) it yields

$t_{23} = \frac{1}{\omega_y} \tan^{-1}\left(\frac{i_{Lr(max)} - I_{o(avg)}}{V_{crm}}\right)$ Eq. (11).

Eqs. (12)–(16):

As per the equivalent circuit diagram of mode 5(t_4–t_5) from Fig. 2, the elements with parallel combination of L_r, L_b and C_b are in resonance, the mode 3 equivalent circuit is redrawn as

From the above circuit, $i_{Lr} + C_{eq}\frac{dV_c}{dt} = I_{0(avg)}$ (i) and $V_c = L_{eq}\frac{di_{Lr}}{dt}$ (ii). The solution from this set of equations is $i_{Lr}(t - t_4) = I_{o(avg)} \cos\omega_z(t - t_4) - \frac{V_{in}}{Z_z}\sin\omega_z(t - t_4)$ Eq. (13).

$V_{cb}(t - t_4) = \frac{V_{in}}{Z_z}\cos\omega_z(t - t_4) - I_{o(avg)}Z_z\sin\omega_z(t - t_4)$ Eq. (14).
$i_{Lb}(t - t_4) = I_{o(avg)} + i_{Lr}$ Eq. (15).

At $t = t_5, V_{cb} = 0$ substituting in Eq. (14) it yields $t_{45} = \frac{1}{\omega_z}\tan^{-1}\frac{V_{in}}{I_{o(avg)}Z_z}$ Eq. (16).

References

[1] Rao NRM, Philips NV. A unifying principle behind switching converters and some new basic configurations. IEEE Trans Consumer Electron 1980;26(1):142–8 [February].

[2] Hua G, Leu CS, Jiang Y, Lee FC. Novel Zero-Current-Transition PWM converters. IEEE Trans Power Electron 1994;9(6):601–6, Nov.

[3] Chen CL, Tseng CJ. Passive lossless snubbers for DC/DC converters. IEE Proc – Circuits, Devices Syst 1998;145(6):396–401 [December].

[4] Wu CC, Young CM. New ZVT PWM DC/DC converters using active snubber. IEEE Trans Aerospace Electronic Syst 2003;39(1):164–75.

[5] Smith KM, Smedley KM. Properties and synthesis of passive snubber for soft-switching boost-type converters. IEEE Trans Power Electron 1999;14(5):890–9, Sep.

[6] Zhang J, Zhang F, Xie X, Jiao D, Qian Z. A novel ZVS DC/DC converter for high power applications. IEEE Trans Power Electron 2004;19(2):420–9 [March].

[7] Bodur H, Bakan AF. A New ZVT–ZCT-PWM DC–DC converter. IEEE Trans Power Electron 2004;19(3):676–84 [May].

[8] Martins MLS, Hey HL. Self-commutated auxiliary circuit ZVT PWM converters. IEEE Trans Power Electron 2004;19(6):1435–45 [November].

[9] Jain N, Jain PK, Joos G. A zero voltage transition boost converter employing a soft switching auxiliary circuit with reduced conduction losses. IEEE Trans Power Electron 2004;19(1):130–9.

[10] Lima FKA, Cruz CMT, Antunes FLM. A Family of turn-on and turn off non dissipative passive snubbers for soft switching single phase rectifier with reduced conduction losses. In: Proc 35th annual IEEE PESC, vol. 5. June 20–25, 2004; p. 3745–50.

[11] Russi JL, Martins MLS, Grundling HA, Peiro H, Pinheiro JR, Hey HL. A unified design criterion for ZVT DC–DC PWM converters with constant auxiliary voltage source. IEEE Trans Ind Electron 2005;52(5):1261–70 [October].

[12] Song TT, Huang N, Ioinovici A. A Family of zero-voltage and zero-current switching (ZVZCS) three-level dc–dc converters with secondary assisted regenerative passive snubber. IEEE Trans Circuits Syst I, Reg Papers 2005;52(11):2473–81.

[13] Borage M, Tiwari S, Kotaiah S. A passive auxiliary circuit achieves zero-voltage-switching in full-bridge converter over entire conversion range. IEEE Lett Power Electron 2005;3(4):141–3 [December].

[14] Schuch L, Rech C, Hey HL, Grundling HA, Peiro H, Pinheiro JR. Analysis and Design of a new high-efficiency bidirectional integrated ZVT PWM converter for DC-bus and battery-bank interface. IEEE Trans Ind Electron 2006;42(5):1321–32 [September].

[15] Huang W, Moschopoulous G. A new family of zero-voltage transition PWM converters with dual active auxiliary circuits. IEEE Trans Power Electron 2006;21(2):370–9 [March].

[16] Russi JL, Martins ML, Hey HL. ZVT DC–DC PWM converters with magnetically coupled auxiliary voltage source: a unifying analysis. Proc IEEE Electric Power Appl 2006;153(4):493–502 [July].

[17] Chuang YC, Ke YL. High-efficiency and low-stress ZVT-PWM DC-to-DC converter for battery charger. IEEE Trans Ind Electron 2008;55(8):3030–7.

[18] Huang W, Gao X, Bassan S, Moschopoulos G. Novel dual auxiliary circuits for ZVT-PWM converters. Can J Electr Comput Eng 2008;33(3):153–60 [Summer/Fall].

[19] Adib E, Farzanehfard H. Zero-voltage transition current-fed full-bridge PWM converter. IEEE Trans Power Electron 2009;24(4):1041–7 [April].

[20] Do HL. A soft – switching DC/DC converter with high voltage gain. IEEE Trans Power Electron 2010;25(5):1193–200 [May].

[21] Pattnaik S, Panda AK, Mahapatra KK. Efficiency improvement of synchronous buck converter by passive auxiliary circuit. IEEE Trans Ind Electron 2010;46(6):2511–7 [November/December].

[22] Bodur H, Cetin S, Yanik G. A new zero-voltage transition pulse width modulated boost converter. IET Power Electron 2011;4(7):827–34 [March].

[23] Urgun S. Zero-voltage transition–zero-current transition pulse width modulation DC–DC buck converter with zero-voltage switching–zero-current switching auxiliary circuit. IET Power Electron 2012;5(5):627–34 [March].

[24] Yang Hong-Tzer, Liao Jian-Tang, Cheng Xiang-Yu. Zero-Voltage-Transition auxiliary circuit with dual resonant tank for DC–DC converters with synchronous rectification. IET Power Electron 2013;6(6):1157–64 [July].

[25] Russi J, Montagner V, Martins M. A simple approach to detect ZVT and determine its time of occurrence for PWM converters. IEEE Trans Ind Electron 2013;60(7):2576–85 [July].

[26] Prasanna UR, Rathore AK, Mazumder SK. Novel zero-current-switching current-fed half-bridge isolated DC/DC converter for fuel-cell-based applications. IEEE Trans Ind Appl 2013;49(4):1658–68.

[27] Chuang Ying-Chun, Ke Yu-Lung, Chuang Hung-Shiang, Wang Yung-Shan. A novel single-switch resonant power converter for renewable energy generation applications. IEEE Trans Ind Appl 2014;50(2):1322–30.

S. Shiva Kumar received the B.Tech. in Electrical Engineering from Gokaraju Rangaraju Institute of Engineering and Technology (GRIET) affiliated to Jawaharlal Nehru Technological University (JNTUK), India, in 2009. He received the M.Tech. in Power Electronics and Drives from Gokaraju Rangaraju Institute of Engineering and Technology affiliated to Jawaharlal Nehru Technological University (JNTUK), India, in 2011 and Pursuing Ph.D. National Institute of Technology Rourkela (NITR). Worked as a faculty in GRIET Hyderabad in 2010 for about a year. His research interest includes analysis and design of high frequency power conversion circuits, power factor correction circuits, SMPS, electric drives, hybrid electric vehicles.

Anup Kumar Panda received the B.Tech. in Electrical Engineering from Sambalpur University, India, in 1987. He received the M.Tech. in Power Electronics and Drives from Indian Institute of Technology, Kharagpur, India, in 1993 and Ph.D. in 2001 from Utkal University. Join as a faculty in IGIT, Sarang in 1990. Served there for eleven years and then join National Institute of Technology, Rourkela, in January 2001 as an assistant professor and currently continuing as a Professor in the Department of Electrical Engineering. He has published over hundred articles in journals and conferences. He has completed two MHRD projects and one NaMPET project. Guided six Ph.D. scholars and currently guiding six scholars in the area of Power Electronics & Drives. His research interest includes analysis and design of high frequency power conversion circuits, power factor correction circuits, power quality improvement in power system and electric drives, Applications of Soft Computing Techniques.

Tejavathu Ramesh was born in Khammam, Andhra Pradesh, India, on April 9, 1987. He received B.Tech. degree in Department of Electrical and Electronics Engineering from G.R.I.E.T affiliated to JNTU Hyderabad, Andhra Pradesh, India, in May 2009 and Masters (M.Tech.) in Department of Electrical Engineering from N.I.T Rourkela, Orissa, India, in May 2011. He is currently working as an Assistant Professor in Department of Electrical Engineering at National Institute of Technology Kurukshetra, and pursuing Ph.D. in Department of Electrical Engineering at National Institute of Technology Rourkela, Orissa, India. His main area of research includes Power electronics and drives, Applications of Soft Computing Techniques, and Artificial Intelligent.