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REVIEW

Implementation of sliding mode controller plus proportional double integral controller for negative output elementary boost converter

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State-space average model

Abstract This article presents a design, output voltage and inductor current regulations of the negative output elementary boost converter (NOEBC) operated in continuous conduction mode (CCM) using sliding mode controller (SMC) plus proportional double integral controller (PDIC). The NOEBC is a dc–dc converter that can provide high voltage transfer gain, high efficiency, and reduced output voltage and inductor current ripples in comparison with the conventional boost converter. Owing to the time varying switched mode operation, the dynamic characteristics of the NOEBC is non-linear and the designed SMC plus PDIC aims at enhancing the dynamic characteristics along with the inductor current and the output voltage regulations of the NOEBC. The proposed SMC is more appropriate to the essentially variable-structured NOEBC when represented in the state-space average based model. Here, the PDIC suppresses the steady state error and excellent initial start-up response of NOEBC in spite of input supply voltage and load resistance variations. The performance of the SMC plus PDIC is verified for its robustness to perform over a broad range of working conditions in MATLAB/Simulink models as well as in the experimental with the comparative study of a SMC plus proportional-integral-controller (PIC). Simulation and experimental results are presented.

Contents

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1. Introduction

In modern days, the dc–dc conversion topologies are developing very fast and it is more suitable for various medical equipment, power supply for telecommunication network, power supply for computer hardware parts, robot systems, defense electronic power supplies, renewable energy power systems, military applications and many more [1–3]. In theoretical point of investigations, the conventional dc–dc converters such as the buck, boost, buck–boost, Cuk, SEPIC (single-ended primary inductor converter), and Zeta converter can achieve a huge voltage transfer gain through an extremely high duty cycle [4–8]. However wretchedly, in real-time practice, which is limited due to the effect of power semiconductor switches, rectifier power diodes and the equivalent series resistance (ESR) of storage elements. Furthermore, the extremely huge duty-cycle operation of the converter will affect in a grave reverse-recovery trouble.

The super-lift technique (SLT) increases the output voltage stage by stage in geometric progression, whereas the negative output elementary boost converter (NOEBC) does the same with a simple formation [9]. The NOEBC is an attractive dc–dc converter topology, which converts the positive dc source voltage into negative dc load voltage. The intensive research has offered most new dc–dc converter circuit topologies reported in [10]. These converters in general have intricate non-linear models with parameters variation. The understandably better candidate in the family of dc–dc converters, the NOEBC, is well thought-out for this article study.

The most famous modeling methods for higher order dc–dc power converters are signal flow graph (SGF) and state space averaging methods [11–14]. The SGF method is simple but dynamic performance is still limited as high frequency components are averaged out in the model. It makes the controller unsuitable for large-signal dynamic control. The small-signal analysis of dc–dc converters with sliding mode controller (SMC) has been reported in [15]. It would not envisage the dynamic response of a switching converter in saturated region and works only for a particular best possible operating condition.

The realization of classical linear controllers namely, pro portional-integral-derivative (PID) or proportional-integral-c ontroller (PIC) for the outer voltage loop control has been well executed in [16–19]. However, these controllers are very sensitive to circuit parameter changes, and transform in working state, input supply voltage and load variations.

The victory of classical non-linear controller lies in performing superior against these problems as dc–dc converters are naturally variable structure systems (VSS) [20]. The controller of NOEBC must manage with their intrinsic nonlinearity and large input voltage and load variations, ensuring stability in any working condition providing fast transient and enhanced dynamic responses. Fundamentally, the SMC utilizes a high-speed switching control law to drive the nonlinear phase trajectory onto a precise surface in the state space, called the sliding or switching surface, and to keep it on this surface for all consequent time [21–25]. All these traditional based SMCs offer many merits over the linear PIC or PID controller; they provide stability even for large line and load variations, robustness, good dynamic response, and simple implementation.

Claim of SMC at variety of sliding surfaces for dc–dc converters has been well reported in [26–31]. However, these conventional SMCs are enforcing the system phase trajectory along with ideal sliding surface at infinite frequency. This is undesirable, as high operating switching frequency will result in excessive switching losses, inductor loss and electromagnetic interference (EMI) noise problems. The reduced order SMC for Cuk' dc–dc converter has been dealt [32]. However, this article discussed about the control of output voltage and supply current for Cuk' converter using SMC, which generated more initial start-up overshoots as well as dynamic operating regions. The reduced order based fixed switching frequency SMC for negative output elementary super lift Luo-converter has been well addressed in [33]. However, this article presented the control of output voltage, inductor current for selection of single integral based sliding surface, which resulted the more steady state error, large start-up settling time of the response, and large overshoots during the dynamic conditions and also difficulty controller implementation. Current distribution control for paralleled POESLLCs and output voltage regulation of NOBC using variable frequency based SMC has been well presented in [34,35]. But, these articles are considered the control of output current and output voltage for sensing all the

state variables of the converters to form the sliding surface for the SMC, which reported the large number of sensor units, and huge number of mathematical calculations are necessary and also huge overshoots during dynamic performance at input supply voltage and load variations. The fixed switching frequency based SMC for higher-order dc–dc converters has been addressed in [36,37]. Yet, this control method has more calculations, complex implementation and needs of larger sensors for sensing the circuit feedback variables. The double integral type of indirect SMC for power converters has been reported [38,39]. The main advantages of the double integral term are added to SMC to reduce the steady state error and also good regulation in comparison with single integral term. Reduced order linear quadratic regulator plus proportional double integral controller for positive output elementary super lift Luo-converter has been presented [40]. The simulation and experimental results of the same double integral controller have produced reduced peak overshoots, quick settling time and excellent steady state error regulation in comparison with single integral controller. These abovementioned problems are overcome by the proposed sliding mode controller (ROSMC) plus proportional double integral controller (PDIC).

Therefore, in this paper, it is proposed to design a variable frequency based SMC plus PDIC for NOEBC operated in continuous conduction mode (CCM). The state-space average model for NOEBC is derived at first and then SMC plus PDIC is developed. The performance of NOEBC with developed SMC plus PDIC is verified at different working regions viz. proper choice of the controller parameters. This initiative and attempt of implementing a SMC for VSS in an analog platform will be a useful contribution to researchers working in this field and also a simple solution to the problems connected with the conventional SMC. The tuning of PDIC parameters is obtained by using Ziegler Nichol's tuning method. The sliding surface coefficient of SMC is found by using state space average model of the NOEBC. The main quality of the designed SMC is implementation with variable frequency (within the boundary limit), simple control structure, small computation, simple implementation and less number of sensing devices.

The organization of this paper is as follows. Section 2 presents the operation and state-space average modeling of the NOEBC. The systematic design procedure of SMC plus PDIC for the NOEBC is presented in Section 3. The simulation and experimental results of the NOEBC and conventional boost converter using SMC plus PDIC and SMC plus PIC at the various operating regions are discussed in Sections 4 and 5. The conclusions are listed in Section 6.

2. Circuit operation and state space average modeling of a NOEBC

2.1. Circuit description and operation of NOEBC

The power circuit diagram of NOEBC is shown in Fig. 1(a). It includes DC input supply voltage V_{in}, capacitor C_1, and input inductor L_1, power switch (n-channel MOSFET) Q, freewheeling diodes D_1, and load resistance R. The efficient voltage step-up capability can be attained by controlling the power switch Q of the NOEBC. It is assumed that all the components are ideal and also the NOEBC operates in CCM. To analyze the operation of the NOEBC, the circuit can be divided into two stages, viz. the switch-ON and the switch-OFF. Fig. 1 (b) and (c) shows the two operation intervals of the NOEBC [9].

In stage 1 operation, when the switch Q is ON, the capacitor C_1 is charged by supply voltage V_{in} and the current through the inductor i_{L1} increases with V_{in}. The equivalent circuit of NOEBC in stage 1 operation is shown in Fig. 1(b). In stage 2 operation, the switch Q is OFF, and i_{L1} decays with the voltage of $-(V_{C1}-V_{in})$. The current i_{L1} flows through the freewheeling diode D_1. The equivalent circuit of NOEBC in stage 2 operation is shown in Fig. 1(c) [9]. The voltage transfer gain is

$$G=\frac{V_o}{V_{in}}=\frac{1}{1-d}-1 \tag{1}$$

2.2. State space averaging analysis of NOEBC

The state variables of NOEBC are the inductor current i_{L1} and the capacitor voltage V_{C1} ($=V_o$) respectively x_1 and x_2. When the switch is in ON state (Fig. 1(b)), the state space equation can be engraved as

$$\begin{cases}\frac{di_{L1}}{dt}=\frac{V_{in}}{L_1}\\ \frac{dV_{C1}}{dt}=\frac{V_{C1}}{C_1R}-\frac{V_{in}}{RC_1}\end{cases}\quad \text{Switch ON} \tag{2}$$

Similarly, when the switch is in OFF state (Fig. 1(c)), the state space equation can be inscribed as

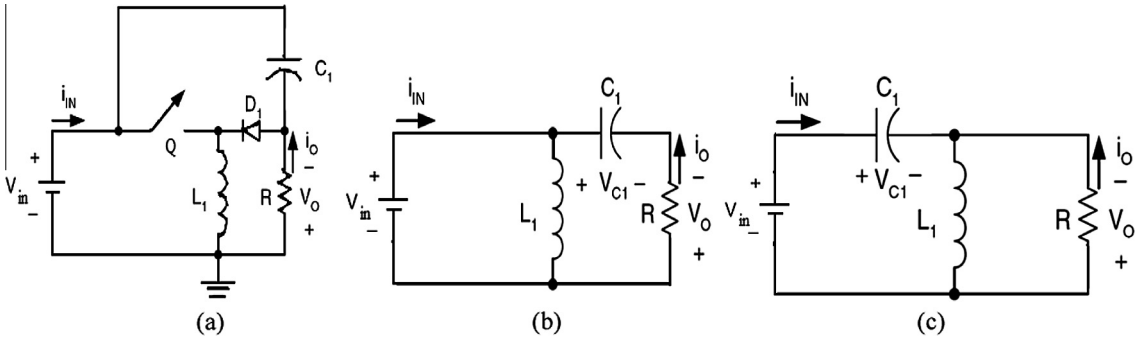


Figure 1 The power circuit of NOEBC, (a) topology, (b) equivalent circuit during stage 1 operation, and (c) equivalent circuit during stage 2 operation.

Table 1 Specifications of the NOEBC.

Parameters name	Symbol	Value
Input voltage	V_{IN}	12 V
Output voltage	V_o	−36 V
Inductor	L_1	100 μH
Capacitors	C_1, C_o	30 μF
Nominal switching frequency	f	100 kHz
Load resistance	R	50 Ω
Output power	P_o	25.92 W
Input power	P_{in}	28.236 W
Average input current	I_{in}	2.283 A
Efficiency	η	94.6%
Average output current	I_o	−0.72 A
Duty ratio	d	0.75
Peak to peak inductor current ripple	Δ_{iL1}	25% of I_{in}
Peak to peak output capacitor ripple voltage	ΔV_o	−0.18 V

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_{in}}{L_1} - \frac{V_{C1}}{L_1} \\ \frac{dV_{C1}}{dt} = \frac{i_{L1}}{C_1} + \frac{V_{in}}{RC_1} - \frac{V_{C1}}{RC_1} \end{cases} \quad \text{Switch OFF} \tag{3}$$

The state-space average modeling of the equivalent circuit of NOEBC with state variables i_{L1} and V_{C1} is given by [11–14].

$$\begin{bmatrix} \dot{i_{L1}} \\ \dot{V_{C1}} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-d}{L_1} \\ \frac{1-d}{C_1} & -\frac{1}{RC_1} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_{C1} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ \frac{1-2d}{RC_1} \end{bmatrix} V_{in} \tag{4}$$

where d is switching duty cycle of the switch or the status of the switch ($d = 1$ when the switch is ON, and $d = 0$ when the switch is OFF).

$$A = \begin{bmatrix} 0 & -\frac{1-d}{L_1} \\ \frac{1-d}{C_1} & -\frac{1}{RC_1} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1-2d}{RC_1} \end{bmatrix} \tag{5}$$

where A and B are averaged system state space matrices.

2.3. Design of NOEBC components

The NOEBC parameters are designed with the following specifications listed in Table 1.

The calculated values of the inductor and capacitor of NOEBC are

$$\begin{aligned} L_1 &= \frac{V_{C1}-V_{in}}{\Delta_{iL1}}(1-d)T = 100\ \mu\text{H} \\ C_o &= \frac{d}{f\Delta V_o}\frac{V_o}{R} = 30\ \mu\text{H} \end{aligned} \tag{6}$$

The design parameters are substituted in (5) and after using the phase-variable transformation, A and B matrices become

$$A = \begin{bmatrix} 0 & -2500 \\ 8333 & -666.67 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{7}$$

3. Design of control techniques

The main aim of this section is to discuss about the design of controller for NOEBC. The controller is divided into two loops namely, an inner current loop which uses SMC for control the inductor current, and an outer voltage control loop utilizing the PDIC to regulate the output voltage and steady state error of NOEBC as shown in Fig. 2(a).

3.1. Design of SMC

Let J be the vector which contains dynamic variables, X be the original state variables and e be the error vector.

$$J = [j_1\ j_2]^T, \quad X = [x_1\ x_2]^T, \quad e = [e_1\ e_2]^T$$

Considered the actual state variables are $x_1 = i_{L1}$, $x_2 = V_o = V_{c1}$, and dynamic reference variables are $j_1 = i_{L1ref}$, $j_2 = V_{oref}$. The error values e_1 and e_2 are expressed as (8)

$$\begin{aligned} e_1 &= [j_1 - x_1] = [i_{L1ref} - i_{L1}] \\ e_2 &= [j_2 - x_2] = [V_{oref} - V_o] \end{aligned} \tag{8}$$

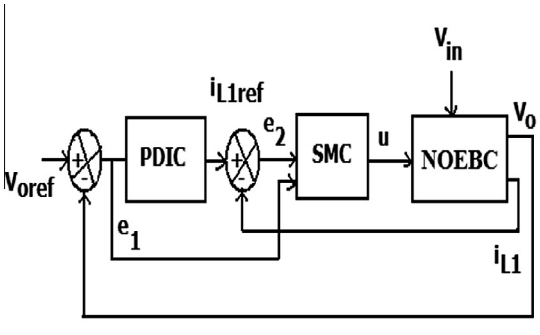
Using the phase-variable transformation to represent the NOEBC while fixing the sliding surface $S(e, t)$, the state space average model of NOEBC in phase-variable form is expressed by (9)

$$\dot{X} = AX + Bu \tag{9}$$

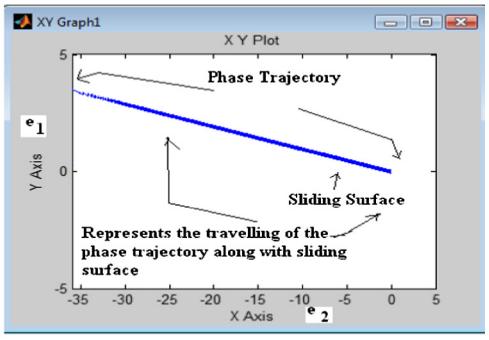
where

$$A = \begin{bmatrix} 0 & -2500 \\ 8333 & -666.67 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{10}$$

For a NOEBC, the $S(e, t)$ is defined as the linear function of tracking vector and is given by (11)



(a)



(b)

Figure 2 Design of SMC plus PDIC, (a) the control scheme for NOEBC and (b) simulated result of region of existence of SM in the phase plane using SMC plus PDIC.

$$S(e,t) = [K][e] \tag{11}$$

where co-efficient vector $K = [K_1 K_2]$ and $K_1, K_2 > 0$.

The aim of the tracking error problem is to keep the error vector (e) always on the sliding surface $S(e, t) = 0$, which implies that the error signal converges exponentially to zero and is engraved by (12).

$$\dot{S}(e,t) = [K][\dot{e}] = 0 \tag{12}$$

On the sliding surface, a second-order system model is reduced to first-order system model with stable linear differential equation. In addition, the system dynamics on the sliding surface is computed only by the controller co-efficient vector K. Thus, the control is insensitive to parameter variations. To calculate the control law, the error state space equation using the nearby states is derived as indicated in (13) and (14).

$$\dot{e} = \dot{J} - \dot{X} \tag{13}$$

$$\dot{e} = \dot{J} - AX + Bu \tag{14}$$

Substituting $X = J$–e in (14), $\dot{e}$ is expressed as

$$\dot{e} = \dot{J} - AJ + Ae - Bu \tag{15}$$

The Filippov's average equivalent switch control u_{eq} that guarantees the $\dot{S}(e,t) = 0$ is found as

$$\dot{S} = Ke = [K]\left[\dot{J} - AJ + Ae - Bu_{eq}\right] = 0 \tag{16}$$

The value of control signal is found by using the above equation and it can be expressed as

$$u_{eq} = [KB]^{-1}K\left[\dot{J} - AJ + Ae\right] \tag{17}$$

Substituting (17) into (15) gives the system error dynamics signals as

$$\dot{e} = \dot{J} - AJ + Ae - B(KB)^{-1}K\left[\dot{J} - AJ + Ae\right]$$

$$\dot{e} = \left[I - B(KB)^{-1}K\right]\left[\dot{J} - AJ + Ae\right] \tag{18}$$

By applying invariance condition $\left[\dot{J} - AJ\right] = 0$, the above equation is simplified as

$$\dot{e} = \left[I - B(KB)^{-1}K\right]Ae = A_{eq}e \tag{19}$$

If $(KB)^{-1}$ exists, the vector K is derived by choosing the eigenvalues of A_{eq} such that it guarantees the asymptotic convergence of error to zero at the desired value. The matrix A_{eq} is selected to satisfy (19) and is expressed as

$$A_{eq} = \begin{bmatrix} -0.904 & 0 \\ 0 & -0.099 \end{bmatrix}$$

The values of matrix K are then found using (19) as

$$K = [K_1 \ K_2] = [1 \ 0.09] \tag{20}$$

Thus, the sliding surface S is given by

$$S = K_1 e_1 + K_2 e_2 \tag{21}$$

Eq. (21) indicates that if the NOEBC works in sliding mode (when $S = 0$, *stability condition*), the dynamics of errors e_1 and e_2 be possible exponentially to zero with a time constant ratio of K_1/K_2. While in the step transient's period, the NOEBC is in reaching mode, and therefore for this use K_1 and K_2 are computed to be in 1 and 0.09, respectively. Also (19) describes the error action under SMC. Once the sliding surface $S(e, t) = Ke$ is designed then the control law for hitting condition is defined as

$$\begin{aligned} u &= M\ sgn(S)x_2 \\ &= Ux_2 \end{aligned} \tag{22}$$

where $\begin{matrix} U = 1 & \text{for } S > \delta \\ U = 0 & \text{for } S < \delta \end{matrix}$.

($U = 1$ when the switch is the conduction subinterval, and $U = 0$ when the diode is the conduction subinterval).

In this work, $\delta = 0.05$ is selected by trial and error iterative method. The (22) is applied to generate the gate pulse to drive power MOSFET of NOEBC, which in turn regulates DC output voltage, steady state error and inductor current.

In this work, M is constant number and equal to unity so that $S\dot{S} < 0$ (*existence condition* is satisfied). The *reaching condition* ensures that the tracking error trajectory is asymptotically involved to $S = 0$ (stability condition). It is shown that Eq. (22) does not depend on the working regions, system parameters and limited disturbances. This is achieved as long as the control input u is more enough to maintain the NOEBC subsystem in sliding mode.

$$S(X) = X_1 + K_2 X_2 \tag{23}$$

where $K^T = [1, K_2]$ is the vector of sliding surface coefficients which correspond to K in (17)

$$\dot{S}(X) = \begin{cases} K^T AX + K^T BU^+ + C^T D, & \text{for } S(X) > 0 \\ K^T AX + K^T BU^+ + C^T D, & \text{for } S(X) < 0 \end{cases} \tag{24}$$

After substituting the values of A, B, C and K, the above equation can be expressed by

$$\begin{aligned} S_1(X) &= 8333K_2X_1 - 2500K_1X_2 - 666.67K_2X_2 \\ S_2(X) &= 8333K_2X_1 - 2500K_1X_2 - 666.67K_2X_2 + K_2 \end{aligned} \tag{25}$$

Equations $S_1(X) = 0$ and $S_2(X) = 0$ define two lines in the state plane with the same slope passing through the origin. These equations represent the sliding surface for switch ON state and OFF state conditions, which are limited to single and the sliding surface of a NOEBC with SMC for K_1, K_2 is shown in Fig. 2(b). From this phase trajectory, it is clearly observed that the suitable value of K_2 controls the dynamic response of the system proficiently. When the phase trajectory is above the sliding surface, the switch is turned off state ($U = 0$) and when the phase trajectory is below the sliding surface, the switch is turned on state ($U = 1$).

3.2. Design of PDIC

A PIC/PDIC is selected for providing the better output voltage regulation in NOEBC. The DC output voltage is sensed and compared with reference output voltage, and error signal is obtained. This error signal is processed by the PIC/PDIC to maintain the output voltage constant and to reduce the steady state error**.** The PIC/PDIC parameters, proportional gain (K_p) and integral times (T_i), are obtained by using Zeigler–Nichols tuning method [16–19].

Table 2 Simulated results – ISE, IAE, ITAE and optimal values of K_p and T_i**s.**

ISE	IAE	ITAE	K_p	T_is (s)
4.352e+5	1.347e+4	3.175e+6	0.013	0.0011 and 0.00133

The transfer function (T.F) model of NOEBC is,

$$\text{T.F} = \frac{-333.3s + 8.333e^7}{s^2 + 666.7s + 2.083e^7} \quad (26)$$

The characteristics equation with proportional control (K) of (26) is expressed by

$$S^2 + (666.7 - 333.3K)s + (K8.33e^7 + 2.083e^7) = 0 \quad (27)$$

The Routh array of equation (27)is

S^2: 1 $\quad K8.33e^7 + 2.083e^7$
S^1: $666.7 - 333.3K$
S^0: $K8.33e^7 + 2.083e^7$

From this Routh array, the range of K for stability is $K8.33e^7 + 2.083e^7 > 0$, $K = -0.33$, $(666.7 - 333.3K) > 0$, $K > 2$, $0 < K < 2$. So, the ultimate critical gain $K_{cr} = 2$. When $K = 2$, the imaginary root since the S^1 row is identically 0. The corresponding auxiliary equation is

$$S^2 + (16.66 + 2.083)e^7 = 0$$

and their corresponding roots are $\omega_n = 13527.7$ rad/s and $P_{cr} = 2 * \text{pi}\omega_n = 84954.26$. After tuning the controller using this method, the NOEBC reaches expected steady state with few oscillations, where the ultimate gain for stability can be found as $K_{cr} = 0.02$ and their corresponding ultimate period as $P_{cr} = 0.0012$ s. Using this method the values of $K_p = K_{cr}/2 = 0.01205$ and integral time $T_i = P_{cr}/.2 = 0.00133$ s are determined. Also, the another value of $T_i = 0.0011$ is found by trial-error method based on the system performance and errors of time. The optimal values of K_p and (T_i)s of PDIC for dc output voltage regulation of NOEBC are obtained by computing the minimum values of integral of square of error (ISE), integral of time of square of error (ITAE) and integral of absolute of error (IAE) using simulation, which are listed in Table 2.

The SMC plus PDIC scheme for a NOEBC converter is shown in Fig. 2(a), where the PDIC voltage controller and SMC act as outer voltage controller and inner current controller, respectively. The input to the PDIC is the output voltage error and the output sets the average reference inductor current for inner current loop. The inputs to the SMC are output voltage error e_1 and the current error e_2. The output of SMC u is the control signal, which in turn sets the new duty ratio of the switching pulse for driving the power MOSFET switch.

4. Simulation results and discussions

The main purpose of this section is to discuss about the simulation results of NOEBC and conventional boost converter with designed control schemes. A SMC plus PIC is used for comparison with the designed SMC plus PDIC. The validation of the system performance is done for five different conditions viz. start-up transient, line variation, load variation, steady state region and also circuit components variations. The MATLAB/Simulink simulation model is performed on the NOEBC circuits with specifications listed in Table 1.

4.1. Start-up transient

Fig. 3(a) shows the dynamic behavior in the start-up region for output voltage of NOEBC for $V_{in} = 12$ V and $R = 50\ \Omega$ using both control schemes. It can be found that output voltage of NOEBC using SMC plus PDIC has a negligible overshoot and quick settling time of 0.003 s, whereas for NOEBC using SMC plus PIC there are overshoots of -0.06 V and long settling time of 0.008 s. Fig. 3(b) shows the output voltage of designed controller for both the NOEBC and conventional boost converters in start-up region. From this figure, it is clearly shown that the output voltage of NOEBC has negligible initial start-up overshoot and quick settling time over the conventional boost converter during the transient region.

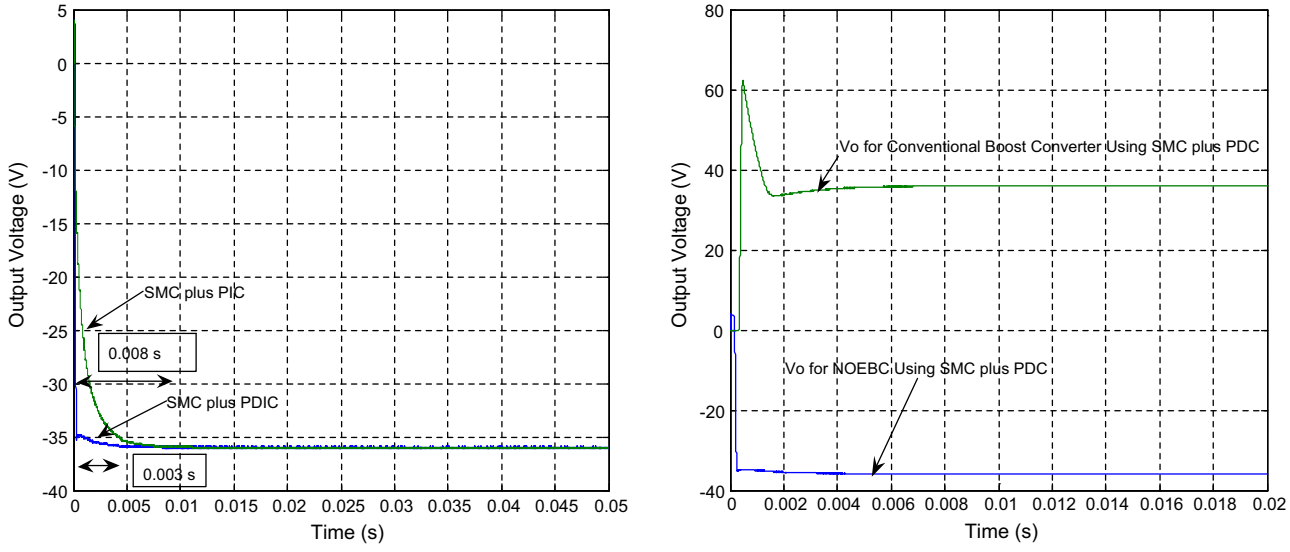


Figure 3 (a) Simulated startup-response of average output voltage of NOEBC for $V_{in} = 12$ V with $R = 50\ \Omega$ using SMC plus PDIC and SMC plus PIC and (b) Simulated response of output voltage of NOEBC and conventional boost converter using SMC plus PDIC.

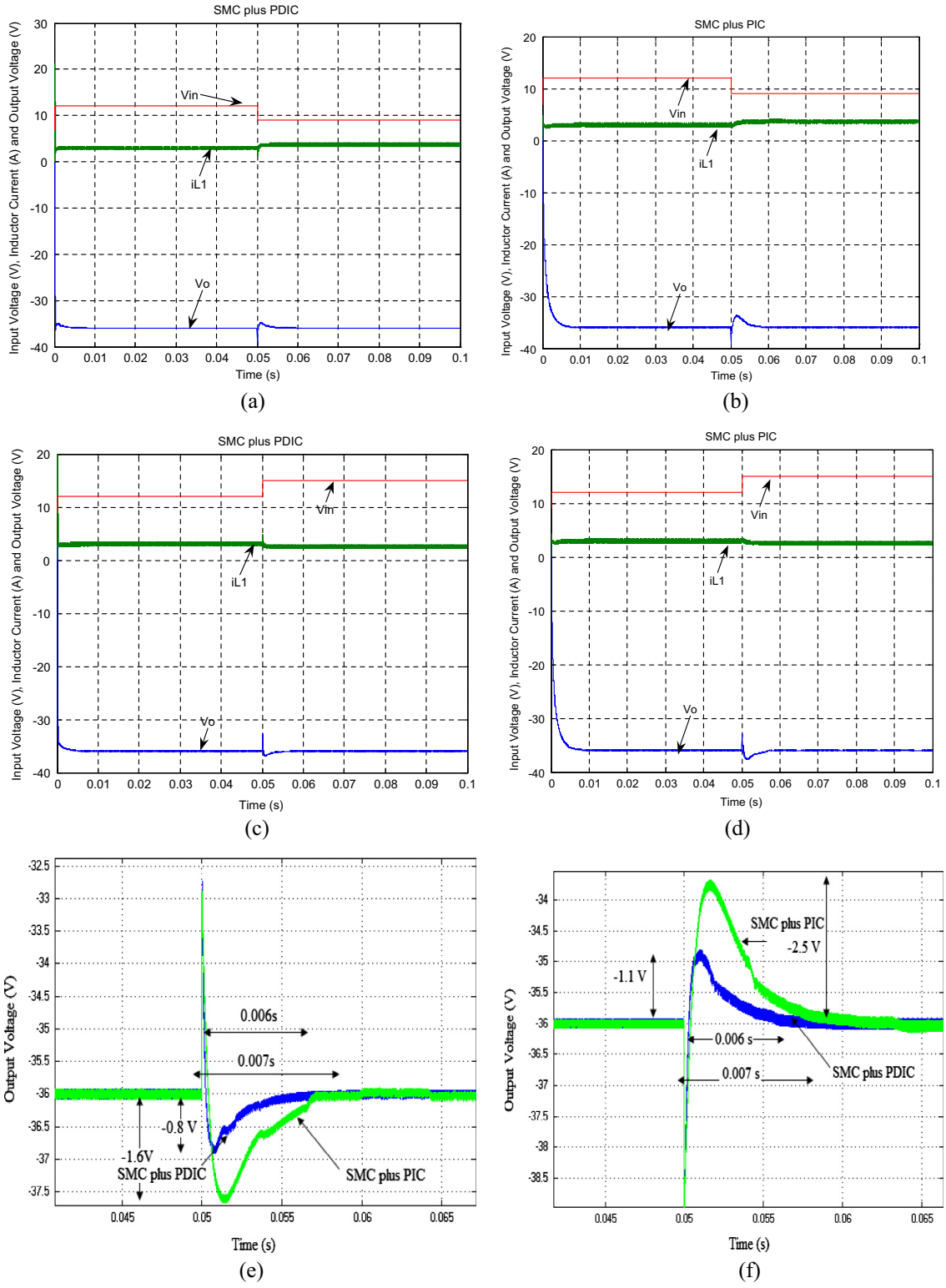


Figure 4 Simulated responses of output voltage, inductor current and input voltage with $R = 50\ \Omega$ at line variation, (a) for input step change from 12 V to 09 V at time of 0.05 s using SMC plus PDIC, (b) for input step change from 12 V to 09 V at time of 0.05 s using SMC plus PIC, (c) for input step change from 12 V to 15 V at time of 0.05 s using SMC plus PDIC, (d) for input step change from 12 V to 15 V at time of 0.05 s using SMC plus PIC, (e) Simulated response (zoomed) of output voltage of NOEBC for input step change from 12 V to 15 V at time of 0.05 s using both controllers, and (f) simulated response of output voltage of NOEBC for input step change from 12 V to 9 V at time of 0.05 s using both controllers.

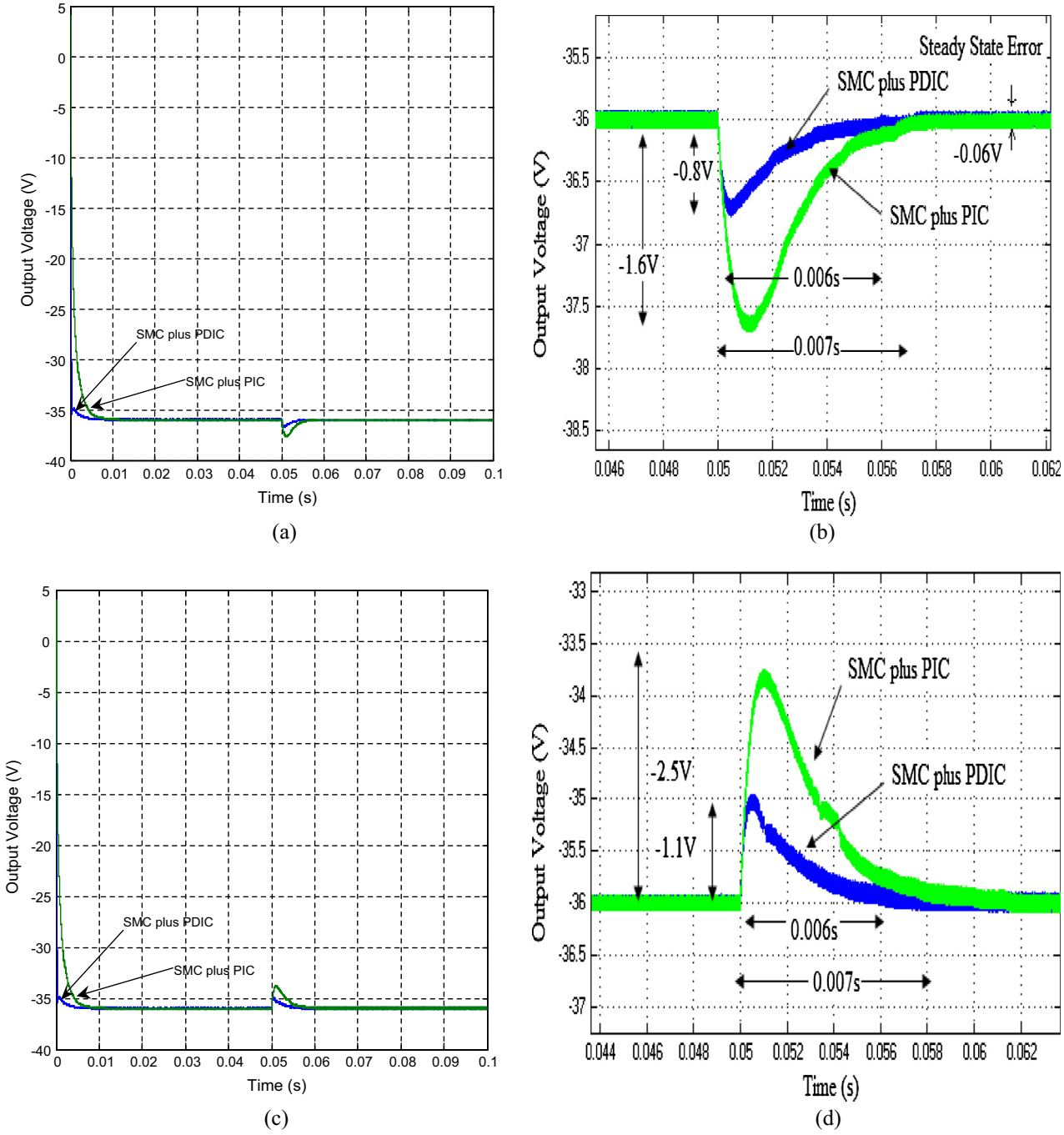


Figure 5 Simulated responses of output voltage of NOEBC with V_{in} = 12 V at load variation (a) when load value takes a step changes from 50 Ω to 60 Ω at time 0.05 s using SMC plus PDIC and SMC plus PIC, (b) zoomed output voltage when load value takes a step changes from 50 Ω to 60 Ω at time 0.05 s using SMC plus PDIC and SMC plus PIC, (c) when load value takes a step changes from 50 Ω to 40 Ω at time 0.05 s using SMC plus PDIC and SMC plus PIC, and (d) zoomed output voltage when load value takes a step changes from 50 Ω to 40 Ω at time 0.05 s using SMC plus PDIC and SMC plus PIC.

4.2. Line variation

Fig. 4(a)–(d) shows the simulation responses of average output voltage and inductor current of NOEBC using both SMC plus PDIC and SMC plus PIC for input voltage step change from 12 V to 15 V and 12 V to 9 V at time of 0.05 s. Fig. 4(e) shows the distended form of response of output voltage of NOEBC for input voltage step change from 12 V to 15 V at time of 0.05 s. From this figure, it is clearly found that simulated responses of output voltage of NOEBC using SMC plus PDIC have overshoot of −0.8 V and settling time of 0.006 s, whereas for NOEBC using SMC plus PIC there are overshoot of −1.6 V and long settling time of 0.007 s. Fig. 4(f) shows the distended response of output voltage of NOEBC for input

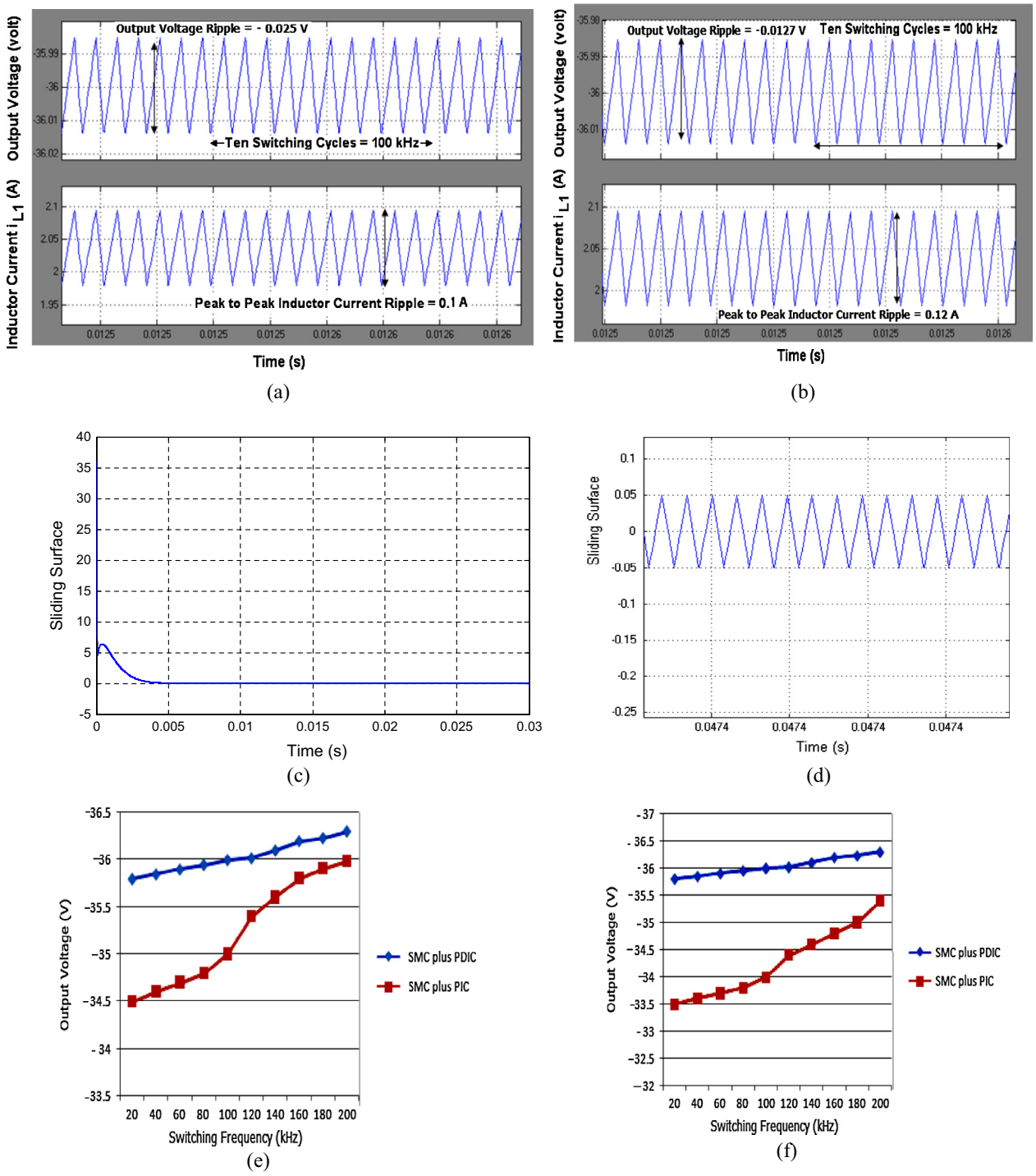


Figure 6 Simulated results of NOEBC in steady state conditions, (a) output voltage and inductor current i_{L1} in steady state condition using SMC plus PDIC, (b) output voltage and inductor current i_{L1} in steady state condition using SMC plus PIC, (c) sliding surface using SMC plus PDIC at $V_{in} = 12$ V and load $R = 50\,\Omega$, (d) sliding surface in steady state condition, (e) plot of steady-state output voltage against switching frequency using both the controllers at minimum output current $I_o = -0.36$ A, and (f) plot of steady-state output voltage against switching frequency using both the controllers at maximum output current $I_o = -1.8$ A.

voltage step change from 12 V to 9 V at time of 0.05 s. It pinpoints that the output voltage using SMC plus PDIC has overshoot of −1.1 V and settling time of 0.006 s, while the SMC plus PIC has the overshoot of −2.5 V and long settling time of 0.007 s. From Fig. 4(a)–(d), it is well evidenced that the simulated results of the designed SMC plus PDIC exhibited an outstanding performance in comparison with a SMC plus PIC under the line variation.

4.3. Load variation

Fig. 5(a) shows the simulation response of output voltage of NOEBC using both control schemes for load step change from 50 Ω to 60 Ω at time of 0.05 s. Fig. 5(b) shows the distended response of output voltage of NOEBC. The SMC plus PDIC possesses the overshoot of −0.8 V with settling time of 0.006 s and negligible steady state error, whereas in SMC plus PIC there are overshoot of −1.6 V with long settling time of 0.007 s and steady state error of −0.06 V. Fig. 5(c) shows the simulation response of output voltage of NOEBC using both control schemes for load step change from 50 Ω to 40 Ω at time of 0.05 s. Fig. 5(d) shows the distended response of output voltage for both the cases. SMC plus PDIC has overshoot of −1.1 V with settling time of 0.006 s and negligible steady state error. The SMC plus PIC has the overshoot, the long settling time and steady state error as −2.5 V, 0.007 s and −0.06 V respectively. Fig. 5(a)–(d) proves that the designed SMC plus PDIC results in less overshoot, quick settling time and negligible steady state error in comparison with a SMC plus PIC under the load variation.

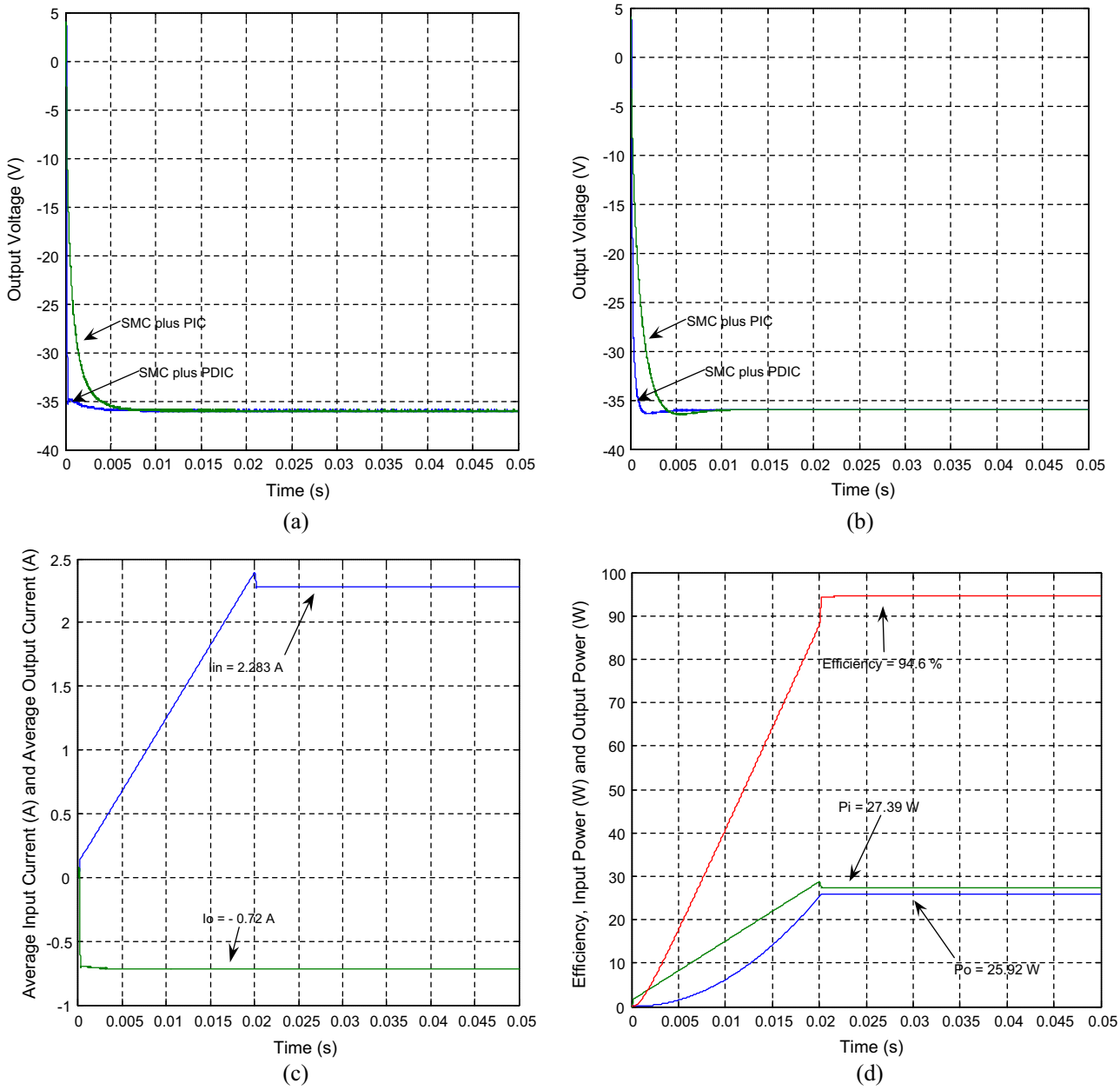
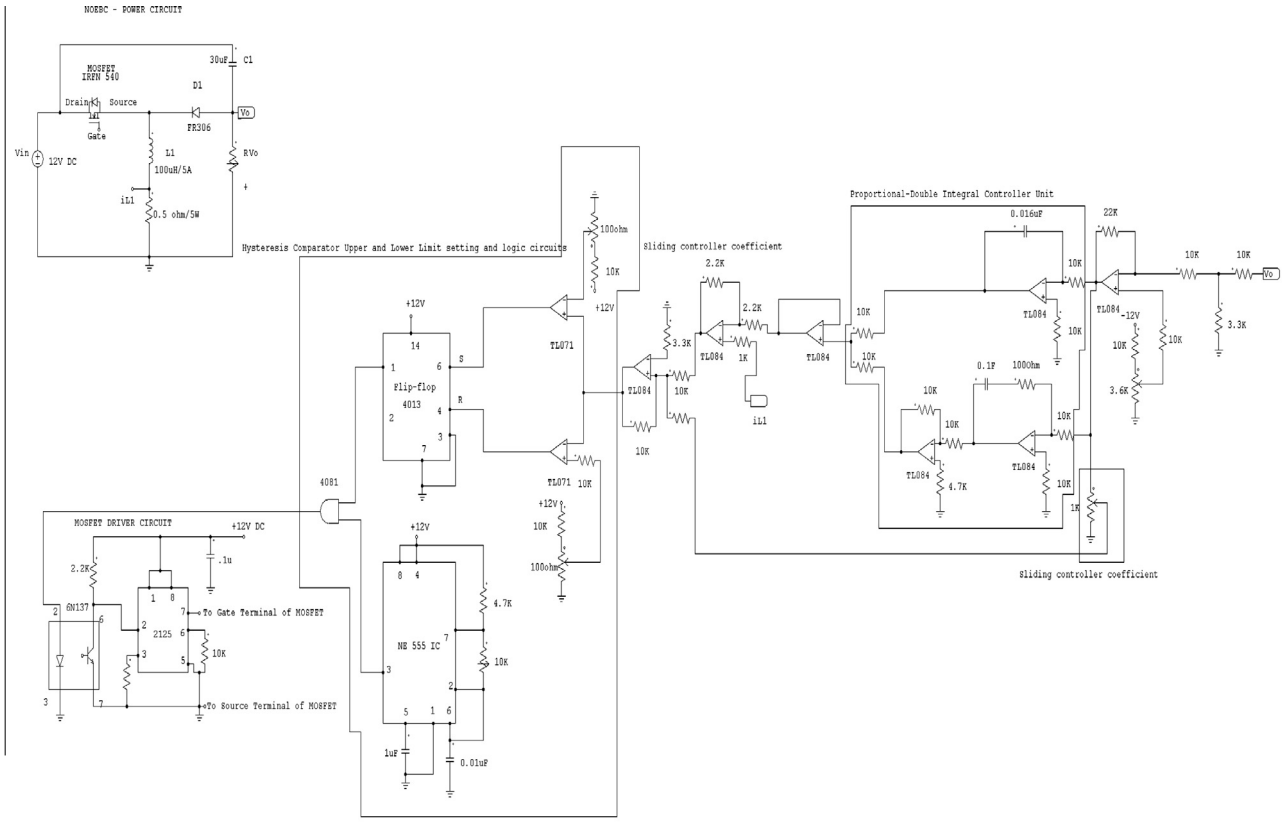
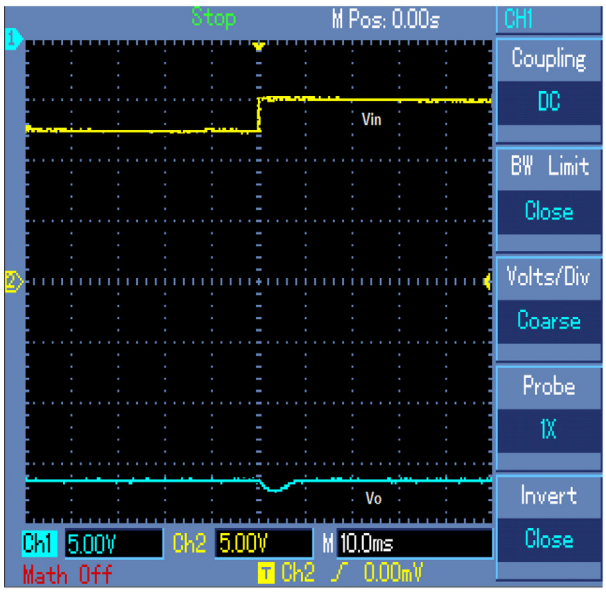


Figure 7 Simulated results of circuit components variation and performance of NOEBC using SMC plus PDIC, (a) output voltage when inductor variation from 100 μH to 150 μH using SMC plus PDIC and SMC plus PIC, (b) output voltage of NOEBC when inductor variation from 30 μF to 100 μF using SMC plus PDIC and SMC plus PIC, (c) average input and output currents using SMC plus PDIC, and (d) input power, output power and efficiency using SMC plus PDIC.



(a)



(b)

(c)

Figure 8 Experimental circuit and results of NOEBC using proposed controller at line variation, (a) Laboratory prototype model of the NOEBC using a SMC plus PDIC in analog platform, (b) output voltage of NOEBC using SMC plus PDIC for input step change from 12 V to 15 V at time 0.05 s with $R = 50\ \Omega$, and (c) output voltage of NOEBC using SMC plus PDIC for input step change from 12 V to 09 V at time 0.05 s with $R = 50\ \Omega$ [Ch1:5V/Div-output voltage and Ch2:5V/Div-input voltage].

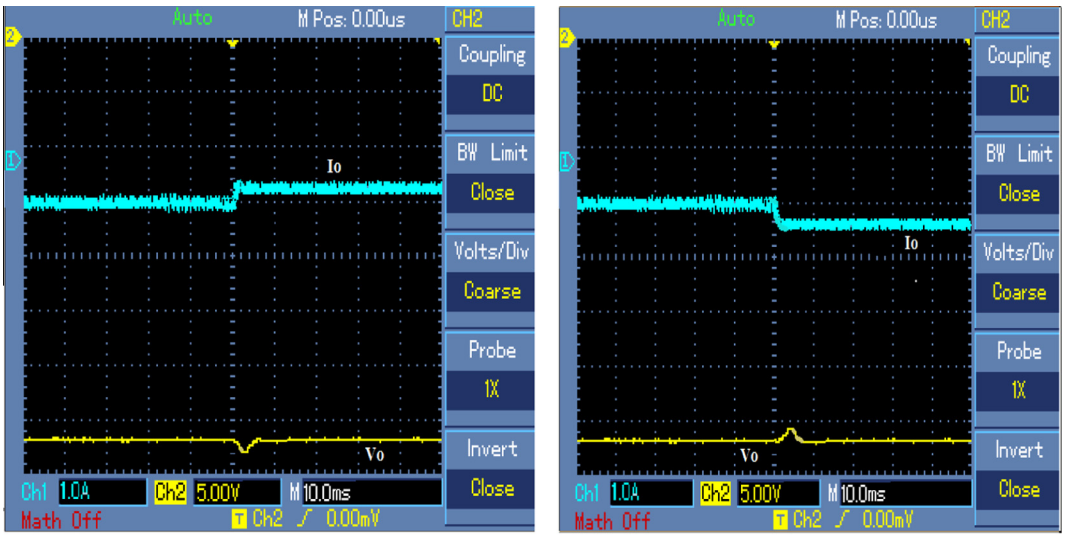


Figure 9 Experimental results of NOEBC using proposed controller at load variation (a) output voltage of NOEBC using SMC plus PDIC for load step change from 50 Ω to 60 Ω at time 0.05 s with V_{in} = 12 V and (b) output voltage of NOEBC using SMC plus PDIC for load step change from 50 Ω to 40 Ω at time 0.05 s with V_{in} = 12 V [Ch1:1A/Div-output voltage and Ch2:5V/Div-input voltage].

4.4. Steady state region

Fig. 6(a) and (b) shows the simulated instantaneous output voltage and the inductor current of NOEBC in the steady state region using both control schemes. It is evident from the figure that the output voltage ripple is very small about −0.025 V/−0.0127 V and the peak to peak inductor ripple current is 0.1 A/0.12 A for the average switching frequency of 100 kHz closer to theoretical designed value listed in Table 1. Fig. 6(c) and (d) shows the simulated response of sliding surface of NOEBC using proposed control scheme, where the sliding surface oscillates around zero. Fig. 6(e) and (f) shows the graphs of the steady-state output voltage against the switching frequency of the NOEBC under the SMC plus PDIC and SMC plus PIC respectively for the minimum and maximum output currents. From this figures, it is clearly found that the proposed controller reduces the steady-state error regulation for all values of switching frequency in comparison with SMC plus PIC.

4.5. Circuit components variations

Fig. 7 shows (a) simulation response of output voltage of a NOEBC using both control schemes for the change in inductor L_1 value from 100 μH to 150 μH. It could be found that the change does not influence the NOEBC behaviors due to proficient designed SMC plus PDIC in comparison with SMC plus PIC. An interesting result is illustrated in Fig. 7(b). It shows the simulation response of output voltage of a NOEBC with both control schemes for the variation in capacitor values from 30 μF to 100 μF. It can be seen that the proposed SMC plus PDIC is very successful in suppressing effect of capacitance variation except a negligible output voltage ripple and quick settling time in comparison with SMC plus PIC. From Fig. 7 (c) and (d), it is evident that the average input/output currents, input/output powers and efficiency of NOEBC using proposed control scheme are 2.283 A/−0.72 A, 27.39 W/25.92 W and 94.6% respectively and match with the theoretical design presented in Table 1.

5. Experimental results

The main purpose of this section is to discuss about the experimental results of NOEBC with designed SMC plus PDIC. The validation of the system performance is done for different conditions. The laboratory prototype model is performed on the NOEBC circuits with same simulation specifications. The laboratory prototype model of NOEBC using proposed control circuits is shown in Fig. 8(a). The parameters of the power circuits are as follows:

Q	IRFN 540 (MOSFET);
D_1	FR306 (diodes);
C_1	30 μF/100 V (electrolytic and plain polyester type);
L_1	100 μH/5 A (ferrite core)

The parameters of the controller are as follows: K_1 = 1, K_2 = 0.09, δ = 0.05, K_p = 0.013 and T_i = 0.0011 s and 0.0013 as calculated in the previous section. The designed SMC plus PDIC is implemented in analog platform as shown in Fig. 8(a) and its operation is as follows: the inductor current and the output voltage V_o of NOEBC are sensed by using shunt resistance, and potential dividing resistances. The measured output of NOEBC is compared with reference output voltage signals by using TL084 operational amplifier, it gives the error signal, this error signal is processed through the PDIC to generate the reference current which is compared with the measured circuit inductor current and this will give the current error signal. Further, both the current and voltage errors are processed through the sliding surface coefficients and its

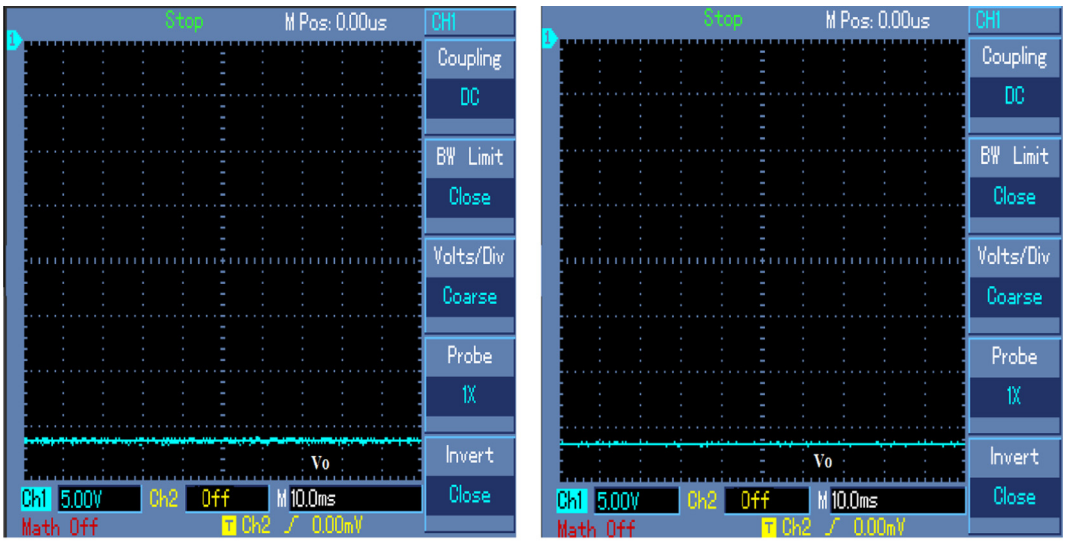


Figure 10 Experimental output voltage response of circuit components variation of NOEBC using SMC plus PDIC (a) for inductor variation from 100 μH to 150 μH and (b) for capacitor variation from 30 μF to 100 μF.

outputs are summed to form the sliding surface using TL084 operational amplifiers. This sliding surface signals are compared using TL071 to generate the pulse width modulated (PWM) gate drive control signal. The hysteresis upper and lower limits are implemented by using the TL071, flip-flop 4013, logical AND gate, and NE 555 IC (used to generate and set the 100 kHz operating frequency for proposed system). The generated gate signal is passed through the op-isolator (6N137), driver IC 2125, and resistances and capacitor arrangement associated in the gate terminal. The output of the driver is directly connected to the gate of the MOSFET (IRFN 540) as shown in Fig. 8(a). Using the SMC plus PDIC, the switching frequency of gate pulse is varied to regulate the output voltage and inductor current and enhance the transient, reduced steady state errors and proficient dynamic performances of NOEBC.

5.1. Line variation

Fig. 8(b) shows the experimental response of output voltage of NOEBC using SMC plus PDIC for input voltage step change from 12 V to 15 V at time of 0.05 s. From this figure, it is clearly found that experimental response of output voltage of NOEBC using SMC plus PDIC has overshoot of −1 V and settling time of 0.006 s. Fig. 8(c) shows the experimental response of output voltage of NOEBC using SMC plus PDIC for input voltage step change from 12 V to 9 V at time of 0.05 s. Experimental response of output voltage of NOEBC using SMC plus PDIC has overshoot of −1.23 V and settling time of 0.006 s.

5.2. Load variation

Fig. 9(a) shows the experimental response of output voltage of NOEBC using proposed control scheme for load step change from 50 Ω to 60 Ω at time of 0.05 s. It could be seen that the experimental result of output voltage of NOEBC using SMC plus PDIC has a small overshoot of −0.72 V with settling time of 0.006 s and negligible steady state error. Fig. 9(b) shows the experimental response of output voltage of NOEBC using proposed control scheme for load step change 50–40 Ω at time of 0.05 s. It could be seen that the experimental result of output

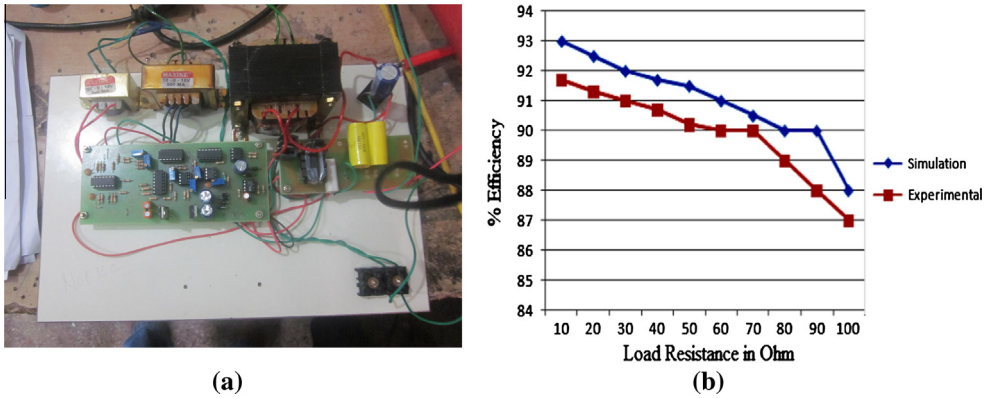


Figure 11 Photograph model and performance of NOEBC using SMC plus PDIC, (a) photograph of laboratory prototype set-up model and (b) simulation and experimental results of % efficiency at various load conditions.

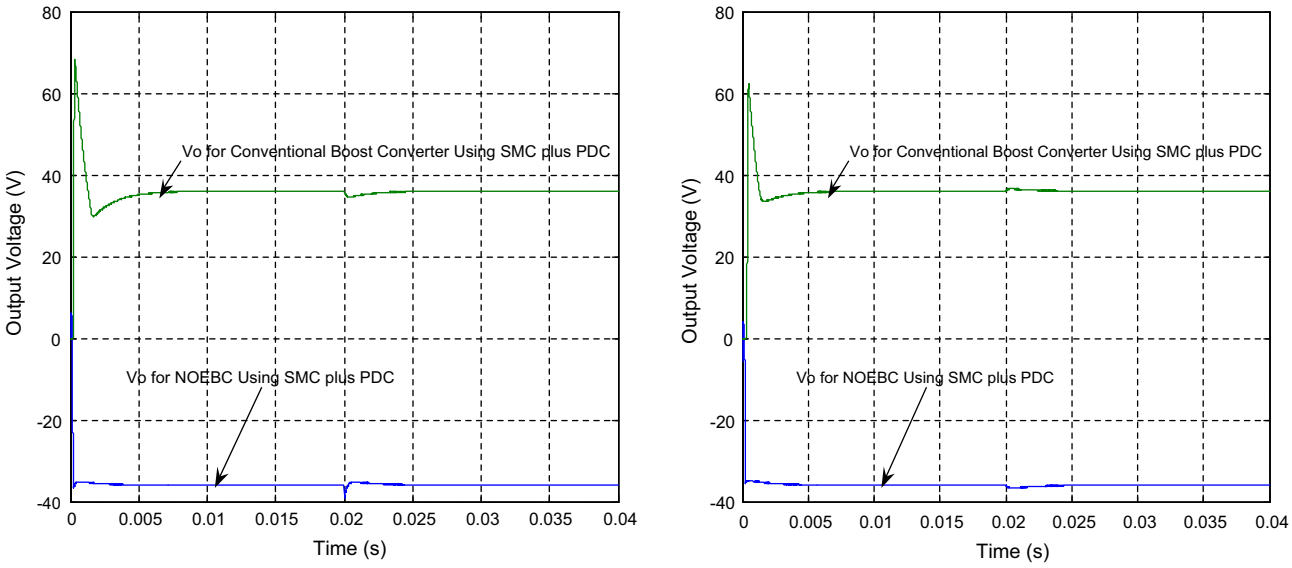


Figure 12 Simulated output voltage of NOEBC and conventional boost converter using SMC plus PDIC, (a) input supply voltage variation from 12 V to 15 V at time of 0.02 s and (b) load resistance variation from 50 Ω to 60 Ω.

voltage of NOEBC using SMC plus PDIC has a small overshoot of −0.88 V with settling time of 0.006 s and negligible steady state error.

5.3. Circuit components variation

Fig. 10 shows (a) experimental response of output voltage of a NOEBC using proposed controller for inductor L_1 variation from 100 μH to 150 μH. It could be found that the change does not influence the NOEBC behaviors due to proficient designed SMC plus PDIC. An interesting result is illustrated in Fig. 10 (b). It shows the experimental response of output voltage of a NOEBC using SMC plus PDIC for the variation in capacitor values from 30 μF to 100 μF. From these figures it is clearly found that the proposed SMC plus PDIC is very successful in suppressing effect of capacitance variation except a negligible output voltage ripple and quick settling time.

Fig. 11(a) indicates the photograph of laboratory prototype set-up model of NOEBC using designed controller. Fig. 11(b) indicates that simulation and experimental results of percentage efficiency of NOEBC using SMC plus PDIC at various load conditions. The efficiency of NOEBC using SMC plus PDIC is improved from 87% to 93% at various load conditions.

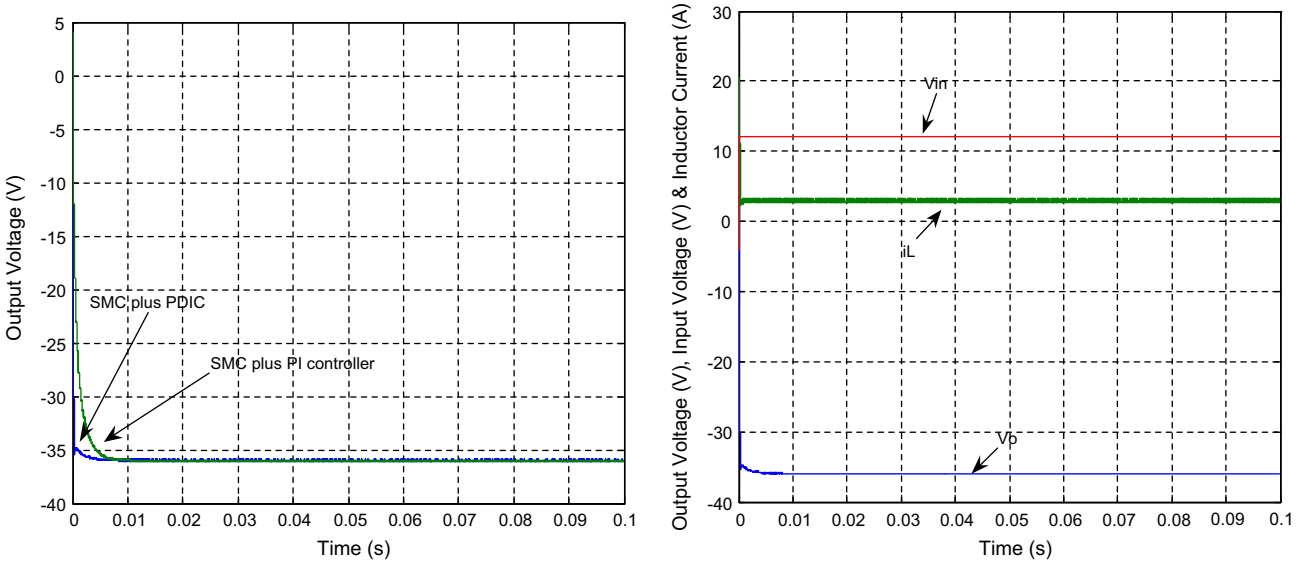


Figure 13 Simulated results of NOEBC with inductive load ($R = 50\ \Omega$ and $L = 10$ μH) using both the controllers in transient region, (a) output voltage and (b) input voltage, inductor current and output voltage.

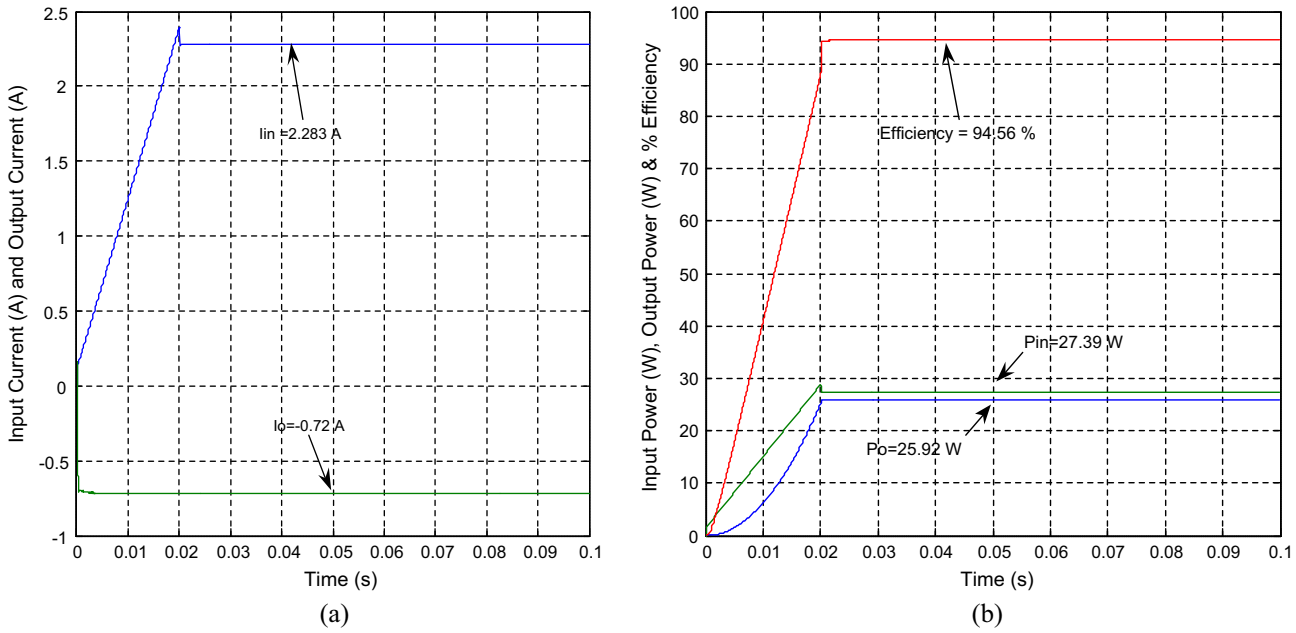


Figure 14 Simulated results of NOEBC with inductive load ($R = 50\,\Omega$ and $L = 10\,\mu H$) using SMC plus PDIC, (a) average input and output currents and (b) input power, output power and efficiency.

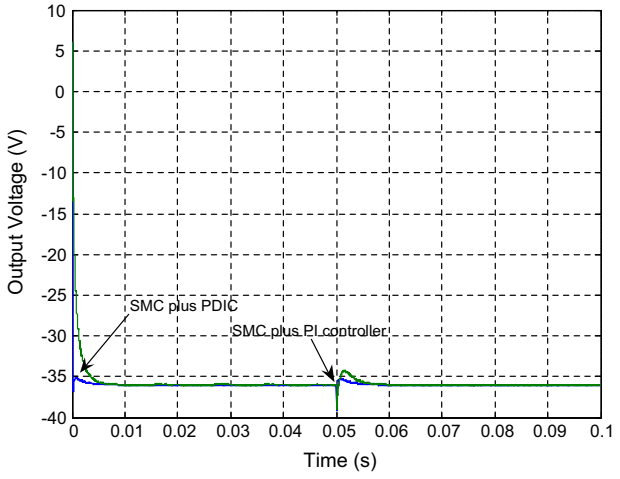
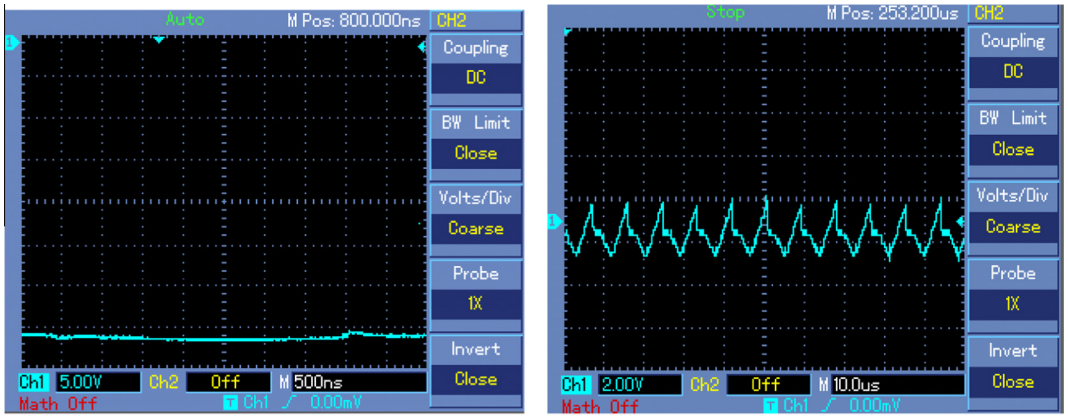


Figure 15 Simulated output voltage results of NOEBC with inductive load ($R = 50\,\Omega$ and $L = 10\,\mu H$) using both the controllers in line variations (12–09 V).

Fig. 12(a) shows the output voltage of designed controller for both the NOEBC and conventional boost converters when input supply voltage varied from 12 V to 15 V. From this figure, it is clearly shown that the output voltage of NOEBC has better performance over the conventional boost converter during line variation region. Fig. 12(b) shows the output voltage of designed controller for both the NOEBC and conventional boost converters when load resistance varied from 50 Ω to 60 Ω. From this figure, it is clearly shown that the output voltage of NOEBC has excellent performance in comparison with the conventional boost converter under the load variation region.

Fig. 13(a) shows the simulated output voltage response of the NOEBC with inductive load ($R = 50\,\Omega$ and $L = 10\,\mu H$) using both controllers in transient state with nominal power ratings. From this result, it is evident that the output voltage of the same converter using designed controller has quick settling time and negligible overshoot over the SMC plus PI controller with inductive load. Fig. 13(b) shows the simulated inductor current, input voltage and output voltage of the NOEBC using SMC plus PDIC. It can be found that the output voltage of this converter has negligible overshoot, whereas the inductor current of same converter using controller has produced small overshoot in transient region with inductive load. Fig. 14(a) shows the simulated average input and output currents of the NOEBC with inductive load using SMC plus PDIC. It is evident that the average output current and input current of NOEBC exactly match the theoretical value. Fig. 14 (b) shows the simulated performance of the NOEBC using designed controller with inductive load. From these results, it is clearly focused that the efficiency of this converter has slightly higher (94.56%) for inductive load in comparison with resistive load. Fig. 15 shows the simulated output voltage of the converter using both controllers for input voltage variation with inductive load. It can be seen that the output voltage of the converter has produced less steady state error, small overshoot and quick settling time using designed controller in comparison with PI controller. Fig. 16 shows (a) experimental output voltage response of the NOEBC using designed controller for line variation (12–09 V) with inductive load. It is found that the output voltage has small overshoot and quick settling time using SMC plus PDIC with inductive load. Fig. 16(b) shows the experimental sliding surface of SMC plus PDIC for NOEBC.

In summary, from Figs. 3–16, it is clearly indicated that the experimental results of the NOEBC using the designed SMC plus PDIC match the simulated results with a tolerance of ±2.5%. Finally, the proposed SMC plus PDIC performed well in the entire operating situation of the NOEBC.



(a) (b)

Figure 16 Experimental results of NOEBC with inductive load ($R = 50\ \Omega$ and $L = 10\ \mu H$) using the controllers in line variations (12–09 V), (a) output voltage (input voltage variation) and (b) sliding surface.

6. Conclusions

In this article, the theoretical analysis, design, and output voltage regulation of the NOEBC operated in CCM using a variable frequency based SMC plus PDIC have been successfully demonstrated. The proposed controller parameters have been implemented in analog platform. A major merit over a linear PIC lies in the fact that the SMC plus PDIC is robust to large variations on line, load and parameter variations without modifying the sliding coefficients. Many simulation and experimental results are presented in order to prove the performance of the proposed controller. The influence of the controller parameters on the performances of the system is studied.

The effortless analog circuit based implementation of a SMC plus PDIC and detailed experimental analysis are the key contributions of this article. Theoretical analysis, experimental and simulations are presented to illustrate the effectiveness of designed SMC plus PDIC for the NOEBC operated in CCM with resistive and inductive loads resulted in fast dynamic response, proficient regulated output voltage, non-disturbed output voltage during the circuit component variations, excellent steady state and transient responses, etc. Also, the simulation results of NOEBC using designed controller have better performance in comparison with conventional boost converter using the same controller. It is, therefore, suitable for any stable power source real-world commercial applications and it is mainly designed for power supply in different medical equipments, telecom, industrial and military applications.

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