Low-Power Universal Edge Tracer Architecture using Accuracy-Controlled Resource Reallocation for Event-Driven Sensing Applications

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Abstract

The low-power memory tracer architecture for sense data acquisition is proposed. The hardware pre-processor based on the proposed sense data tracer enables the low-power sense data analysis in a noisy environment. The sensed signals are tagged with the edge phases, threshold level, and elapsed timing distance between previous signal edges. The incoming sense data analysis is delayed, and its raw data is reallocated into the tracer memory. The traced sensed data is analyzed by the allocated event pattern-matcher in the silent background mode without any CPU assistance. The proposed method and hardware architecture enable an accurate original sense data reconstruction in the slow processor clock frequency. Newly designed building blocks are integrated into previously designed sensor processors for 3DTV active shutter glasses. The experimental result shows an additional power reduction to about 25\% of our previous work by allowing a small amount of error in the original sense data reconstruction. This paper describes the systems’ architecture and details of the proposed memory tracer in addition identifying the key concepts and functions.

Keywords: low-power sensor interface; event-driven processing; wearable sensor system;

1. Introduction

Nowadays, the front-end sensor interface IC for the human interface is easily implemented on a general-purpose system-on-a-chip (SoC) based on the integration of analog/digital circuit technology, a high-performance microcontroller powered by the digital hardware and on-chip embedded software algorithmic techniques, such as the ARM Cortex-M series. These processors are not suitable for sense data analysis only in terms of the power consumption per performance.

In the sense applications, there are two considerations. First, the external event is very slow compared with the internal CPU’s operating frequency. The low-power SoC architecture for the sensing applications has to consider
the total energy consumption in order to handle all external sense events over the long term. Second, in the case of the human interface, the analysis accuracy and sensitivity of the sense response time have to be relatively considered according to the frequency of external events because of slow external signal transitions.

The subsystem for the sensing applications generally require a very long lifetime because it is generally operated by the on-board battery. Because of these special considerations, a dedicated processor for sensing systems has to provide the systematic control of all digital/analog hardware and software operations to save total energy consumption during the entire time to analyze external analog signals, which happen in very rare event frequency compared with the processor operating frequency.

Fig. 1. Proposed sense data tracer architecture

2. Related Works

This paper introduces an improvement result starting from our previous studies\textsuperscript{1,2,3} and presents a low-power technique based on the proposed hardware architecture for sensing applications, especially 3DTV active shutter glasses used to sense the infrared radio signals transmitted from 3DTV.

The concept used to improve the original work is adopted from the previous creative concepts of energy-delay trade-off consideration\textsuperscript{4,5}. The event-driven system architecture, by merging the incoming sense data into meaningful events, adopts the original methodologies\textsuperscript{6,7,8,9}.

Our previous works focuses on the design optimization in terms of power consumption for specific sensor applications in which the external events are very slow, and the accuracy to reconstruct information from the sensed data is dynamically configured in the human environment. The protection technique for the robust sensor signal detection is presented in\textsuperscript{1}. The event-driven sense data processing method for sensing applications is introduced in our previous work\textsuperscript{2}. The resource reallocation for the accuracy configuration is presented in\textsuperscript{10} to utilize the time resource in the CPU IDLE. The self-synchronization technique based on accuracy-configuration using the sensor-off mode is presented to maximize the energy reduction performance in\textsuperscript{3}.

The proposed technique improves our previous studies\textsuperscript{1,2,3} to enhance the energy efficiency in the analog front-end in order to receive the wireless sense data in 3DTV applications. We applied the proposed techniques to the 3DTV active shutter glasses, which use the IR sensors to receive the synchronization pulse from the 3DTV’s emitter. The proposed method in this paper presents two contributions to enhance the previous studies. The first one is to provide the generalization of incoming sense data with edge phase, threshold level, and edge-to-edge timing distance. The general representation of the sensed data enables a reduction in the gate count of the dedicated pattern analysis hardware to handle various incoming sense data patterns. The second contribution is to introduce a concept of memory data reallocation in tracing the sensed data before the analysis hardware is activated. From this benefit, the power consumption needed to identify the meaningful sense data will be reduced by balancing the sense data shaping and patterns analysis.

In this paper, a newly designed systematic architecture named to the edge tracer is proposed along with a hardware technique for energy reduction, considering the special characteristics of these sense applications. Section III presents
3. Proposed Architecture

Conventional asynchronous events, which are triggered at an analog level, are first sensed with the analog-to-digital converter (ADC) operation. The ADC periodically has to wake up to sense the external signal transition and repeat to enter into the sleep mode in case of the event absence. The ADC performance and clock speed has to always be tuned for peak performance, regardless of the sensor input pattern frequency. This requires excessive power consumption during very long-term distances between events.

However, the accurate detection of every incoming sensor signal is not always necessary to handle the sensor signal correctly. There are urgent sense data that have to be directly processed on demand. Otherwise, the pattern analysis of the incoming sense data can be delayed to reduce the excessive energy consumption by the sensitive operation. From these considerations, we introduce the on-demand input filtering method, which can be applied to analog sensor front-end.

Fig. 1 describes our conceptual architecture of the proposed front-end for the sensor processor. Our approach adopts three additional components; threshold controllable multi-level comparators, event frequency detector, and the edge tracer building blocks, including tracer buffer memory and dedicated hardware, for the pattern analysis.

The proposed sensor input front-end starts from the minimal performance in which the clock speed is slow and all parts except for the analog signal transition detector, such as the analog comparator, are turned off. The selective detection by identifying the analog signal level (event type 1, 2, ...) enables to wake up conditionally to minimize the sensor processor wake-up. The tracer tracks the incoming sensor signals into the tracer buffer memory to delay the
sense data pattern analysis. This method will ignore the incoming sense data in first sequences and then gradually performs the adaptation for the specific patterns of the sense data. The analog comparator is added in the first stage of the analog sensor front-end to choose an analog signal transition with a specified signal filtering. This comparator separates analog signal levels with the specific priorities to inform the CPU and the remaining blocks.

The CPU core conditionally wakes up the ADC to detect the analog signal level in detail in case of the appropriate signal level presence. The current threshold level, which is used in this comparator, will be tagged into the sense data packets to trace the sense data. The frequency of the incoming signal events are monitored by the event frequency detector to control the system operating clock frequency. When the incoming event frequency is low, the event frequency detector (EFD) blocks decreases the system clock speed dynamically. If the urgent event requiring the fast operation occurs, the EFD block increases the clock speed to accelerate the ADC operation. The analyzed incoming sense data by the ADC are traced into the tracer block. The collected incoming sense patterns are independently analyzed by the dedicated finite state machine without any support of the CPU core and software operation. This means that the CPU operating current is reduced by turning off the CPU core and memory blocks.

The detailed edge tracer architecture is described in Fig. 2. The incoming sense data will be traced and reallocated with priority into the linear internal memory to accelerate the pattern analysis. The priority information is defined using the edge level and phases by the system programmer. The dedicated hardware, which is implemented in a tailor-made DSPs and its finite state machine, performs the pattern analysis silently in the background mode without any CPU assistance using the software. The tracer scans the incoming data and performs the adaptation to extract the priorities for the current sense data. With this information, the next incoming sense data analysis will be delayed and its sensed data is reallocated into the internal tracer buffer memory so that the sense data analysis is performed with the accelerated hardware for the serialized sense data stream during a short time period.

Fig. 3. Sense data tracing example according to the time/spatial sequences and pattern analysis hardware reallocation in battery capacity
The low-energy sensor front-end recognizes the on-demand event based on the event frequency of the input sense data and analyzes it directly using the high-performance-pattern analysis accelerator. Most events separated from urgent events are collected into the internal event tracer buffer, which can delay the analysis tasks to save processing energy. Fig. 2(a) shows the overall architecture of the edge tracer. The input sync pulses are accumulated in the SRAM via the direct-memory access (DMA) bus. The traced edges are analyzed by the trail-made DSP and FSMs. Fig. 2(b) is the field structure used to describe the general information about the edges. We minimized the field information to reduce the SRAM's size needed by the edge tracer.

In addition, the matching hardware could be generalized and easily reconfigured with the register control for the specific pattern-matching. Fig. 2(c) shows an example of incoming sync patterns affected by external noise, not causing the CPU wake-up by tracing the incoming sense data. Fig. 2(d) is an example of edges traced into the SRAM buffer. The sense data are collected with the specific conditions defined by the system programmer. We manage the SRAM buffer by using a ring type to increase the area of utilization. At the specific time, we perform the analysis of the past N number of edges accessed from the end-point of the SRAM buffer.

Fig. 2(e) shows the operation of the window-matcher DSP used to scan the traced data in the SRAM buffer, which is implemented with the finite state machine powered by the tailor-made DSPs. Because the sense data is represented by the information generalized with the edge phases, level, and its elapsed distance, the sense data analyzer is easily implemented with the pattern-matcher, which waits for the specific edges. This special DSP hardware and FSM are reconfigured with the register’s control to match the correct patterns for specific edge phases, the number of counts, and the time distance between edges. This block chooses specific patterns matched with predefined field values and merges them into the event group to be easily used by the sync reconstruction engine, which is introduced in our previous work.

The EFD building block controls the operating clock speed according to the event presence and its frequency. In case of event presence, the upper logic counter will be incremented until the counter overflow value for the event frequency increment. In case of event absence, the bottom logic counter calculates the counter threshold to decrease the clock frequency for adaptive sensor input processing with reasonable amounts of clock speed, which is fast enough to process the incoming data.
to handle the incoming sense data patterns. The sense data analyzer using the dedicated DSPs and FSM conditionally wake up to perform the sense data reconstruction according to the frequency of the incoming sense data and previously adapted sense data information. If current sense data is identified as a noise sequence, its sense data will be archived into the special region of the tracer memory, in case which the analysis is delayed with lower priority.

The current system battery capacity controls the accuracy and resolution for the sense data analysis, which is described in Fig. 2(g). The proposed edge tracer’s resources including the on-demand front-end and event tracer is selectively applied according to the current power performance to extend the battery lifetime. Fig. 3(a) shows the data reallocation in the sense data tracing step before the sense data analyzer is activated. This enables the proposed sense data analyzer in Fig. 2(a) to reduce the computation overhead in the analysis step. Continuous incoming sense data is first scanned with the pattern analysis method of the time sequence and its data are traced into the linear memory.

This is useful for identifying the normal signal reconstruction, which is encoded by the external sensor. If a noisy environment is detected, the current incoming data will be spread into the archived area in the memory space to assist in the spatial analysis for the correlation of previous signals, which is merged into several events. Fig. 3(b) describes the analyzer resource reallocation method to control the analysis resolution according to the current battery capacity. The internal brown-out detector monitors the current power level to estimate the performance of the analysis hardware in terms of the remaining battery capacity. The on-demand resource allocation manager indicated by the brown-out detector will be applied to perform the sense data analysis, considering the current battery capacity.

The ADC performance is decreased from high to low resolution to reduce the activated blocks in the ADC IP. The clock frequency and counting resolution for the sense data edge distance measurement is relaxed with a reasonable amount of bits. If sense data is stable and the battery level is becoming low, the parallel pattern-matcher block is not necessary, and several parts of the pattern-matcher blocks can be turned off with the clock gating. The wake-up frequency and analysis resolution is gradually decreased to extend the battery operating time by allowing the error of the sense data reconstruction. This approximation technique by allowing a reasonable number of errors is effective in the case of human-related timing data construction because the sense data triggered by the human is relatively slow and ignorable to the operating speed of the processing chip.

4. Implementation Results

We applied our technique to the sync processor for the 3DTV active shutter glasses, which is described in Fig. 4. The implemented chip improved the original performance in terms of the power consumption by adding additional building blocks, including the on-demand input front-end of the sensor interface, the edge tracer, and its pattern-matcher. These blocks are emphasized with the red-dotted line in Fig. 4(a). The first sequence for the low-power operation of the 3DTV shutter glasses is to trace the incoming packets into the SRAM buffer to hibernate the CPU resources and then to delay the sync analysis until several edges are merged into the pre-defined event unit. The edge phase and threshold level represent the detailed information of the received sense data.

We implemented the proposed analysis hardware described in Section IV to accelerate the sync analysis for the 3DTV shutter glasses so as reduce the overhead for CPU processing. This block performs the analysis in a parallel fashion in the background mode without any CPU interruption. The collected sense data will be reconstructed slowly for a unit event that represents minimum information. To achieve low power, a small size, and general-purpose reusability, we adopted and implemented the proposed edge tracer concept to track the common information monitored with the edge phase, edge threshold levels, and edge distances for the incoming packets transmitted from 3DTV and to delay the sync pattern analysis requiring fast CPU resources. We integrated a dedicated SRAM buffer with the edge tracer to trace the incoming packets without using the CPU.

During the tracer operation, the CPU can hibernate to minimize the system’s power consumption, but the accuracy needed to reconstruct the original sense data becomes low until the minimum condition reaches the value defined by the system programmer. In our experiment, we allow a 5%-20% error deviation, which is caused by applying the inaccurate front-end and hardware to relax the active blocks. When the proposed method is enabled, there is an average of about 25% additional power reduction in the case of 20% clock accuracy, the counter of 20 bits resolution in DSPs to measure the edge distance, and one activated pattern-matcher, compared with our latest result.
This is achieved with the hardware cost of the tracer buffer (8KB buffer), small logic gates (under about 5000 NAND gates) and specific number of accuracy errors (minimum 5%). Fig. 4(b) illustrates the overall operation using the proposed edge tracer architecture allowing the specific number of errors of the sense data analysis resolution.

5. Conclusion

The sense data-tracing technique and its hardware architecture are used to enable the low-power sense data analysis to reconstruct the original sensing information. The proposed methods delay the incoming sense data analysis and the sensed signals are represented with edge phases, threshold levels, and timing distance from the previously received signals. The generalized sense data will be reallocated into the local tracer memory based on the priorities that are extracted from the previous pattern analysis. The timing sequence allocation will be used to perform the signal patterns, but the spatial analysis will be effective for scanning the noise embedded in the original sense data. The data reallocation in incoming data-tracing step enables the dedicated sense data analyzer to easily perform the pattern analysis. The chip implementation of the proposed technique is applied to improve the performance, which is previously presented in our work for the 3DTV application, by getting a benefit of the maximum 25% current reduction with the cost of additional area and accuracy error.

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References