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Analysis of the sub-surface damage of mc- and cz-Si wafers sawn with diamond-plated wire

Rajko Buchwald\textsuperscript{a}\textsuperscript{*}, Kilian Fröhlich\textsuperscript{a}, Sindy Würzner\textsuperscript{a}, Toni Lehmann\textsuperscript{a}, Kirsten Sunder\textsuperscript{b}, Hans Joachim Möller\textsuperscript{a}

\textsuperscript{a}Fraunhofer THM, Am St.-Niclas-Schacht 13, Freiberg D-09599, Germany
\textsuperscript{b}PV Crystalox Solar Silicon GmbH, Gustav-Tauschek-Straße 2, 99099 Erfurt, Germany

Abstract

The usage of diamond-plated wire to produce silicon wafers for the photovoltaic industry is still a new and highly investigated wafering technology. The requirements regarding the quality of the wafer surface are very high and they have to compete with the cost effectiveness and quality of wafers produced by the established loose abrasive sawing technology. Hence, the wafer topography, the fracture stress and the corresponding sub-surface damage have to be investigated and improved.

This paper discusses the topographic parameters, the crack depths and the fracture stress of mono- and multi-crystalline silicon wafers that were produced on multi-wire saws using diamond-plated wire and comparable process parameters. Especially multi-crystalline silicon (mc-Si) wafers exhibit lower fracture stress values compared to mono-crystalline silicon (cz-Si) wafers. We investigated the relations between crack depth and fracture stress. In detail, we determined a 15\% higher median and a 40\% increased interquartile range of the crack depth of mc-Si wafers in comparison to similar produced cz-Si wafers. That correlates with lower fracture stress values of textured mc-Si wafers compared to cz-Si wafers. In the following, we studied the sub-surface damage as a function of crystal orientation in detail. It was found that the crack depths increases from the \{100\} plane over the \{111\} plane to the \{101\} plane. However for the \{101\} plane two grains were investigated, resulting in a discrepancy of 4 µm. This may be related to the unknown rotation angle between the corresponding \{111\} cleavage planes and the wire direction and requires further investigations.

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* Corresponding author. Tel.: +49 3731 2033 122; fax: +49 3731 2033 199.
E-mail address: rajko.buchwald@thm.fraunhofer.de
1. Motivation

An alternative technique to the common used sawing technique with loose abrasives like silicon carbide particles is the usage of steel wire coated with diamond particles. The advantages of this technique are higher cutting speeds, less wire requirements and the usability of a cheap cooling fluid such as water. Recent developments have shown that it can also be used to cut silicon wafers [1, 2], but some basic problems still have to be solved.

The experiences so far indicate that fixed abrasive cutting of cz-Si ingots into wafers of standard thickness of 180 μm shows a higher sawing performance than mc-Si wafer slicing. In general, wafer surface quality differs from loose abrasive cut wafers. Fracture stress measurements on as-cut and textured mc-Si and cz-Si wafers sawn with diamond-plated wire verify lowered fracture stress values in comparison to slurry wafers. Higher breakage rates of diamond cut wafers and especially of mc-Si wafers are the consequence.

We initiated this work to investigate the origin of the increased breakage rate of mc-Si wafers in detail.

2. Sample description

To investigate the origin of the increased breakage rate of diamond cut wafers, we produced comparable sets of cz-Si and mc-Si wafers on lab scale. These as-cut wafers were used for fracture stress analyses, topographical and sub-surface damage investigations. Furthermore we produced on industrial scale mc-Si wafers in a standard loose abrasive sawing process and in a diamond-plated wire sawing process, respectively. After texturing we determined the fracture stress of these wafers. A sample overview is given in Table 1 together with the information which analyses were performed.

<table>
<thead>
<tr>
<th>production type</th>
<th>material</th>
<th>abrasive</th>
<th>TTV</th>
<th>topogram</th>
<th>analysis</th>
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</thead>
<tbody>
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<td>diamond wire</td>
<td>X</td>
<td>X</td>
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<tr>
<td>laboratory scale</td>
<td>mc-Si</td>
<td>slurry</td>
<td></td>
<td>X</td>
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<td>mc-Si</td>
<td>diamond wire</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

3. Methods

Roughness and total thickness variation (TTV) of the lab scale wafers were measured optically with a white light confocal measurement system. The TTV was taken from six profile lines, three of them on each wafer surface. A schematic draft of the profile line positions can be seen in Fig. 1 (a). The measurement point distance was 100 μm. All lines started and ended with a distance of 4 mm from the corresponding wafer edge. Roughness and waviness were analyzed on nine profile lines per wafer (Fig 1 (a)). The directions of the TTV- and roughness-profile lines were perpendicular to the wire direction. The crack depth was determined on beveled samples using a laser confocal microscope. The
positions of the beveled samples for the crack depth comparison of cz-Si and mc-Si wafers are shown in Fig. 1 (b).

For the investigation of crack depth as a function of crystal orientation, we used a wafer that was produced on industrial scale. This implies that the wire web was moved regularly back and forth with a small wire supply (pilgrim mode). To ensure a constant state of the diamond wire and therewith of the wafer surface the wafer for crack analysis originates from the fresh wire side of the brick. We determined the crystal orientation of large grains on this wafer by means of the XRD-Laue method. The positions of these grains on the wafer are shown in Fig 2. For the final crack depth analysis we used three samples marked as E, F and G. These samples contain crystal orientations of \{100\}, \{101\} and \{111\}. The number of measured maximum crack depths was 40 per grain. Caused by a small grain size for E\{101\} only 28 maximum crack depths could be determined.

The fracture stress was measured via a four-line bending test.

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Fig. 1. Schematic draft of the used profile line setup for measuring (a) TTV (dotted lines) and roughness (crosses). (b) shows the positions of the three beveled samples for the comparison of cz- and mc-Si wafers sub-surface damage analyses.
4. Results and discussion

4.1. Optical surface measurements

As shown in Fig. 3 we determined a TTV median of 16.7 µm for cz-Si wafers and 28.2 µm for mc-Si wafers. That equals an increased TTV median of 68 %. Furthermore a ~40 % higher interquartile range was measured for mc-Si wafers. Hence, the lower quartiles of the mc-Si wafers never fall below the higher quartiles of all cz-Si wafers. Both materials showed a slightly increased TTV (TTV2) in the middle of the wafers.
In the following we measured the roughness and waviness. We found that the median of the roughness value $R_z$ was slightly larger (7 %) for mc-Si (3.2 μm) than for cz-Si (3.0 μm). In dramatically contrast to that we measured a 113 % higher waviness for the mc-Si wafers.

4.2. Fracture stress analysis

The fracture stress measurements were done with a parallel and perpendicular alignment of the bending bars to the wire direction of the wafer. In case of the perpendicular alignment, the fracture stress for textured mc-Si wafers was similar for both slurry sawn and diamond-plated wire sawn wafers (Fig. 4). Concerning the as-cut diamond-plated sawn wafers the cz-Si results in an only 4 % higher fracture stress than mc-Si (not shown).

In contrast the parallel bar-wire-direction-alignment yield for the textured mc-Si wafers a 66 % increased fracture stress for slurry sawn wafers than for diamond-plated wire sawn wafers (Fig. 4). And also the comparison of as-cut mc-Si and cz-Si wafers sawn with diamond-plated wire show an enhancement of ~40 % for the cz-Si wafers (not shown).
4.3. Sub-surface damage analysis

The topographic and fracture stress measurements indicate a higher and directional sub-surface damage of diamond wire sawn wafers. On that account we have made crack depth analyses on beveled samples. We found a 15 % lower median and a 40 % lower interquartile range of the crack depth for cz-Si as for mc-Si wafers, as one can see in Fig. 5. To understand this significant difference in detail, we made crack depth analyses on mc-Si wafers as a function of crystal orientation.
4.4. Sub-surface damage analysis as a function of crystal orientation

Fig. 6 shows a height map and a 3D surface image of a small section of sample E that contains three grains. Hence, two grain boundaries (two thin and dark lines from middle left edge to lower right corner) separate the grains. On the right half of the sample one can see a broad line of rough surface damage. The direction of this rough area follows the direction of the wire. In the lower right corner of Fig. 6 the rough surface crosses the two grain boundaries. It is obvious that the surface roughness changes between the two grain boundaries. That indicates a crystal orientation dependency of the material removal process and therewith of the resulting crack depths.

To underline this finding we determined the crack depths of four crystals on three samples (E, F, and G) out of the same wafer (Fig. 2). Thus three crystal orientations were investigated ({100}, 2 x {101}, and {111}).

We found a clear crystal orientation dependency of the crack depth for sample F and G which contains all three crystal orientations (see Fig 7). The median of maximum crack depths increases from 3.66 μm for the {100} plane to 5.83 μm for the {111} plane and to 7.25 μm for the {101} plane which confirms a crystal orientation dependency of the crack depth.

In contrast the crack depth of sample E{101} is 4 μm smaller than of sample F{101} which has the same orientation plane. This fact may be related to the unknown rotation angle between the corresponding {111} cleavage planes and the wire direction. For the measured {101} crystal orientation, two of three cleavage planes are perpendicular orientated to the wafer surface. If one of the two cleavage planes is parallel orientated to the wire direction, the mechanical stress field, that is caused by the indenting diamond particle will also have a parallel orientation to the cleavage plane which results in a deep crack with low energy consumption. To verify this thesis further investigations are required.
5. Conclusion

The aim of our investigation was to decrease the wafer breakage rate of cz- and mc-Si wafers sawn with diamond-plated wire. Therefore we investigated the wafer topography and the fracture strength of cz- and mc-Si wafers first. We determined a TTV median of 16.7 $\mu$m for cz-Si wafers and 28.2 $\mu$m for mc-Si wafers. That equals an increased TTV median of 68 %. The fracture strength investigations on textured mc-Si wafers show a 66 % increased fracture stress for slurry sawn wafers than for diamond-plated wire sawn wafers (parallel bar-wire-direction-alignment). Also the comparison of as-cut mc-Si and cz-Si wafers sawn with diamond-plated wire show an enhancement of ~40 % for the cz-Si wafers.

We suggest that these material impacts result from the various crystal orientations in mc-Si. This assumption is supported by the dependency of surface roughness on crystal orientation which are confirmed by means of wafer surface topography. Furthermore we verify the dependency of crack depth on crystal orientation via crack depth analysis of four grains on a mc-Si wafer. It was found that the crack depths increases from the \{100\} plane over the \{111\} plane to the \{101\} plane. However for the \{101\} plane two grains were investigated, resulting in a discrepancy of 4 $\mu$m. This may be related to the unknown rotation angle between the corresponding \{111\} cleavage planes and the wire direction and requires further investigations.

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