Available online at www.sciencedirect.com

ScienceDirect

Energy Procedia 38 (2013) 833 – 842

Energy Procedia

SiliconPV: March 25-27, 2013, Hamelin, Germany

IPA-free texturization of n-type Si wafers: Correlation of optical, electronic and morphological surface properties

Jan Kegel[a,b]*, Heike Angermann[b], Uta Stürzebecher[c], Bert Stegemann[a]

[a]*HTW Berlin - University of Applied Sciences Berlin, Wilhelminenhofstr. 75a, D-12459 Berlin, Germany*
[b]*Helmholtz-Zentrun Berlin für Materialien und Energie, Institut für Silizium-Photovoltaik, Kekuléstraße 5, D-12489 Berlin, Germany*
[c]*CiS Institut für Mikrosensorik und Photovoltaik, Konrad-Zuse-Str. 14, D-99099 Erfurt, Germany*

Abstract

The application of an Isopropanol(IPA)-free potassium hydroxide (KOH) solution was evaluated in order to prepare random pyramids on as-cut crystalline n-type Si wafers to reduce reflection losses of substrates for high-efficiency hetero-junction solar cells. The influence of saw damage removal and texturization processes on the resulting pyramid morphology and the corresponding interplay between optical and electronic properties are revealed. It is shown that both the depth of the saw damage etching (SDE) and the duration of the texturization etching have crucial influence on the resulting pyramid size distribution. Reflection losses can be reduced with decreasing fraction of small pyramids. By intermediate saw damage removal and texture etching times in (IPA)-free KOH solution the densities of electronic interface states were found to be strongly decreased ($D_{it,min} < 5 \cdot 10^{-11}$ cm^{-2}eV^{-1}), in comparison to pyramids prepared in IPA containing solutions. For the purpose of fabricating amorphous/crystalline (a-Si:H/c-Si) heterojunction solar cells the Si substrate surfaces were passivated with an intrinsic layer of amorphous silicon (a-Si:H(i)) leading to minority charge carrier lifetimes τ_{eff} of 2 to 4 ms, depending on the preceding texturization process.

Keywords: c-Si; a-Si:H; Defect Density; Etching, Heterojunction; n-type; Optical Losses; Texture, Texturization, Pyramids

1. Introduction

The successful fabrication of high-efficiency amorphous/crystalline heterojunction solar cells requires proper texturization of the Si substrates in order to minimize reflection losses and to increase the

* Corresponding author.
E-mail address: kegel_j@yahoo.de.

doi:10.1016/j.egypro.2013.07.353

absorption probability by light trapping. Since this improvement of the optical properties is associated with the creation of a larger surface area, the density of electronic defect states is expected to increase, compared to flat substrate surfaces [1]. Conventionally, random pyramid textures are achieved by wet-chemical etching of the as-cut wafer in alkaline solution containing IPA as additive. Due to its high volatility and environmental impact IPA was replaced by GP Alkatex Zero [2]. While in industrial processes saw damage removal and texture etch are done in a single process step in this study the two steps are separated to reveal the particular influence of both processes on the pyramid morphology. The correlation of saw damage removal and texturization was investigated with the goal to optimize systematically the resulting pyramid morphology with respect to minimal reflection and recombination losses.

2. Experimental

Single crystalline as-cut Si(100) wafers (float zone grown, n-type, 1 - 5 Ωcm, diameter 4″ n-type, thickness 260 - 300 µm) were used to prepare two sets of textured samples with (i) systematically varied depth of saw damage etch (set A) and (ii) systematically varied duration of texture etching in IPA-free KOH solution (set B). For the stepwise removal of saw damages the as-cut samples were etched in 10 % aqueous solution of KOH heated to 75 °C with increasing treatment duration (table 1, set A). For the preparation of random pyramids (texturization) after saw damage removal the samples were processed in alkaline solutions for different treatment times (table 1, set B). For IPA-free surface texturing GP Alkatex Zero was added to KOH solution (3 %, 80 °C). Reference samples were prepared in standard KOH + IPA solution (table 2). The wafers were subsequently cleaned by the standard RCA process [3]. The resulting oxides were removed by HF-dip (1%, 2 min) immediately before a-Si:H(i) deposition. In order to check the effect of surface micro-roughness on pyramid facets, similar samples were additionally treated by a smoothing procedure consisting of wet-chemical oxidation in $H_2SO_4 : H_2O_2$ solution and oxide removal by a second HF-dip (1%, 2 min) [4]. In Tables 1 and 2 the parameters of SDE, texture preparation and wet-chemical surface pre-treatment for all samples are listed.

Nominally intrinsic a-Si:H(i) films ($d_{a\text{-}Si:H(i)}$ = 6 nm) were deposited in a 13.56 MHz parallel plate PECVD system described elsewhere [5]. After deposition the a-Si:H(i)/c-Si stacks were treated in hydrogen plasma [6,7].

Morphologically analysis was done using a Phillips XL20 Scanning Electron Microscope (SEM). To reveal the pyramid size distribution a special evaluation algorithm was applied.

Reflection losses were analyzed with a Perkin Elmer Lambda 1050 UV-Vis-NIR spectrometer with integrated sphere. Spectra were taken in the range of 250 nm to 1500 nm. For significant comparison of the samples the normalized reflection R_n was considered. R_n is derived from the ratio of the integrated UV-Vis reflection spectra in the range of 250 nm to 1200 nm and the complete reflection (100 %) in this interval.

Field-dependent Surface photovoltage (SPV) measurements were carried out immediately after wet-chemical preparations utilizing the same experimental set up as described elsewhere [4,8,9]. The sample under test became part of an artificial metal-insulator-semiconductor structure (MIS). Therefore it was placed between a sheet of mica with a transparent conductive oxide front contact (TCO) and a metallic back contact. Illuminating the MIS structure with an intense laser pulse (1.36 eV, 162 ns, intensity 10^{19} photons/($cm^2 \cdot s$)) result in generation of excess charge carriers leading to band flattening and quasi Fermi level split up. The difference in the surface potential leads to a capacitively measureable photovoltage transient. By applying an external electric field perpendicular to the sample it is possible to determine the energetic distribution of the density of states $D_{it}(E)$ at the interface under the assumption that the charge state does not change during the light exposure [4].

By transient photoconductance decay (TrPCD) measurements using a Sinton Consulting WTC-100 [10] we estimate the minority charge carrier lifetime τ_{eff} of the a-Si:H(i)/c-Si stacks (excess charge carrier density = 10^{15} cm^{-3}) after post-deposition hydrogenation.

Table 1. Wet-chemical preparation of textured samples to evaluate the effect of SDE (set A) and texturization (set B).

	SDE	Texturization IPA-free solution	Cleaning RCA	H-termination HF-dip	SEM	SPV	TrPCD
set A	5 µm/side	20 min	x	x	Fig. 3 a (1)	Fig. 4 (1)	Inset Fig. 3
	10 µm/side	20 min	x	x	Fig. 3 b (2)	Fig. 4 (2)	Inset Fig. 3
	20 µm/side	20 min	x	x	Fig. 3c (3)	Fig. 4 (3)	Inset Fig. 3
set B	10 µm/side	5 min	x	x	Fig. 5 a	Fig. 6 (1)	Inset Fig. 5
	10 µm/side	20 min	x	x	Fig. 5 b	Fig. 6 (2)	Inset Fig. 5
	10 µm/side	40 min	x	x	Fig. 5 c	Fig. 6 (3)	Inset Fig. 5

Table 2. Wet-chemical pre-treatment of samples textured (i) in IPA-free and (ii) in IPA containing solutions to evaluate preparation induced micro-roughness.

Texturization	Cleaning	Wet-chemical oxidation	H-termination	SEM	SPV
IPA-free solution	RCA	-	HF-dip (2 min, 1 %)	Fig. 1a)	Fig. 2 (1)
IPA-free solution	RCA	H_2SO_4 : H_2O_2	HF-dip (2 min, 1 %)	-	Fig. 2 (2)
KOH + IPA	RCA	-	HF-dip (2 min, 1 %)	Fig. 1b)	Fig. 2 (3)
KOH + IPA	RCA	H_2SO_4 : H_2O_2	HF-dip (2 min, 1 %)	-	Fig. 2 (4)

3. Results and discussion

3.1. Comparison between conventional texturization in KOH + IPA and IPA-free texturization

In order to evaluate the differences between the conventional texturization in IPA-containing KOH solution (i.e. KOH + IPA) and the IPA-free approach, the pyramid morphologies and densities of interface states on the resulting substrate surfaces were investigated by SEM and SPV measurements.

In Fig. 1 the SEM images of samples textured by these different wet-chemical solutions are shown. The conventional wet-chemical etching in KOH + IPA (Fig. 1b) results in morphologies with bigger pyramids compared to the IPA-free texturization (Fig. 1a). The average size of these pyramids is about 10 times higher than the average size obtained by etching in the IPA-free solution. By the SEM investigation of sample surface, textured by the conventional KOH + IPA solution, roughened pyramid planes are found. To evaluate the influence of surface micro-roughness on the density of surface states subsequent to the standard RCA process an additional wet-chemical oxidation process in H_2SO_4 : H_2O_2 [4] was applied on both types of samples - prepared in KOH + IPA and the IPA-free solutions, respectively (Table 2.).

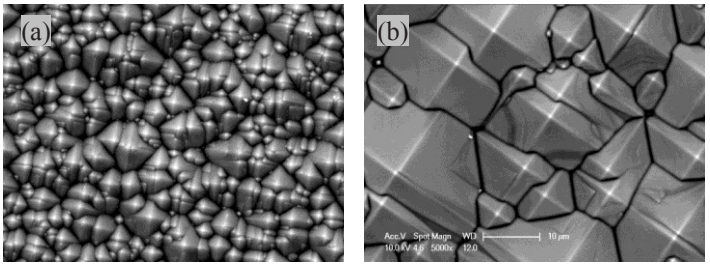

Fig. 1. SEM images (size: 60 µm x 40 µm, tilt = 0°) of textured Si wafers a) after IPA-free texturization b) after texturization in KOH + IPA.

Fig. 2 shows the energetic distribution of interface states $D_{it}(E)$ as determined on both types of samples by field dependent SPV measurements. Comparison of the $D_{it}(E)$ distributions allows to derive differences in the surface electronic properties. Whereas the curves (1) and (2) (IPA-free texturization) with and without additional smoothening show only slight differences in the lower half of the bandgap, a huge difference in width and minimum of the $D_{it}(E)$ distributions can be seen for the KOH + IPA texturized samples after standard RCA clean (curve 3) and subsequent smoothing procedure (curve 4). This big difference indicates a higher density of surface states on conventionally prepared substrate surfaces (curve 3) after standard RCA-clean and HF-dip. On these samples an additional oxidation with H_2SO_4 : H_2O_2 and subsequent HF-dip reduces the density of surface states resulting from crystallographic defects at the surface and incomplete H-termination due to roughened pyramid planes [4].

Fig. 2 illustrates also that IPA-free texturization with Alkatex Zero generally is advantageous for low surface state densities (curves 1 and 2). Even with a standard cleaning process (RCA + HF-dip) a surface with low density of states is achieved (curve 1). The additional smoothing in H_2SO_4 : H_2O_2 only leads to a slight reduction of surface states (curve 2), indicating a low micro-roughness on the initial surface after texturization.

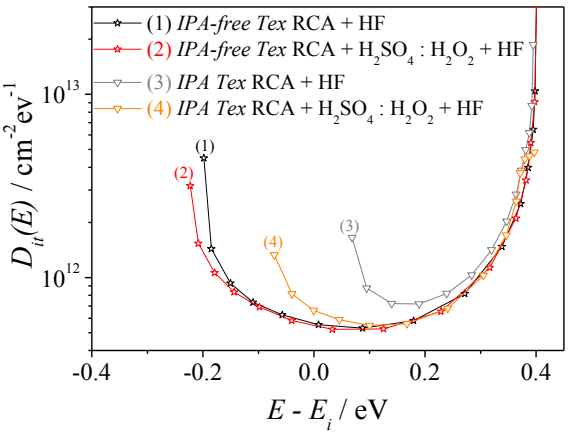

Fig. 2. Distribution of energetic surface states $D_{it}(E)$ for samples with different wet-chemical texture preparation.

3.2. Influence of saw damage removal on electronic interface properties

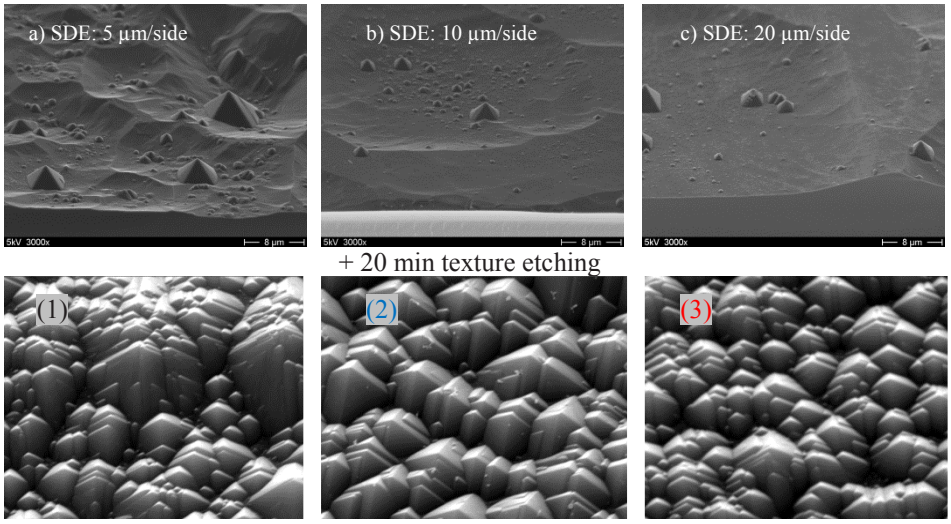

Fig. 3. SEM images of Si wafers with different SDE (a), b) and c)); image size: 40 µm x 30 µm, tilt = 30°) and subsequent texturization of 20 min ((1), (2) and (3)); image size: 25 µm x 19 µm, tilt = 30°).

To evaluate the effect of SDE on the morphology and electronic properties of substrates with random pyramids on a set of samples (A) the depth of saw damage removal was systematically varied from 5 to 20 µm/side. Subsequently, these samples were treated with KOH + Alkatex Zero for constant duration (20 min) (Table 1).

In the upper row of Fig. 3 SEM images of samples only treated with SDE are shown. The SEM image of the sample with only 5 µm/side SDE (Fig. 3a) clearly shows an increased inhomogeneity compared to a sample with intermediate (10 µm/side) saw damage removal (Fig. 3b). For a higher saw damage removal of 20 µm/side (Fig. 3c) only a marginal improvement of homogeneity is found.

The lower row of Fig. 3 shows SEM images of similarly saw damage etched samples after subsequent texturization etching of 20 min. As shown in the SEM images of Fig. 3 due to the low depth of saw damage removal (5 µm/side) the texturization process does not completely eliminate the inhomogeneities at the surface (1), compared to the samples with higher depth of damage removal (2) and (3). Moreover intermediate saw damage removal results in a surface with bigger pyramids (2). Even at the surface of the sample with deeper SDE a higher fraction of small pyramids was obtained (3).

Fig. 4 presents the corresponding energetic distributions of the density of electronic surface states $D_{it}(E)$ determined by SPV measurements on these textured samples (set A) with increasing saw damage removal immediately after RCA clean and HF-dip. The $D_{it}(E)$ distributions of all samples reveal minimum values of 5.2 to 6.4 · 10^{-11} $cm^{-2}eV^{-1}$.

While the distribution for intermediate (curve 2) and deep (curve 3) saw damage removals barely differ, the $D_{it}(E)$ distribution obtained on textured surfaces after insufficient saw damage removal (curve 1) is narrowed in the lower half of the bandgap. Due to the low saw damage removal (5 µm/side) the remaining surface is very uneven after SDE as well as after texturization process. A rough and uneven surface, however, causes an enlarged number of electronic defect states located in the lower half of the bandgap [11], which leads to the difference between the $D_{it}(E)$ distributions of the sample with low (curve 1) and intermediate/deep saw damage removal (curves 2 and 3). In comparison to SDE of

10 µm/side (curve 2) no further decrease in the density of surface states was observed after deeper SDE of 20 µm/side (curve 3).

The inset of Fig. 4 presents the resulting the minority charge carrier lifetimes τ_{eff} determined by TrPCD measurements on identically prepared samples (set A) after deposition of intrinsic amorphous silicon (a-Si:H(i)) layers and post-deposition hydrogenation. It is shown, that for all samples an appropriate passivation of defects is achieved. Highest carrier lifetime τ_{eff} is obtained by intermediate saw damage removal (e.g. (2), approx. 4 ms). A lower (1) as well as a further saw damage removal (3) result in lower values of τ_{eff} of approx. 2.8 and 2.4 ms, respectively. As a reason for the decrease of charge carrier lifetimes after longer SDE we assume the longer overall etching duration and the corresponding appearance of a higher number of smaller pyramids and therefore an increased number of pyramid valleys. Pyramid valleys are known to cause defects at the a-Si:H(i)/c-Si interface [12]. Furthermore many smaller pyramids cause additional defects due to an enlarged roughness at the surface.

From these findings it is concluded that an intermediate saw damage removal (10 µm/side) is sufficient to eliminate defects in the material caused by the saw damage itself and does not lead to further defects resulting from a rough and uneven textured surface with smaller pyramids.

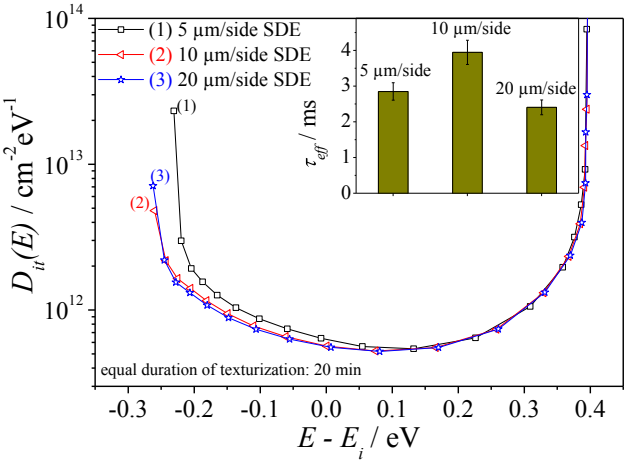

Fig. 4. Energetic distribution of electronic surface states $D_{it}(E)$ on samples prepared by different SDE (5, 10 and 20 µm/side) and constant texture etching time of 20 min (set A). Inset: Corresponding carrier lifetimes τ_{eff} of similar samples after a-Si:H(i) deposition and post-deposition hydrogenation.

3.3. Influence of texturization durations on electronic interface properties

To elucidate the influence of the texturization time on the surface morphology and electronic interface properties, a second set of samples (set B) was prepared by constant SDE (10 µm/side) but varying texturization times ranging from 5 to 40 min (equals a texture etch of 2.2 to 8.5 µm/side) utilizing the IPA-free KOH solution (Table 1).

In Fig. 5 the resulting morphologies of three samples after increasing texture etching times are shown by SEM images. Short etching duration of 5 min leads to an uneven surface with smaller pyramids (Fig. 5a). The SEM images reveal that morphologies with a higher fraction of bigger pyramids can be achieved by intermediate texturization durations (e.g. 20 min, Fig. 5b). However, a very inhomogeneous texture with many small pyramids is found after extended texturization duration of 40 min (Fig. 5c).

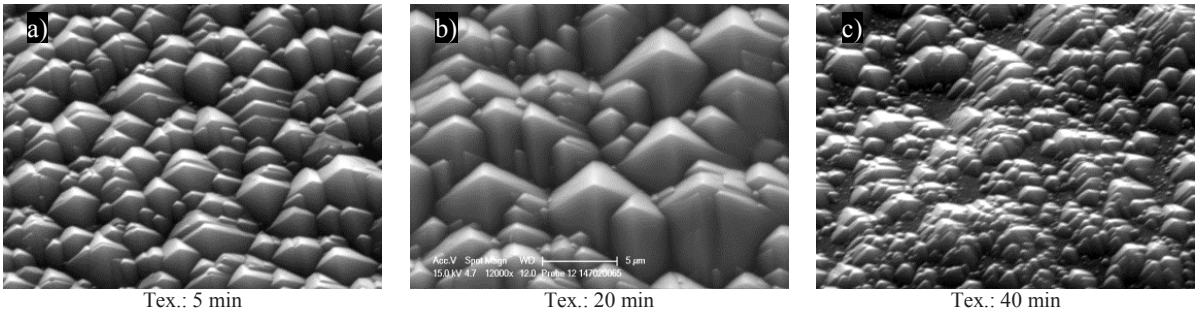

Fig 5. SEM images of samples (set B) prepared with different duration of texturization a) 5 min b) 20 min c) 40 min, subsequent to SDE: 10 µm/side (picture size: 25 µm x 19 µm, tilt: 30°).

Apparently, long texture etching times result in variable morphologies and roughened pyramid planes with some pyramid-free surface areas.

The results of SPV measurements carried out on these samples (curves 1, 2, 3) immediately after RCA clean and HF-dip are given in Fig. 6. Compared to samples (1) and (2) prepared by shorter texturization times (5 min and 20 min respectively), the $D_{it}(E)$ distribution obtained on the sample (3) after the longest duration of texturization (40 min) exhibits a higher density of surface states in the lower half of the bandgap. As already demonstrated in the SEM image of sample (3) this textured surface is very inhomogeneous (see Fig. 5c). The extended etching duration also leads to micro-roughened pyramid planes which are known to be particularly responsible for crystallographic imperfections [4]. The results of SPV measurements indicate that pyramid facets are affected when the duration of texturization extends 20 min.

The inset in Fig. 6 shows the effective charge carrier lifetime τ_{eff} determined from TrPCD measurements on similar samples (set B) textured in IPA-free KOH solution (5, 20 and 40 min) after a-Si:H(i) deposition and post-deposition hydrogenation. Longest charge carrier lifetimes of τ_{eff} = 4 ms were obtained on a -Si:H(i)/c-Si interfaces prepared on sample (2) applying intermediate duration of texturization (20 min).

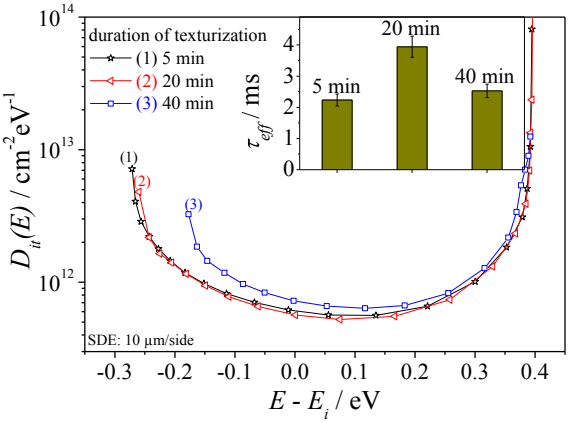

Fig. 6. Energetic distribution of electronic surface states $D_{it}(E)$ on samples prepared by SDE (10 µm/side) and different texturization times (set B). Inset: Charge carrier lifetime τ_{eff} of similar samples after a-Si:H(i) deposition and post-deposition hydrogenation.

For extended duration of texture etching (40 min) lower effective lifetime τ_{eff} of 2.5 ms were preserved as shown exemplary for sample (3).However, also short texturization times (5 min) applied on sample (1) yield charge carrier lifetimes of 2.2 ms. On the one hand this even lower value of τ_{eff} can occur due to the low overall etch removal (SDE + texture). On the other hand the too short etching leads to an incomplete texturization with a higher fraction of small pyramids and surface irregularities on the planes of bigger pyramids resulting in a defect-rich a-Si:H(i)/c-Si interface.

Summerizing these results it is concluded that intermediate saw damage removals of ≈10 µm/side and subsequent texture etch of 10 to 20 min (equals 3.8 to 5.7 µm/side) lead to a homogeneous texture with excellent electronic properties.

3.4. Influence of pyramid size-distribution on reflection losses

Statistical analysis of the SEM images was performed with the help of a specific software algorithm. It yields the sizes and the size distribution of textured silicon wafers. As an example, in Fig. 7 the resulting pyramid size distributions are shown as determined on the samples (1,2,3 of set B) prepared by increasing texturization times in IPA-free KOH solution (see also Fig. 5). It can be clearly seen that an intermediate duration of texturization (20 min) leads to a size distribution with bigger pyramids (sample 2) compared with the size distributions on the samples (1) and (3) textured for 5 min and 40 min, respectively. Whereas on samples (1) and (3) pyramids with a base size bigger 10 µm² have a fraction of ≈ 6 % (5 min) respectively 2 % (40 min) the sample (2) with intermediate texture etch shows about 38 % in those classes. To characterize the size distribution the mean size of the pyramid base (≙ avg. size) and the fraction of the first three size-classes relative to the total area (≙ fraction of small pyramids) were deduced.

The statistical analysis of SEM images was applied to reveal the particular influence of the pyramid morphology on the reflection. Therefore we investigated the normalized reflection R_n as a function of the avg. size and the fraction of small pyramids. The results are shown in Fig. 8. Aside from IPA-free textured samples (red in Fig. 8) we also probed samples with different wet-chemical texture preparations resulting in bigger pyramids (green in Fig. 8). In Fig. 8a it is obvious that samples with mainly smaller pyramids (2 to 5 µm²) have a higher reflection than samples with larger pyramids (> 5 µm²), i.e., there is a clear decrease of the reflectivity with increasing pyramid size, as was reported already in [13, 14].

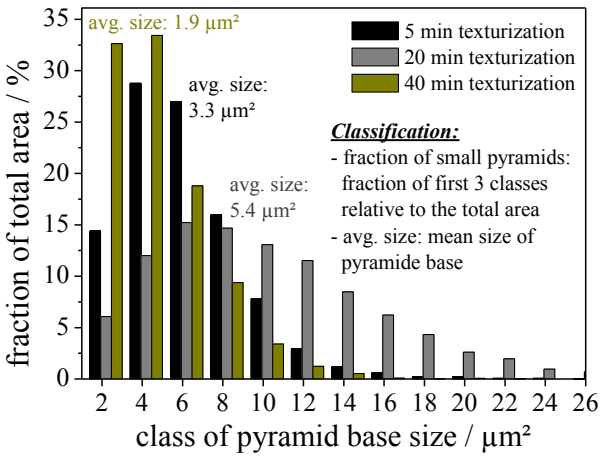

Fig. 7. Distribution of pyramid-sizes of samples (1,2,3 of set B) prepared with different durations of texturization.

Since it was observed that small pyramids exhibit a larger amount of horizontal facets (pyramid valleys), more light can be reflected directly. However, for samples which were not textured by IPA-free solutions this trend is reversed when the pyramids exceed a certain size. For these samples (avg. size: 25 µm² to 70 µm²) a slightly higher reflection compared to samples with 8 µm² is found.

The samples with different wet-chemical texture preparations fit well in the trend of R_n relative to the fraction of small pyramids (Fig. 8b). Low reflection losses can only be achieved with a low fraction of small pyramids. Lowest reflection corresponds to a fraction of small pyramids less than 20 %. For samples with a low amount of small pyramids there is a higher probability of light absorption due to the appearance of multiple reflections at the surface [15]. It is important to note that for the appearance of multiple reflections smaller pyramids surrounding bigger ones are necessary [15]. The clear correlation between R_n and the fraction of small pyramids as well as the integration of samples with bigger pyramid sizes in this trend leads to the finding that the reflection is mainly influenced by the size distribution rather than the absolute pyramid size.

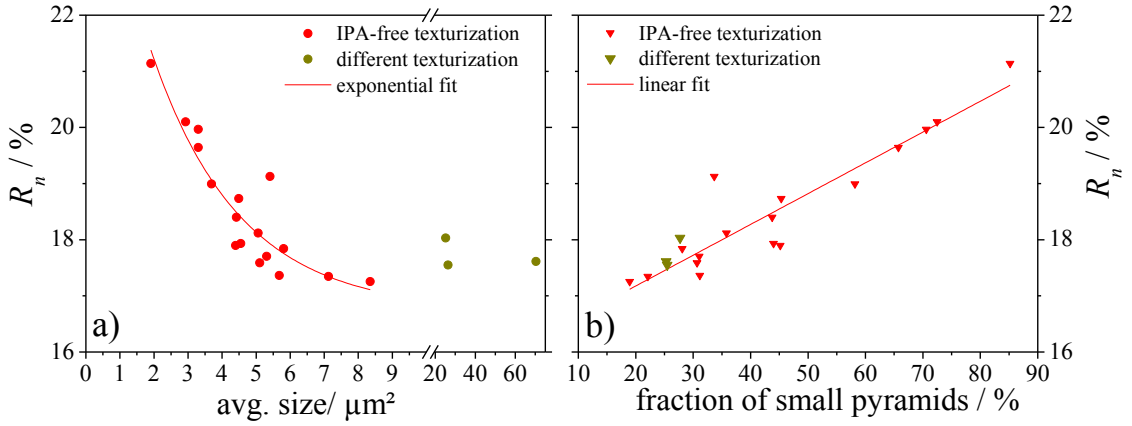

Fig. 8. Correlation between the normalized reflection R_n and a) average pyramid base size (avg. size) b), fraction of small pyramids.

4. Conclusion

In comparison to conventional texturization using IPA as an additive, our approach, the application of IPA-free texturization, benefits from a low density of surface states due to less occurrence of micro-roughness at the surface.

In our study it was found that an adequate saw damage removal is important to achieve homogenous and even surfaces. With an intermediate saw damage removal (i.e., 10 µm/side) the lowest densities of surface states are achieved. Longer SDE does not improve the electronic properties.

Optimal surface morphologies with respect to low reflection and recombination losses were achieved by a saw damage removal of ≈10 µm/side and subsequent texture etching in IPA-free KOH solution for intermediate duration of 10 to 20 min (i.e., 3.8 to 5.7 µm/side) resulting in average pyramid area sizes of 5 to 10 µm^2. On a-Si:H(i)/c-Si interfaces prepared on such textured substrate surfaces longest charge carrier lifetimes of τ_{eff} = 4 ms were achieved. Too long duration of texturization leads to pyramid elimination as well as to appearance of an increased fraction of small pyramids and to a corresponding increase of electronic surface state density and charge carrier recombination losses.

From the statistical analysis of SEM images the sizes and size distribution of the pyramids on textured silicon wafers were determined. Thereby it was shown that the reflection losses decrease with the

appearance of mainly bigger pyramids. Thus, the reflection is less influenced by the absolute pyramid size but more by the size-distribution. It is concluded that the fraction of small pyramids is the relevant parameter to describe the pyramid size-dependence of reflection losses.

Acknowledgement

The authors thank C. Klimm (Helmholtz-Zentrum Berlin) and K.-D. Wustig (HTW Berlin) for SEM image acquisition and A. Lawerenz (CiS Erfurt) for fruitful discussions. This work is part of the project "μ-Tex" and is supported by the HTW Berlin.

References

[1] H., Angermann, A. Laades, U. Stürzebecher, E. Conrad, C. Klimm, T.F. Schulze, K. Jacob, A. Lawerenz, L. Korte. Wet-chemical preparation of textured silicon solar cell substrates: Surface conditioning and electronic interface properties. *Solid State Phenomena* 2012;**187**:349-52

[2] http://www.gpsolar.de [Accessed: 20-Mar-2013].

[3] W. Kern, D. A. Puotinen. Cleaning Solutions Based on Hydrogen Peroxide for Use in Silicon Semiconductor Technology. *RCA Review* 1970; **31**:187-206.

[4] H. Angermann, J. Rappich, L. Korte, I. Sieber, E. Conrad, M. Schmidt, K. Hübener, J. Polte, J. Hauschild. Wet-chemical passivation of atomically flat and structured silicon substrates for solar cell application. *Appl. Surf. Sci.* 2008;**254**:3615-25.

[5] L Korte, E. Conrad, H. Angermann, R. Stangl, M. Schmidt. Advances in a-Si:H/c-Si heterojunction solar cell fabrication and characterization. *Solar Energy Materials and Solar Cells* 2009;**93**:905-10

[6] Mews, M.; Schulze, T. F.; Mingirulli, N. & Korte, L. Hydrogen plasma treatments for passivation of amorphous-crystalline silicon-heterojunctions on surfaces promoting epitaxy. *Applied Physics Letters* 2013;**102**:122106

[7] B. Stegemann, J. Kegel, M. Mews, E. Conrad, L. Korte, U. Stürzebecher, H. Angermann. Passivation of Textured Silicon Wafers: Influence of Pyramid Size Distribution, a-Si:H Deposition Temperature, and Post-Treatment. submitted to *Energy Procedia* 2013.

[8] B. Stegemann, J. Kegel, O. Gref, U. Stürzebecher, A. Laades, K. Wolke, C. Gottschalk, H. Angermann. Conditioning of Textured Silicon Solar Cell Substrates by Wet-Chemical Treatments. in 27th European Photovoltaic Solar Energy Conference 2012; pp. 547-51.

[9] K. Heilig. Messung der Oberflächen-Photospannung am Si und Ge. *Experimentelle Technik der Physik* 1968;**16**:138–48.

[10] R. Sinton, A. Cuevas. Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasisteady-state photoconductance data. *Applied Physics Letters* 1996;**69**:2510-3.

[11] H. Angermann, W. Henrion, M. Rebien, and A. Röseler. Wet-chemical preparation and spectroscopic characterization of Si interfaces. *Applied Surface Science* 2004;**235**: 322-9

[12] S. Olibet, C. Monachon, A. Hessler-Wyser, E. Vallat-Sauvain, S. De Wolf, L. Fesquet, J. Damon-Lacoste, and C. Ballif. Textured Silicon Heterojunction Solar Cells With Over 700 mV Open-Circuit Voltage Studied by Transmission Electron Microscopy. in 23rd European Photovoltaic Solar Energy Conference 2008; pp. 1140-4.

[13] H. Mäckel, D. M. Cambre, C. Zaldo, J. M. Albella, S. Sánchez, C. Vázquez, I. Sánchez, and M. Á. Vázquez. Characterization of monocrystalline silicon texture using optical reflectance patterns. in 23rd European Photovoltaic Solar Energy Conference 2008; pp. 1160-3.

[14] E. Fornies, C. Zaldo, J.M. Albella, "Control of random texture of monocrystalline silicon cells by angle-resolved optical reflectance. *Solar Energy Materials & Solar Cells* 2005;**87**:583-93.

[15] N. Bachtouli, S. Aouida, R. H. Laajimi, M. F. Boujmil, and B. Bessais. Implications of alkaline solutions-induced etching on optical and minority carrier lifetime features of monocrystalline silicon. *Applied Surface Science* 2012;**258**:8889–94.