Abstract

Over the past decade VLSI manufacturing industry flourishing very rapidly. Now a days hundreds and thousands of millions of transistors that are incorporated on a chip. As the circuit complexity increasing design for test circuitry also became more complex. These complex test circuitry heavily stressed to check the functionality of the CUT (Circuit under Test). Compared with normal functional mode, Power dissipation during test mode is much higher. Power dissipation during testing is more than twice compared with normal functional mode. Large Test data volume and High power consumption are the main problems in Design for Testability. This excessive power consumption is mainly due to switching of the scan cells. The technique proposed in this paper reduces switching activity in the scan cells there by the power consumption during testing can be reduced. In the proposed scan cell architecture some of the idle flip-flops are disabled during scanning using a control signal. By disabling idle flip-flops can be possible by an external control signal or with any internal signal. Excessive power consumption during testing may cause performance degradation and high system cost. These problems can be eliminated with the proposed scan cell architecture.

1. Introduction

As per Moore’s law the number of transistors that can be integrated is continuously growing and crossed millions of transistors. As the technology improving the circuit complex also increasing. In order to design such a complex circuits new design techniques should be adopted. Many design challenges are adopted for complex digital circuit
design. Low power design is the major design objective which is widely observed in communication and signal processing circuits. Now a days many digital systems working on battery power. Frequent charging of these portable devices may be burden for the users. Power source for charging those devices may not be available all the time. If those devices consume high amount of power frequent charging is required for them. Because of this high power consumption battery may be reduced. In order to overcome this problem now a days designers are concentrating more on low power design techniques. On the other hand power consumption during testing is much higher compared with normal he circuitry with the help of scan chains. In the scan chain the test vector is loaded serially bit by bit. While storing test vectors serially in the chain, bit by bit there are so many unwanted change states of the scan cells. Power consumption during testing may be measured with the switching activity of the scan cells. If these unwanted switching of scan cells are reduced power consumption in test mode also reduces.

Excessive power consumption during test mode is very much high compared with normal functional mode. There are so many techniques proposed for low power design during normal functional mode. C. Shi et al. (2004) stated that the power consumption during test mode is several times of normal functional mode. Sabaghian-Bidgoli et al. (2012) stated that Power dissipation in digital circuits during scan based test is generally much higher than that during functional operation. Now there was a need to develop low power test techniques. The main reason why the power consumption is high in test mode is, many test pattern generating circuits concentrate more on pattern minimization and low test time. These test patterns may cause high switching activity and results high power consumption during testing.

2. High Power Effects

Power dissipation in VLSI circuits is such an important issue when it comes with portable devices. Now a day’s portable device market increasing rapidly. These portable electronic devices depends on battery power. In battery operated devices power consumption matters a lot. According to Moore’s law the circuit complexity and functionality increasing rapidly. High complex circuits with heavy functionality demands high speed computations. As the VLSI technology is advancing the transistor size is decreasing. Scaling of transistors increases power consumption rapidly. While in the development of portable devices power consumption is the main criteria. Because it is very difficult to assemble huge battery packs inside a portable electronic device. Frequent recharging of the portable devices is also a big headache for the consumer. Industry demands more features for portable devices with low power consumption and with low cost. If the devices are attached with high performance battery packs, cost also increases. By considering all these effects low power consuming device development is greatly needed.

In the case of mobile phones consumer wants a smart mobile phone with lots of features. Mobile phone it should be sleek, slim and weight less. It should have high speed data transmission capability, high talk time and with many functionalities like camera, Bluetooth, NFC (Near Field Communication) etc. In order to fulfill all these demands these smart phones must be equipped with advanced processors. These advanced processors need high amount of power. When smart phone is used for multiple applications the peripheral devices that are assembled also more. In order to work with those peripheral devices complex integrated circuits are needed. These

Because of this high power consumption battery life may be reducing. Battery packed used for portable devices stressed heavily while testing such a high complex circuits. This effects the degradation of battery life. Another important issue with high power consumption is the temperature raise. If the raise is temperature raise above a threshold value the Integrated Circuit may damage in some of the circuits the circuit functionality may change with the effect for high temperatures above a threshold temperature. Next is the parameter that effected by high power consumption is yield loss. Due to high temperature traditional cooling techniques may not sufficient. Expensive cooling techniques may be used. They may increase the cost of the IC also the area occupied may affect the yield loss. Because of the excessive test power heat dissipated also high. In order to handle high temperature costly packaging is required. Plastic packaging is very much cheap compared to all other packaging techniques. But plastic packaging not able to withstand for high temperature. Traditionally used plastic packaging may not handle such a high temperature. Instead ceramic or any other packaging technique which can withstand at that high temperature can be used. Expensive packaging may lead to increase of chip cost. High temperature and current density may lead to circuit malfunctioning. Due to high temperature and current density caused by high switching activity in the testable electronic circuitry may lead to malfunctioning of the circuit under test.
3. BIST using Scan Cell

As the technology is increasing the VLSI circuits becoming more and more complex with improved functionality. In order to test these complex VLSI circuits is very difficult for a test engineer. Manual testing is not possible in the case of these complex VLSI circuits. Built in Self-Test (BIST) techniques may solve the problem of testing these complex circuits. Figure 1 shows the schematic diagram of a universal scan cell. By using two multiplexers in the scan cell, it can be operated in any of the four modes namely normal mode, Update mode, Capture mode and Shift mode. Output multiplexer used to select either the normal mode or update mode. When mode is zero it is in normal mode and the direct data in input is passed through the multiplexer data out signal. When mode is one indicates an update mode. Shift DR input signal is used to select capture mode or shift mode. When the Shift DR input signal is zero then direct data input is transferred to the D flip-flop. When the Shift DR input signal is one then it is called shift mode. Shift data that is coming from previous scan cell is stored in present scan cell.

![Schematic diagram of a Universal Scan Cell.](image)

In the Scan cell based testing circuits there are scan cells connected serially to form a scan chain. Each test pattern is loaded in to the scan cells serially into the scan chain. Main drawback of the scan chain architecture is unnecessary toggling of the flip-flops during loading of the test pattern. In test mode multiplexer selects data from the scan cells and during normal functional mode multiplexer select external data from the combinational circuit.

4. Power Analysis

In scan cell based testing each test pattern is loaded in to the scan chain serially. While loading test patterns serially in the scan cells those flip-flops toggles unnecessarily many times. Power consumption in scan based architectures mainly depends on the switching activity. In a CMOS circuit average power can be given as:

$$ P_{\text{avg}} = \frac{1}{2} C_L V_{dd}^2 N_T \frac{T}{T} $$

Where $C_L$ is the load capacitance, $V_{dd}$ is the supply voltage, $N_T$ represents the number transitions both rising and falling and $T$ is the time period. For a CMOS circuit at a given supply voltage power consumption can be reduced by reducing number of logic transitions. In Scan cell based testing the number of transitions are high there by power consumption also high. Many techniques have been proposed for minimizing power consumption with the minimization of number of transitions in scan cell. The technique proposed here in this paper can minimize power consumption effectively without effecting the test time and reliability.

When Scan In signal is enabled then the scan cell is in Shift mode. Scan data that is coming from previous scan cell is shifted to next cell. When Scan In signal is zero then the scan cell is in normal mode or capture mode depend on the mode selection input. In the shift and capture mode the Figure 2 shows the current drawn in the scan cell. Current drawn in the circuit shows the switching activity at each clock cycle. At each clock cycle transition the
current drawn can be observed high in Scan enable mode. When it is disabled and it is in capture mode also the high currents can be observed.

Fig. 2. Current drawn during shift and capture mode.

5. Modified Scan Cell

Switching activity in scan cells can be minimized using a control signal which can disable the second flip flop which is in idle state during shift operation. As long as the scan cell is in shift mode the second flip flop is in idle state. Until entire test pattern loaded serially in the scan chain second flip flop is in idle state. With an external control signal the flip flop can be disabled. If the flip flop is controlled by an external control signal the extra hardware necessary for the external control signal may be burden, which in turn increase the chip area. Second flip flop can be disabled by any one of the normal input signals in the scan cell.

Fig. 3. Modified Scan cell with a control input.

In this case ShiftDR select line is used as control signal. ShiftDR select line is used to enable or disable the second flip flop. When the shiftDR select line is high then the scan cell is in shift mode. The control signal is connected to a transmission gate as shown in figure 3. Here in this case ShiftDR select line is used as the control signal, and can disable the second flip flop using transmission gate. During shift mode, the transmission gate disconnects the second flip flop from the circuit. There by there is no transition in the second flip flop. This way number of transitions can be reduced. When in capture mode transmission gate sets a connection between first flip flop and second flip flop.
6. Experimental Results

Scan cell based test circuitry is designed and is verified using Xilinx ISE simulator. ISCAS’89 benchmark circuit S298 is used a benchmark circuit. For this benchmark circuit Scan cell based test circuitry is added. Complete logic is implemented using VHDL language and is simulated using Xilinx ISE simulator. There are 14 D flip flops in S298. Those D flip flops are replaced with the scan cells. Mode select line is used to select normal mode or update mode. ShiftDR select line is used to select capture mode or shift mode.

![Simulation results showing capture mode and Scan mode.](image1)

Figure 4 shows the simulation results when a scan cell is operated in capture mode or in shift mode. When the scan cell is in capture mode data coming from the external benchmark circuit is captured in the first flip flop. When the scan cell is in shift mode, scan data is loaded into the scan chain.

![Simulation results showing normal mode and update mode.](image2)

Figure 5 shows the simulation results of the scan cell when it is operated in normal mode and in update mode. In normal mode operation data coming from the external benchmark circuit is transferred. In update mode second flip flop is updated with scan data or input data. This type of architecture is not an optimized design. In modified scan cell architecture transmission gate structure is used to disable some flip flops in order to limit unnecessary transitions. Proposed architecture is implemented using Tanner S-Edit and the power consumption with benchmark circuits is calculated and is compared with both the architectures. Table 1 shows the comparative power analysis in the benchmark circuit by using traditional scan cell and the proposed scan cell.

<table>
<thead>
<tr>
<th>ISCAS’89 Benchmark circuit</th>
<th>Traditional Scan cell based arch.</th>
<th>Low power arch.</th>
<th>Percentage Power reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>S298</td>
<td>246.48</td>
<td>212.15</td>
<td>13.93%</td>
</tr>
<tr>
<td>S344</td>
<td>1520.48</td>
<td>1127.05</td>
<td>25.88%</td>
</tr>
<tr>
<td>S349</td>
<td>2324.15</td>
<td>1813.04</td>
<td>21.99%</td>
</tr>
</tbody>
</table>
7. Conclusions

In DFT test circuitry scan cell based approach is a popular one. In this scan cell based testing much of the power is due to unnecessary transitions in the shift mode. During shift mode the test pattern is loaded in to the scan chain serially. In each scan cell there is a flip flop idle during scan mode. Throughout this scan mode the second flip consumes some amount of power due to unnecessary toggling. This unnecessary toggling is avoided with the introduction of a control signal. Internal signal is used as the control signal so there is no area burden the chip. When the switching activity is reduced then the power consumption also reduces. As the circuit complexity is increasing the power reduction also increases. With the introduction of a new architecture for scan cell there is no effect on the fault coverage but the test time is somewhat increased due to increase in clock period.

References


