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Design of Low Power MAX Operator for Multi-Valued Logic System

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Abstract

A voltage-mode three transistor based MAX circuit for implementation of multi-valued logic (MVL) system is proposed in this paper. The proposed MAX operates at very low power consumption ranging in micro watts. To evaluate MAX performance, a NOR gate realization is done and compared to standard CMOS NOR gate. The HSpice simulation result confirms the MAX based NOR gate to operate with minimal delay at low power level. The simulations have been performed on 180nm technology.

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Keywords: Logic operator; multi-valued logic; logic realization

1. Introduction

Multi-Valued Logic (MVL) system has been used in the design of various logic and arithmetic systems, which also includes few special purpose digital processors, circuits of next generation quantum computers, signal encoding in long distant communication, efficient memory design, synthesis of combination and sequential circuits and many

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other in field of digital communications[1,2]. MVL circuitry also plays an important role in the synthesis of digital circuits as well as in the use of low power computing[3].

Over the last two decades, synthesis and simplification of logic functions has become a major research field. One of the most upcoming research topics is the multi-valued logic (MVL). It is defined as a non-binary logic and involves the switching between more than 2 states[4]. Moreover, it is better than binary as it can reduce the number of lines required for the parallel transmission of large amounts of data[5]. The binary logic realization with maximum effort of optimization still has a problem of increased hardware cost for bus connections compared to logic realization. With MVL synthesis, these problems can be solved to some extent[6-16]. According to Chowdhury, Raj and Singh , there are many methods to synthesis MVL as discussed[17]. Apart from that, the synthesis of MVL can also be done with other methods such as the Non-Zero Multi-Valued Decision Diagram[18], the neural network approach[19] and with the use of high deduction algorithm[20]. MVL can be used in the design of a number of logic systems, including memory, multi-level data communication coding and a number of special purpose digital processors[5,21]. In communications, Testing and Fault analysis field have recognized the potential of non-binary digital signal transmission by using MVL[5]. Arithmetic operator implementation and linear feedback registers were also prominent in the field of MVL[22]. MVL is also used in developing multiple-valued quantum logic and circuit for next generation quantum computing[23,24]. Arithmetic operators have also been implemented in MVL logic[22]. Combinational and sequential digital circuits are proposed in[14]. To achieve the reduction in required number of test cases for many practical design problems MVL system has been implemented[25].

In hardware, basic circuitry for multi-valued sequential logic is presented in by Gawande and Ladhake (2008)[26]. MVL circuits using complementary metal-oxide semiconductor (CMOS) technology have been successfully used in implementing a number of digital signal processing (DSP) applications[26,27-30]. Research has shown that current-mode MVL circuit implementation reduces power consumption[31-32]. If the MVL functions could be synthesized close to optimal level, it would be reduce the cost of circuit implementation. As of the most recent research the main aspect of MVL is to reduce bus connection and produce efficient circuit level logic component, MVL synthesis is highly important. MVL synthesis and realization is mainly observed through logic gates such as MIN and MAX. In this paper it is focused to realize the MAX operator in voltage mode with minimum number of transistors. Further to evaluate the advantage of using MAX in binary logic is done via NOR gate realization with respect to standard CMOS logic. The paper is divided into the following sections; section 2 covers short summary on MVL MAX operator. Section 3 details the proposed MAX circuit using three transistors and NOR gate realization. Simulation results are discussed in section 4 followed by conclusion in section 5.

2. MAX operator and its algebraic property

Consider an *m*-valued *y*-variable function f(x), where $x = \{x_1, x_2, \cdots, x_m\}$ and x_i takes on values from $R = \{0,1,2,\cdots, y-1\}$, where "*y*" is the radix. The function f(x) is a mapping $R = \{0,1,2,\mathrm{L}\ , y-1\}$. There are y^{y^m} different possible functions. If y = 3 and m = 2, then there are y^{y^m} , meaning 19683 possible existing functions available [22-24], [26] and [27]. A max (maximum) operator is defined as below, where a_n and b_n is a definite value and both of them are a member of set of all real values R[5,26,28-29,31,33-34]:

$$a_1, a_2, \cdots, a_n \in R\ ,\ b_1, b_2, \cdots, b_n \in R \text{ and } 0 \le \{a,b\} \le (y-1) \tag{1}$$

$$\max(a_1, a_2, \cdots, a_n) = a_1 + a_2 + \cdots + a_n \ \text{ and } \ \max(b_1, b_2, \cdots, b_n) = b_1 + b_2 + \cdots + b_n \tag{2}$$

Therefore,

$$\max(a,b) = a + b = a \cup b \tag{3}$$

And the maximum operator could be represented by the following relation:

$$\max(a,b) = \begin{cases} a & if \quad a > b \\ b & otherwise \end{cases} \tag{4}$$

where $a_1, a_2, \cdots, a_n \in R$, $b_1, b_2, \cdots, b_n \in R$ and $0 \le \{a,b\} \le (y-1)$

3. Proposed MAX circuit

The proposed circuit is shown in Fig. 1. It uses two PMOS (MP1 and MP2) and one NMOS (MN1) transistor. Under normal condition, the PMOS is ON when its source-to-gate voltage is greater than threshold voltage and in similar fashion NMOS require its gate-to-source voltage greater than threshold voltage. The MP1 transistor source terminal is connected to output node while the drain is connected to the gate of MP2. The gate of MP1 and MN1 are tied together as used for signal input A. The other signal input B is connected to gate of MP2. The source terminal of MP2 and drain terminal of MN1 are tied together. The body terminals of the respective transistors are tied to their source terminals to avoid threshold variation effect caused by bulk-to-source effect.

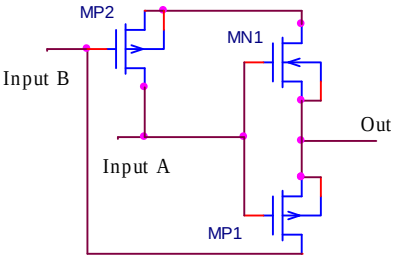

Fig. 1 *Proposed MAX circuit*

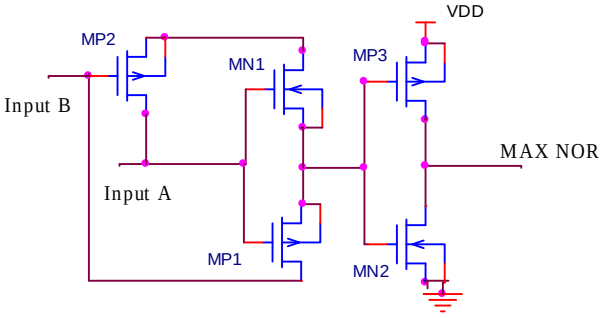

Fig. 2 *NOR gate realization using proposed MAX circuit*

The circuit uses two power supplies input A and input B. The mode of operation of each of these transistors is determined by the voltage difference between these input signals. Depending on the magnitude of whichever signal input is higher the output track the input. Further using the MAX circuit, a NOR gate realization is done shown in Fig. 2 and is compared with conventional CMOS NOR gate.

4. Simulation results

The proposed MAX circuit simulation has been performed on HSpice on 180nm technology. The W/L ratio of MOS transistors used in all circuits is kept at its minimal value which is 0.24u/0.24u. The simulation result of Fig. 1 and Fig. 2 is shown in Fig. 3 and Fig. 4 respectively. In Fig. 4, the NOR gate realization done using proposed MAX operator is compared with conventional CMOS NOR gate.

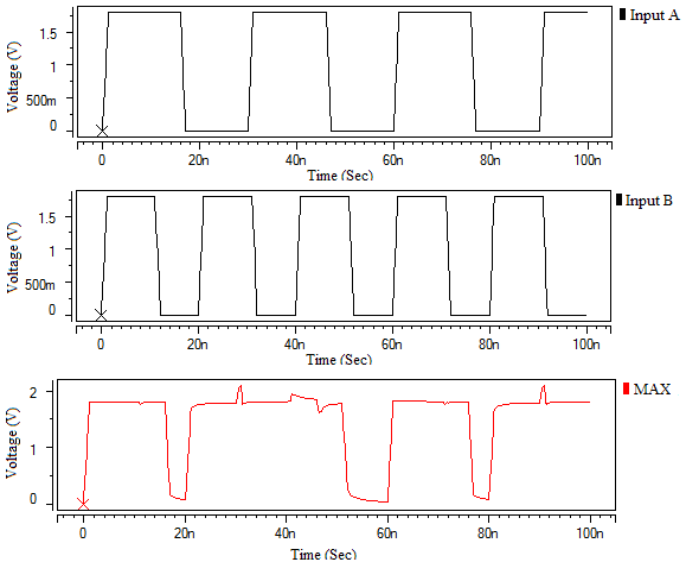

Fig. 3 *Simulation result of proposed MAX operator*

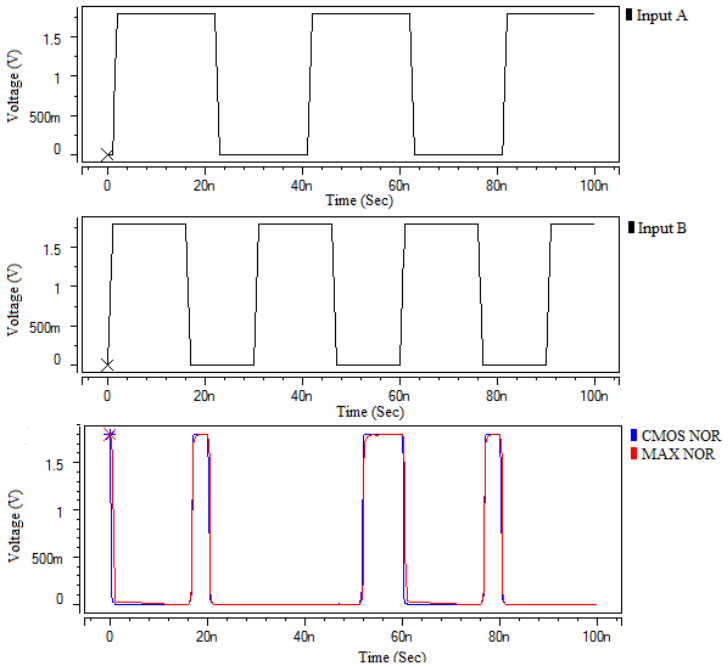

Fig. 4 *Simulation result of NOR gate: using CMOS and proposed MAX operator*

To evaluate the advantage of using MAX based NOR gate, is shown in fig. 5 where a single pulse is analyzed for delay response. From plot it become quite clear that the MAX based realization results in minimal delay and requirement of less current extraction from supply voltage makes the circuit to reduce power consumption by 50 percent. The comparison results for delay and power is shown in table 1.

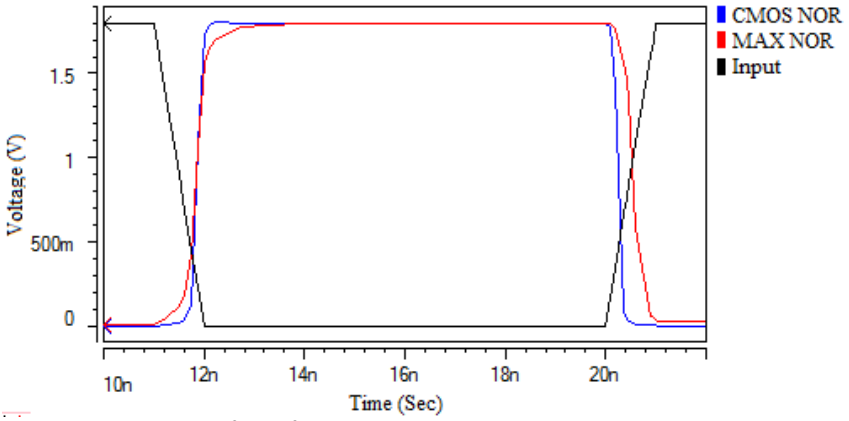

Fig. 5 *Analysis of delay for NOR gate: using CMOS and proposed MAX operator*

Table 1. Performance comparison of NOR gate

Logic	Transistor count	Rising delay (*nS*)	Falling delay (*nS*)	Power (*uW*)
CMOS	4	0.45	0.28	13.4
Proposed MAX based	5	0.35	0.006	10

5. Conclusion

A voltage-mode three transistor based MVL circuit is proposed in this paper. Using less count of transistor is not only effective in terms of area saving but also speed-up the circuit due to less presence of parasitic capacitances. Since, MAX is a basic operator for synthesizing MVL function so with optimized MAX operator can do fast realization with increased efficiency. An effective use of this operator is shown by realizing NOR gate and its comparison with standard CMOS NOR gate.

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