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Title: A Flexible Front-End Signal Processor for High-Speed Image Sensor Readout

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Corresponding Author: Dr Carl Grace,

Corresponding Author's Institution: Lawrence Berkeley National Laboratory

First Author: Carl Grace

Order of Authors: Carl Grace; Dario Gnani, MS; Jean-Pierre Walder, MS; Bob Zheng, BS

Abstract: The High-Speed Image Pre-Processor with Oversampling (HIPPO) is a prototype image sensor readout integrated circuit designed for both high performance and enhanced flexibility. HIPPO's initial target application is the instrumentation of bufferless, column-parallel, soft x-ray Charge-Coupled Device (CCD) image sensors operating at column rates up to 10 MHz, enabling 10,000 frames-per-second (fps) video rates. HIPPO's architecture is flexible and allows design tradeoffs between speed, accuracy, and area. This architectural flexibility will enable the fast development of related image sensor and particle detector readout ICs based on HIPPO technology. HIPPO contains 16 channels, each comprising a charge amplifier, a dual-slope correlated double sampler, a sample-and-hold, a multiplexed 12b, 80 MS/s pipelined ADC (one ADC for every 4 channels), and a 480 Mb/s output serializer.

HIPPO achieves 35 e- read noise at 10,000 fps for a 1 Mpixel sensor, improving to 24 e- at 5000 fps. HIPPO's charge-domain input obviates the source follower amplifier used in most CCDs and enables the implementation of a fully column-parallel CCD architecture. HIPPO was specifically designed to be flexible in both the sequencing of its operations and in its ability to accommodate input rates potentially varying over an order of magnitude.

Response to Reviewers: Reviewers' comments:

Reviewer #1: This article describes a powerful new ASIC for fast, column parallel readout at 10MHz rates, enables 10k frames/second for bideo rates of Mpixel CCD arrays. On-chip ADC, shared ADCs and CDS capabilities make this a very promising and flexible device for future applications. Respectable noise rates are demonstrated in simulation. However an obvious deficiency is a lack of fabricated measurements to verify simulations. The paper is generally very clearly written and easy to follow. However it does, in places, descent into jargon and presupposes a level of circuit topology understanding that might be understandable for a JSSC article, but is perhaps a bit too much for NIM.

It is recommended that the following revisions be made to further improves the paper:

 doi:10.1016/j.phpro.2012.02.491

1) Citations should be provided to specific circuit topologies, as it is difficult to follow otherwise. Specifically, on page 4:

a) what is the architecture of the "switched Miller capacitor bank" in amplifier A1 ?

b) it is not at all clear what constitutes a "switched symmetrical transconductance" topology

RESPONSE TO REVIEWER COMMENT NO. 1: I have clarified the meaning of "switched Miller Capacitor bank". I have added a reference to the literature to explain the symmetrical transconductance topology.

2) Some of the data plots that are clearly made in Excel suffer from poor presentation (e.g. x-axis overwritten in Fig. 9), not up to the usual standards of a scholarly article.

RESPONSE TO REVIEWER COMMENT NO. 2:

I have replotted the data from the Excel plots in MATLAB. It is the same information but it is now presented in a manner fitting the scholarly standards of TIPP.

3) In a number of figures, the fonts are simply too small to read (e.g. Fig 11, Fig 12, 13)

RESPONSE TO REVIEWER COMMENT NO. 3:

Where possible, I have redrawn the figures with larger fonts. In several cases the figures were simulation output from a software tool where it is not possible to adjust the font size on the axes. In these cases, I explained the meaning of the axis markers in the figure text.

4) Page 8, can the magnitude of the additional load, described in the last sentence on this page as "small" be quantified?

RESPONSE TO REVIEWER COMMENT NO. 4:

I quantified the term "small" by indicating it was small relative to the input capacitance of the Sample-and-Hold amplifier.

5) Perhaps Fig. 10 would be clearer if the clocking/timing diagram of the SHA were explicitly shown?

RESPONSE TO REVIEWER COMMENT NO. 5:

I added a new figure, labeled figure 5, that shows the clocking and timing diagram of the SHA explicitly.

6) A modest number of suggested, small text changes can be provided if the author would like.

RESPONSE TO REVIEWER COMMENT NO. 6:

As I do not know the identity of the reviewer, I was unable to make these small changes. However, I did read the manuscript with fresh eyes and made small changes throughout to enhance clarity.

It should not require much effort to address these issues and will hopefully lead to a clearer paper.

First page corrections:

Please make the following minor changes in front page:

(1) Conference Title:

"TIPP 2011 - Technology and Instrumentation in Particle Physics 2011"
(2) Copyright:
{(c) copyright symbol} "2011 Published by Elsevier Ltd. Selection and/or peer-review under responsibility of the organizing committee for TIPP 2011"

RESPONSE TO REVIEWER COMMENT FIRST PAGE CORRECTIONS:

The requested corrections have been made.

TIPP 2011 - Technology and Instrumentation in Particle Physics 2011

A Flexible Front-End Signal Processor for High-Speed Image Sensor Readout

Carl Grace, Dario Gnani, Jean-Pierre Walder, and Bob Zheng

Lawrence Berkeley National Laboratory,One Cyclotron Road, Berkeley, CA 94720 USA

Abstract

The High-Speed Image Pre-Processor with Oversampling (HIPPO) is a prototype image sensor readout integrated circuit designed for both high performance and enhanced flexibility. HIPPO's initial target application is the instrumentation of bufferless, column-parallel, soft x-ray Charge-Coupled Device (CCD) image sensors operating at column rates up to 10 MHz, enabling 10,000 frames-per-second (fps) video rates. HIPPO's architecture is flexible and allows design tradeoffs between speed, accuracy, and area. This architectural flexibility will enable the fast development of related image sensor and particle detector readout ICs based on HIPPO technology. HIPPO contains 16 channels, each comprising a charge amplifier, a dual-slope correlated double sampler, a sample-and-hold, a multiplexed 12b, 80 MS/s pipelined ADC (one ADC for every 4 channels), and a 480 Mb/s output serializer.

HIPPO achieves 35 e- read noise at 10,000 fps for a 1 Mpixel sensor, improving to 24 e- at 5000 fps. HIPPO's charge-domain input obviates the source follower amplifier used in most CCDs and enables the implementation of a fully column-parallel CCD architecture. HIPPO was specifically designed to be flexible in both the sequencing of its operations and in its ability to accommodate input rates potentially varying over an order of magnitude.

Keywords: Analog, Instrumentation, Charge-Coupled Device, Data Conversion, Digitizer, Imaging, Integrated Circuit

1. Introduction

The High-Speed Image Preprocessor with Oversampling (HIPPO) is an integrated system for solid-state imager readout. HIPPO is designed for both high performance and enhanced flexibility compared to earlier integrated readout systems. Emerging particle detection and scientific imaging applications require greatly increased readout rates to enable the capture of dynamic processes. Future x-ray light sources, for example, will require instrumentation that digitizes at pixel rates in excess of 100 Gpixel/s [1]. Its initial application will be the instrumentation of thick, fully depleted, column-parallel soft x-ray charge-coupled devices (CCDs) operating at column rates up to 10 MHz, enabling 10,000 frames-per-second (fps) video rates for 1 Mpixel square sensors. HIPPO's flexible architecture allows design tradeoffs between speed, accuracy, and area. This architectural flexibility will enable rapid development of related image sensor and particle detector readout integrated circuits (ICs) based on HIPPO technology.

Conventional CCDs provide excellent performance due to their low noise and nearly lossless charge transfer. Figure 1 shows a schematic diagram of a traditional 3-phase CCD. The three clock phases are operated without overlap to shift the charge packets toward the output amplifier. At the end of the clocked MOS capacitor array, the output charge packet is dumped onto a floating diffusion. The voltage at this diffusion is buffered off-chip by an output amplifier. This on-chip output amplifier is typically implemented in a source follower configuration. The output speed of the CCD is usually limited by this amplifier as the CCD manufacturing process is not optimized for MOSFETs and because of architectural challenges associated with parallelizing the columns. Therefore, HIPPO is designed to instrument column-parallel CCDs without on-chip output buffer amplifiers.

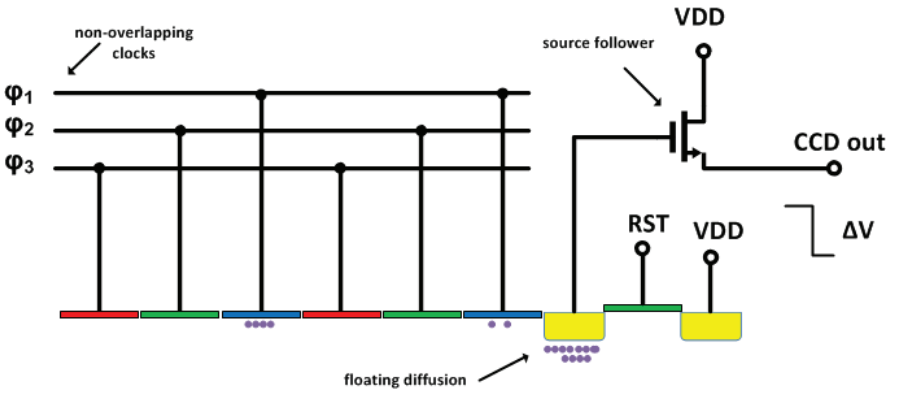

Figure 1. Schematic diagram of a conventional charge-coupled device.

These bufferless CCDs are clocked at a column rate of up to 10 MHz. A schematic diagram of the output of a bufferless, column-parallel CCD is shown in Figure 2 Instead of a buffer amplifier, the output of the bufferless CCD is a floating diffusion, which means that HIPPO reads out the signal charge packet destructively. In order to do this successfully at the requisite 10 MHz rate, the input stage of HIPPO must be charge-sensitive, fast, low-noise, and capable of accepting and returning to the CCD large amounts of charge during its reset phase (the transfer gate charge injection of approximately 200 ke-), while still sensing small signal charge packets.

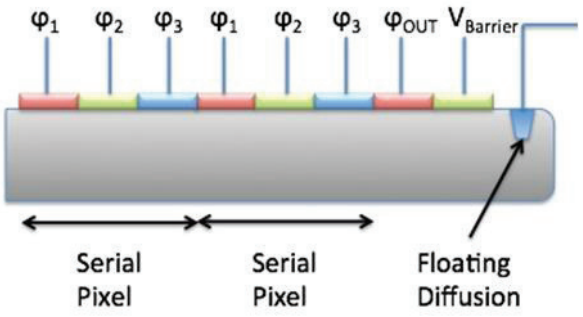

Figure 2. Schematic diagram of bufferless CCD output structure.

2. HIPPO Channel

Within HIPPO, the CCD output charge is read out directly (without on-CCD voltage buffering) using the signal chain shown in Figure 3. The signal chain comprises a charge-domain preamp, a single-ended-to-differential converter, cross-coupled switches for implementing continuous-time correlated double-sampling (CDS), a fully differential, continuous-time integrator, a fast-settling sample-and-hold amplifier (SHA) and a Pipelined ADC. The ADC is multiplexed between four signal conditioning channels. Because the ADC also implements oversampling, it operates at a sampling rate that is greater than the rate of the channel by a multiple of four. The sampling rate difference between the channel and the ADC determines the oversampling ratio and is programmable. The HIPPO channel itself operates at a rate of between 625 kHz and 10 MHz. In the HIPPO prototype, channels are grouped in sets of four with each group sharing a single ADC. This is done in order to match the pitch of the ADC with the column pitch of the CCD.

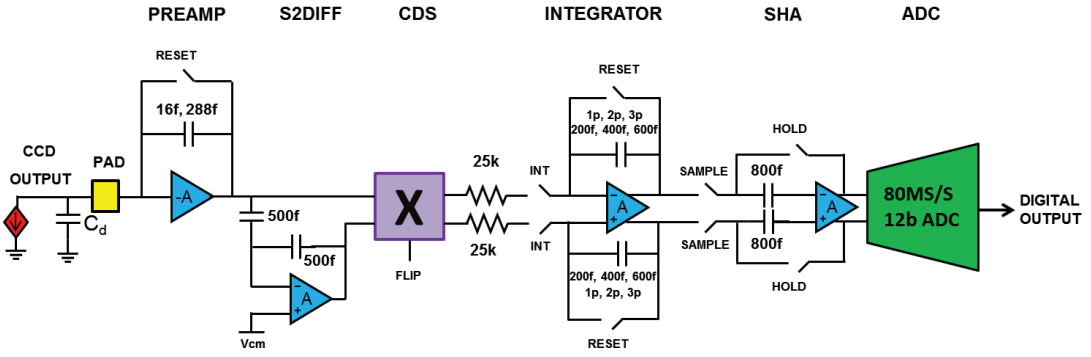

Figure 3. HIPPO signal chain.

The channel is controlled by a digital state machine that generates the timing signals shown in Figure 4. After it is reset, HIPPO integrates the reset level of the CCD. The CDS circuit is idled when the CCD

video signal is processed by the preamp. Then, the CDS integrates in the opposite direction to cancel the reset noise of the CCD. Finally, the output of the CDS is sampled by the SHA and sent to the ADC.

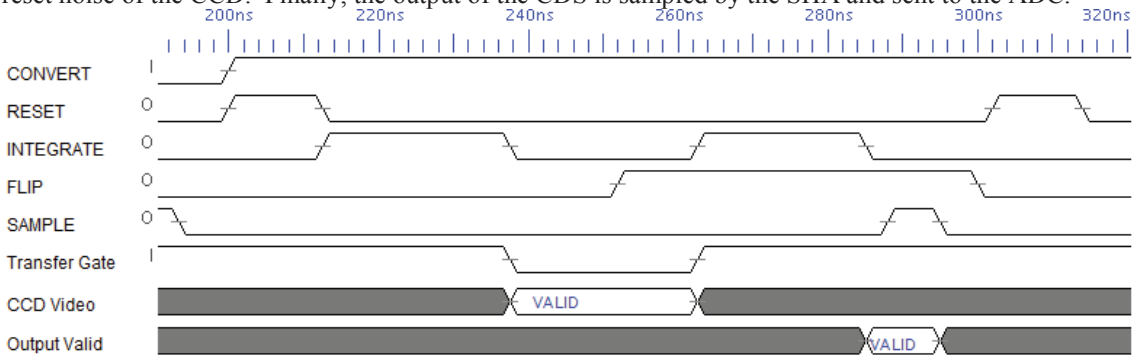

Figure 4. HIPPO timing diagram. This diagram assumes a channel rate of 10 MHz.

3. HIPPO Preamp

A block diagram of the preamplifier is shown in Figure 5. The main strategy is transimpedance amplification. The signal path comprises a two-stage, Miller-compensated, transconductance amplifier labeled A1, with capacitive feedback to convert input charge to output voltage. The first stage of this Miller amplifier consists of a folded cascade differential pair in order to increase the power-supply rejection ratio over the bandwidth of the preamplifier. A set of switches, S1a and S1b, allows the gain setting to be changed from a 50 ke- and a 1 Me- full-scale range. To preserve loop stability, different values of Miller capacitance are used inside amplifier A1 depending on the gain setting.

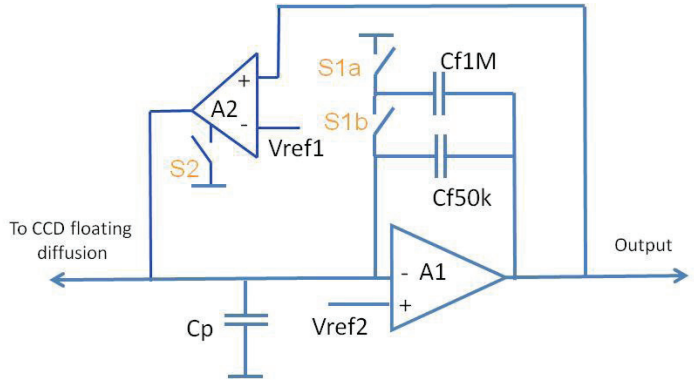

Figure 5. Block diagram of HIPPO preamp.

A second transconductance amplifier [2] (A2) is used to reset the preamplifier feedback capacitance. It uses a switched symmetrical transconductance topology. The circuit is switched in the sense that it is powered down when not in use to reduce DC power dissipation. Two external reference voltages set the DC output of the preamplifier. The capacitor Cp represents all the parasitic capacitance present at the input (i.e. bonding wire, bonding pads, and CCD floating diffusion). Under nominal conditions, the full scale voltage at the output of the preamplifier ranges from 850 mV to 350 mV. The preamplifier uses large devices biased in moderate inversion to provide low thermal noise, but cannot remove the kT/C

noise introduced by the reset amplifier or the reset noise introduced by the CCD. To lower the total noise, the preamplifier drives a correlated double-sampling circuit described in the next section.

Figure 6 shows a simplified schematic of the preamp main amplifier (A1 in Figure 5). The single-ended output of the CCD is sensed by differential pair MN1 and MN2. While differential sensing increases the input noise, it greatly improves the ability of the preamp to reject noise on the negative power supply. The differential pair does this by transforming noise on the negative power supply into a common-mode signal. This is critical here because the gain seen by the negative supply of a single common-source device is the ratio of the input capacitance to the feedback capacitance (in this case approximately 64). Even low-amplitude noise on the negative power supply in this case would render the preamp inoperable in the sense it would be impossible to separate the signal from power supply bounce.

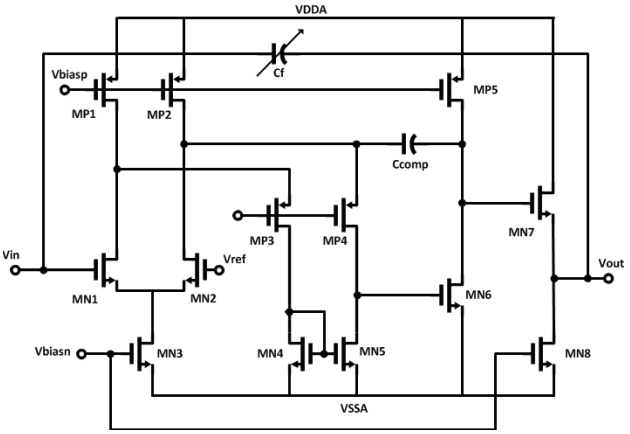

Figure 6. Simplified schematic of preamp main amplifier.

The output of the differential pair is folded to increase swing and then drives common-source amplifier MN6 and MP5. The output is then buffered by the source follower consisting of MN7 and MN8. The output is fed back to the input through capacitor Cf. Cf can be adjusted to implement different gains. The charge gain of the preamp, in the limit of large open-loop gain, is approximately 1/Cf. The feedback capacitor Ccomp is used to implement cascode compensation by feeding back a portion of the output signal to the folding node.

Because the reset time allowed for the preamp in the highest channel rate case is so small, an active reset circuit as described above is required. The feedback reset OTA is used to reset the main amplifier. The OTA uses a symmetrical architecture for efficiency is energized only when the preamp is being reset. Because a low transconductance is required here for noise purposes, the devices are biased with large drain-source voltages.

The linearity performance of the preamp in 50 ke- mode and with a 100 ns integration following the output is shown in Figure 7. The peak nonlinearity (at full-scale) is less than -0.15 bit at a 10-bit level, indicating that the preamp is capable of approximately 12-bit linearity performance in this mode. The linearity is degraded somewhat in the higher gain modes.

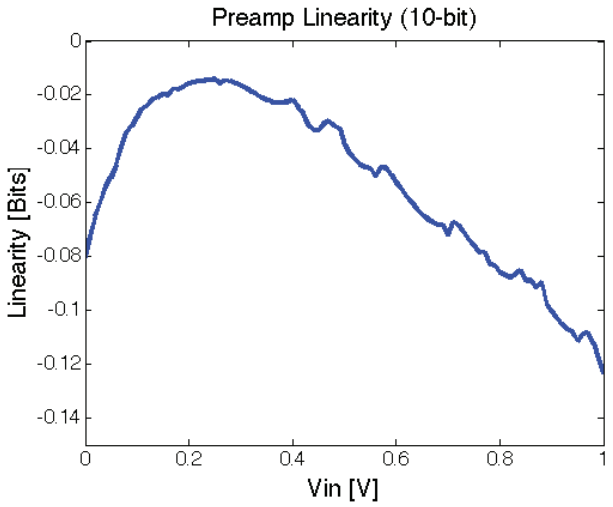

Figure 7. Preamp linearity in bits at a 10-bit level. The integration period is 100 ns and preamp is in 50k e- mode. The simulation was run at room temperature using the nominal process corner.

4. Correlated Double-Sampler and Gated Integrator

To remove the reset noise from the CCD and the preamplifier reset amplifier, HIPPO uses continuous-time dual-slope correlated double-sampling (CDS). CDS is a powerful, widely used technique to suppress reset noise in solid-state imagers. The basic concept is to take two samples of the CCD output: the first after the CCD is reset and the second when the signal charge packet is available at the CCD output. Since the charge injection from the reset operation is common to both samples, taking their difference can reject the charge injection while retaining the signal. Typically, the CDS technique is implemented using switched-capacitor techniques. However, in the case of low-noise scientific imaging, the residual kT/C noise from the sampling capacitors typically used to implement CDS would limit the performance of the channel. Therefore, HIPPO uses the continuous-time dual-slope technique to implement CDS. A block diagram of the concept of cascading a charge preamp with a gated integrator is shown in Figure 8.

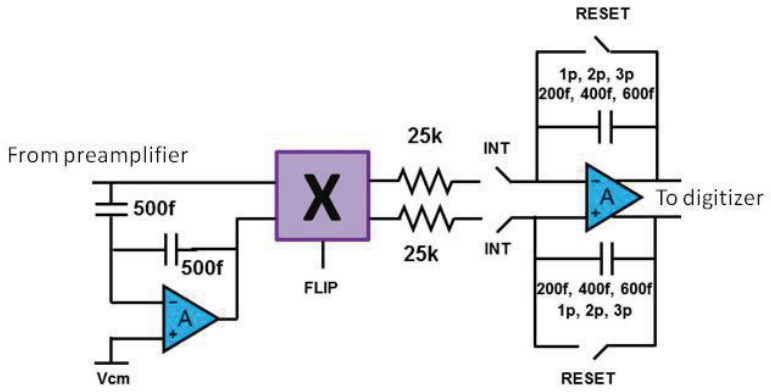

Figure 8. Block diagram of CDS and integrator circuits.

The CDS is implemented using fully differential circuits to improve both the signal-to-noise ratio at the integrator output and to be compatible with the digitizer which samples its output. The single-ended output of the preamplifier is converted to differential by sending the preamp output through two paths. One path goes directly to the integrator's inverting input and the other goes through a unity-gain inverting amplifier before it reaches the integrator's noninverting input. Because the inverting amplifier has finite bandwidth, the phase difference between the two signals is not exactly 180 degrees, but since the channel rate is limited to 10 MHz, the phase mismatch does not significantly affect the CDS performance. Three different integration periods are available: 50 ns, 100 ns, and 150 ns. These different integration periods provide the same level of reset noise rejection but provide thermal noise rejection proportional to the time spent integrating. There are diminishing returns here with respect to longer integration times because half the integration is spent accumulating noise, rather that rejecting it. Figure 9 shows the linearity of the integrator after parasitic extraction. The integrator displays better than 10-bit linearity.

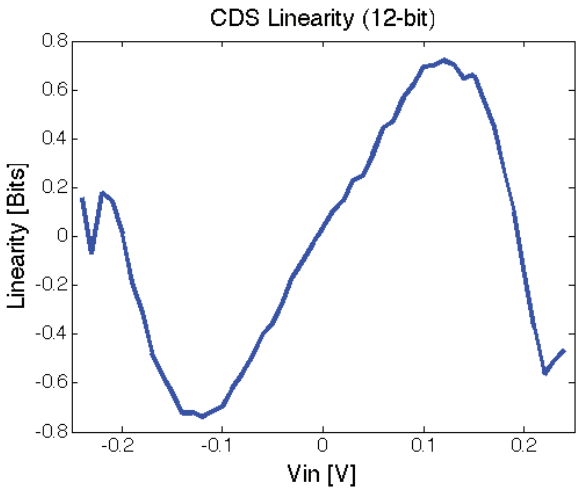

Figure 9. Linearity of the CDS circuit. The integration period is 100 ns. The simulation was run at room temperature using the nominal process corner.

5. Analog-to-Digital Converter

The HIPPO ADC digitizes the output of the integrator to give a digital output that is proportional to the magnitude of the input charge packet. A block diagram of the ADC is shown in Figure 10. The ADC uses a pipelined architecture. It consists of 11 identical stages, each of which contains a low-resolution 1.5-bit analog-to-digital subconverter (ADSC), a 1.5-bit digital-to-analog subconverter (DASC), an analog subtractor, a sample-and-hold amplifier (SHA), and a gain stage [3].

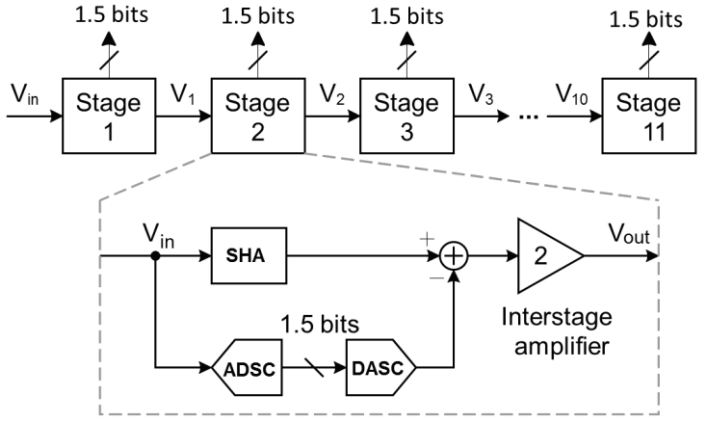

Figure 10. ADC block diagram.

A timing diagram for the ADC is shown in Figure 11. The SHA for each odd stage acquires the input signal on φ_1 and the odd stages generate residues on φ_2. The phases are reversed for the even stages. The ADSCs make their decisions during the non-overlap time.

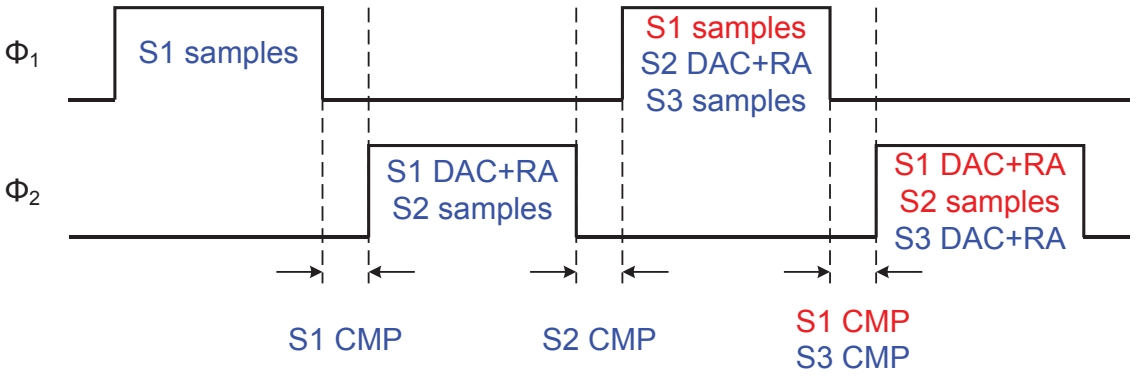

Figure 11. Timing diagram for ADC.

6. HIPPO Layout

The layout strategy for the HIPPO core is shown in Figure 12. Each of the preamps, CDS circuits, and SHAs is laid out on a 200 µm pitch. To maintain a 50 µm channel pitch to match the CCD, four of each circuit is placed in a row and the outputs are then fed to the ADC. This has minimal impact on performance, since the additional load driven by the preamp due to stacking of circuit blocks is small relative to the input capacitance of the CDS circuit it is driving.

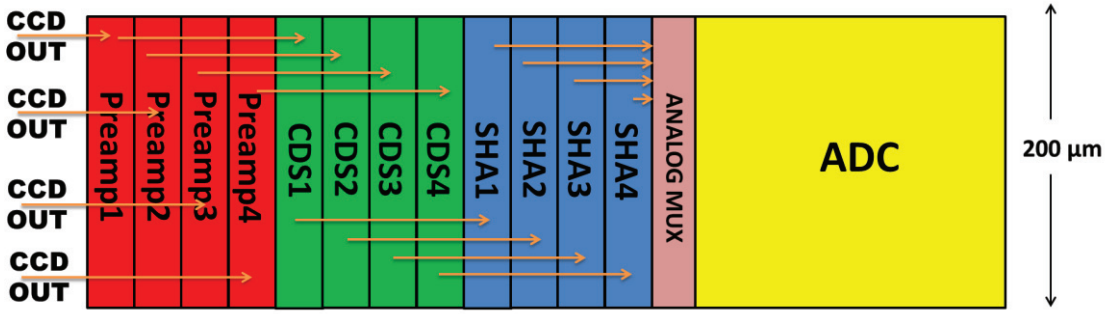

Figure 12. Layout strategy for HIPPO core.

7. Performance

An extracted simulation of the channel front end is shown in Figure 13. The simulation was done for the 50 ke- gain mode. The output noise level here is about 37.5 e-. At half speed (5000 fps) the output noise level is 24 e-. A full-chip, extracted simulation is shown in Figure 14. At time of writing, the fabricated HIPPO prototype is undergoing bench testing.

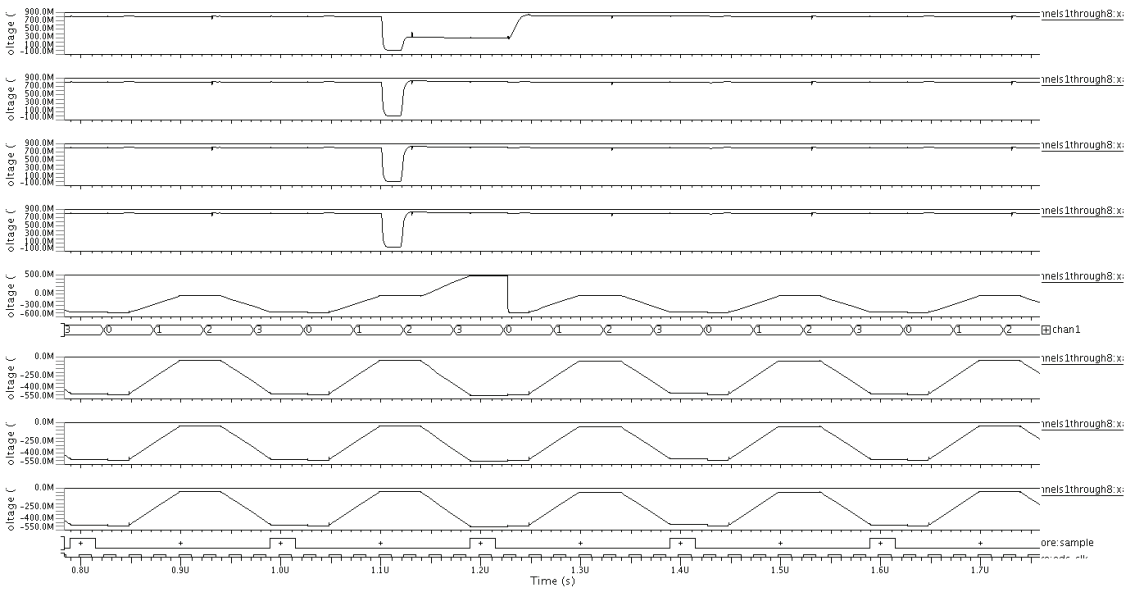

Figure 13. Extracted simulation of channel front end. The top four traces are the first four preamps and the bottom four traces are their corresponding integrators. The y-axes span -500 mV to 500 mV and the x-axis is from 0 to 1.8 µs.

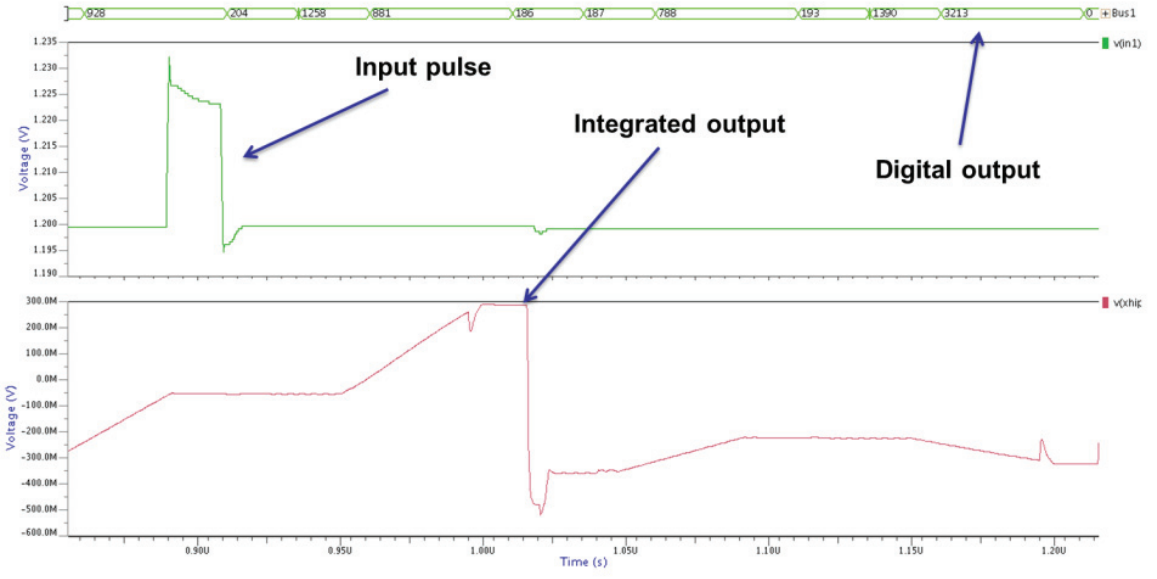

Figure 14. Full-chip simulation of parasitic extracted HIPPO (including pads). The top y-axis spans 1.19 V to 1.235 V. The bottom y-axis spans -600 mV to 300 mV. The x-axis spans 0.8 µs to 1.25 µs.

The die photo of the 65 nm HIPPO IC is shown in Figure 15. The simulated extracted performance of the IC is summarized in Table 1.

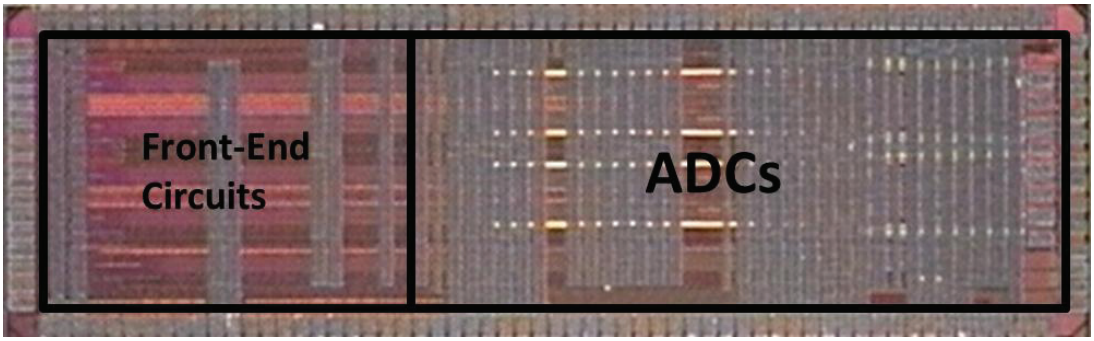

Figure 15. Annotated HIPPO die photo.

Requirement	Value	Comment
Channel Rates	10, 5, 2.5, 1.25	MHz
ADC Rates	80, 40, 20, 10	MHz
Input Noise	35 e-	Max Speed
	24 e-	Min Speed
Full Scale	50e3/1e6 e-	Mult gain steps
Output Resolution	12	Bits
Linearity	0.5 LSB	10-bit level
Technology	65 nm CMOS	

Table 1. Simulated HIPPO performance.

8. Conclusion

HIPPO, a front-end signal processor for column-parallel CCD readout implemented in 65 nm CMOS technology, is presented. It achieves achieves 35 e- read noise at 10,000 fps for a 1 Mpixel sensor, improving to 24 e- at 5000 fps. The IC enables the readout of bufferless, column-parallel, soft x-ray Charge-Coupled Device (CCD) image sensors.

References

[1] J.N. Corlett, et al., "Design Studies for a VUV soft X-ray FEL Facility at LBNL" *Proceedings of IPAC* 2010, Kyoto, Japan

[2] J. Crols and M. Steyaert, "Switched-Opamp: An Approach to Realize Full CMOS Seitched-Capacitor Circuits at Very Low Power Supply Voltages" *IEEE Journal of Solid-State Circuits* Vol. 29 no. 8 August 1994

[3] S.H. Lewis, et al., "A 10-b 20-Msample/s Analog-to-Digital Converter" *IEEE Journal of Solid-State Circuits* Vol. 27 no. 3 March 1992

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