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Preface

As chips grow in speed and complexity, global control of an entire chip using a single clock is becoming increasingly challenging. In the future, multi-core and large-scale systems on chip (SoC) designs are therefore likely to be composed of several timing domains. Global asynchrony and local synchrony (GALS) is emerging as the paradigm of choice for SoC design with multiple timing domains. In GALS systems, each timing domain is locally clocked, and asynchronous communication schemes are used to glue all of the domains together. Thus, unlike purely asynchronous design, GALS design is able to make use of the significant industrial investment in synchronous design tools.

There is a significant need for formal methods for GALS systems. In synchronous designs, formal methods and design automation have played an enabling role in the continuing quest for chips with ever greater complexity. Due to the inherent subtleties of asynchronous circuit design, formal methods are likely to be vital to the success of the GALS paradigm. This workshop aims at bringing together researchers from different communities interested in GALS design, and in applying formal methods in creating CAD tools enabling correct by construction GALS design.

In 2003, the first FMGALS workshop was held in conjunction with Formal Methods Europe (FME 2003) conference. This one-day workshop brought together researchers from Europe, Asia and the U.S. to discuss various research directions and to share the then state-of-the-art in GALS design. The proceedings of the FMGALS 2003 workshop was published informally, and was followed through by a special issue of the Kluwer Journal on Formal Methods in System Design. The special issue is scheduled to be published late 2005. The FMGALS 2003 was quite successful, with 5 invited talks, and 9 contributed papers. The proceedings can be downloaded from
http://filebox.vt.edu/users/shukla/fmgalsproc.pdf.

The FMGALS 2005 workshop featured an invited talk by Professor Alberto

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Sangiovanni-Vincentelli from University of California at Berkeley. There were 10 contributed papers, of which seven were full-length with 25 minutes of presentation time, and the remaining three have shorter 15-minute presentations.

There were three regular paper sessions at FMGALS 2005. Session I featured the first paper about a specific GALS based crypto ASIC design, which provided insights obtained by the authors during a real design. The second and the fourth papers were about verification of GALS designs and Latency Insensitive Protocols (LIPs) respectively, and the third is about formal modeling of the relay-station approach for LIPs. The second contributed session contained two papers, one on LIP implementation and dealing with back-pressure, and the other one on a process-algebraic verification technique for asynchronous designs, which may be of interest to GALS researchers. The third and the final contributed session contained four papers. The first paper in this session described an extension of LIP with multiple clocks, and wrapper synthesis. The second one was an interesting case study done at Intel, in designing a GALS based test chip. The third paper was on how to design delay-insensitive circuits from a specially characterized design termed "weakly endochronous." Finally a survey of desynchronization techniques in synchronous paradigms concluded the sessions. A Panel discussion ended the workshop with interesting and lingering questions on the future of Formal Methods applications in GALS design.

Although the sessions were a bit unstructured in terms of themes of the sessions, we believe that the papers exposed the audience to a wide range of efforts being undertaken in the general area of GALS design, and specific area of formal approaches to GALS design. We also believe that like its previous incarnation, FMGALS 2005 allowed researchers to start dialogues, identify problem areas, and lead to interesting collaborative research in the near future.

We would like to thank several people who helped make FMGALS 2005 possible. First, we would like to thank the MEMOCODE committee for hosting FMGALS 2005 as a part of the ACM/IEEE MEMOCODE 2005 conference. We also thank ACM SIGDA and ACM SIGARCH for agreeing to accord the "in cooperation" status to FMGALS. Prof. Franco Fummi and his colleagues deserve special thanks for all the local arrangements and the hosting of the workshop in the beautiful city of Verona. Special thanks are also due to Prof. Alberto Sangiovanni-Vincentelli for agreeing to travel to this workshop and give the invited talk. The program committee members who worked hard to provide at least three in-depth constructive reviews for each submitted paper are acknowledged for their hard work and enthusiasm. But most of all, we gratefully acknowledge the interest and support of all the authors and the

attendees, whose contribution made this a high-quality workshop.

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Sandeep K Shukla
General Chairs

Montek Singh
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