Thermal Management in 3-D Integrated Circuits with Graphene Heat Spreaders

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Abstract

In this paper, we performed thermal analysis in three-dimensional (3-D) chip built on silicon-on insulator substrate. Since heat dissipation is one of the most serious issues in 3-D electronics, efficient thermal management is necessary for reliable and efficient circuit operation. 3-D finite element analysis was used to study the feasibility of the use of graphene in thermal management of 3-D integrated circuits. The simulation results showed that the incorporation of graphene heat spreaders lower the maximum temperature of the chip. We calculated the equivalent thermal resistance for different design schemes and found that larger thermal resistance cause higher temperature rise within the chip. The maximum temperature rise of the chip was studied as a function of dissipated power across the channels and interconnects and thermal conductivity of few-layer graphene. The simulation results are important for the thermal management of three-dimensional integrated circuits and next generation electronics.

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1. Introduction

The concept of 3-D integrated circuit (IC) has gained much attention because of its improved features like increased device density (smaller footprints), reduced cost, heterogeneous integration, less power consumption, and more importantly shorter interconnect length and hence a wider bandwidth than its 2D counterpart [1]. The continuous downsizing in 2-D technology and the consequent increase in integration densities have resulted in longer interconnected structures that consume more power and the corresponding delay budget is also very high especially for below 130 nm technology [2,3]. The compact

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3-D integration (stack of multiple layers into monolithic structure) plays its important role here; it increases the number of ‘nearest neighbors’ seen by each transistor, yet the interconnect length remains shorter and hence it results in less RC delay. The shorter interconnect in 3-D structure has a direct consequence on the reduction of the switching energy and switching time, reduction of the cycle time and energy dissipation and a subsequent enhancement of IC performance [4].

Despite the above expected advantages, 3-D technology also faces some challenges. One of the major challenges of this technology is the thermal problem. Thermal issue is very important because high temperature in the chip physically degrades the performance, reliability and increases aging sharply [5-7]. Due to low thermal conductivity of ILD layers, the heat generated by the active devices and interconnects cannot be dissipated effectively, thereby produces localized heat i.e. hot spots [8]. High packing density of 3-D IC causes high power density [9]. And also increased layers of 3-D chip increase the thermal resistance by a significant amount. These result in higher temperature rise making thermal management a big challenge for the designers [1,10-11]. One of the possible solutions to mitigate this thermal problem is to incorporate material with high thermal conductivity into the chip design. Therefore, we propose the use of graphene for the heat management of 3-D integration.

Graphene is the 2-D allotrope of carbon with very high thermal conductivity and very high electron mobility. The thermal conductivity of graphene is in the range of 3080 Wm⁻¹K⁻¹ to 5000 Wm⁻¹K⁻¹ at room temperature [12-14]. The unique features of graphene have made it an excellent choice for electrical and thermal management applications [15-18]. The effectiveness of the use of graphene as heat spreader has already been studied using two dimensional model [19-20]. In this work, we carry out three dimensional thermal modeling in order to study the effect of graphene heat spreaders in thermal management of 3-D chip.

Fig. 1. Schematic of the 3-D chip with Graphene lateral heat spreaders (a) 3D view and (b) cross sectional view. Graphene heat spreaders are attached to side heat sinks and embedded underneath the device and interconnect layers.
2. Thermal Modeling of a 3D Chip

The designing of an actual 3-D integrated circuit faces many challenges from both the technological and designing viewpoints. With a view of thermal study, we develop a three dimensional model of 3-D chip, composed of two strata face-to-face stacking as shown in Fig. 1. The two strata are bounded through a wafer-to-wafer Silicon-di-Oxide (SiO₂) bonding layer. The first stratum is bulk and the second one is thinned silicon-on-insulator (SOI). The lower stratum has silicon substrate and the dimension of the substrate is 50μm x 30μm x100μm. Each stratum has its own device layer and metal interconnects. Each device layer has 2x2 MOSFETs and we approximate MOSFETs as rectangular channels. The length, thickness and width of each channel are 40 nm, 30 nm and 1μm, respectively. The separation between two channels is 10 μm. We model several copper interconnect layers, arranged in a array, with a thickness of 236 nm. The thickness of oxide layer between the interconnects is 2.9 μm. The two strata are connected internally with copper “super via” which has a thickness of 236 nm. The thickness of the SiO₂ bonding layer is 10 μm. Device and interconnect layers generate heat due to Joule heating and cause localized heat generation. Graphene heat spreaders with two-side heat sinks are placed underneath the interconnect layers and the device layers. The thermal conductivity of silicon substrate, bonding and oxide layer and copper interconnects are considered to be 155 Wm⁻¹K⁻¹, 1.38 Wm⁻¹K⁻¹ and 400 Wm⁻¹K⁻¹, respectively. A conventional heat sink is attached at the bottom of the first stratum.

We conducted the three dimensional thermal modeling with the help of finite element analysis using the software COMSOL. We have only considered diffusive heat transport because the size of the graphene layer is larger than phonon mean free path [12,15]. We model the heat conduction by solving Fourier’s law

\[-\nabla \cdot (k\nabla T) = Q,\]  

(1)

where \(Q\) is the heat source which is defined as the heat generated per unit volume per unit time (Wm⁻³) and \(\nabla = \frac{\partial}{\partial x} + \frac{\partial}{\partial y} + \frac{\partial}{\partial z}\).

The external boundaries were considered to be adiabatic and given by \(n \cdot (k\nabla T) = 0\), i.e. the temperature gradient across the boundary is zero. All the heat sinks were considered to be held at constant room temperature and were described as \(T = T_0\), where \(T_0 = 300K\).

Fig. 2. Maximum temperature rise as a function of dissipated power across the channels and interconnects in 2-D and 3-D ICs.
3. Simulation Results

Thermal issue is more critical in 3-D integrated circuit than that in 2-D integration. We get a clear picture of this phenomena from the simulation result shown in Fig. 2. The maximum temperature in 3-D chip is higher compared to that in 2-D for the same power density in the channels and interconnects. We vary the total power generation in both channels and interconnects between 2mW ~ 24mW. As a result, the corresponding maximum temperatures in 2-D and 3-D integration vary between 302K ~ 327K and 318K ~496K, respectively. The high power density, compact size and high thermal resistance result in the high temperature rise in 3-D chip. Both the designs have same circuit parameters.

Fig. 3. Temperature distribution in simulated 3-D IC (a) without and (b) with graphene heat spreaders attached to the side heat sinks. The thermal conductivity of single layer graphene is assumed to be 5000 Wm$^{-1}$K$^{-1}$. The total power within the chip is 16.2 mW.

Fig. 4 Maximum temperature in the chip as a function of dissipated power (a) across the channel only and (b) across the interconnect only.
From the above result, we are encouraged to find a solution to lower the maximum temperature in 3-D IC. Since graphene has very high RT thermal conductivity, we have incorporated graphene layers as heat spreaders underneath the device layer and interconnect layer. Fig. 3 shows the calculated temperature profiles for the 3-D integration without (Fig. 3(a)) and with (Fig. 3(b)) graphene heat spreaders placed underneath the device layers and interconnect layers. The thermal conductivity of single layer graphene is assumed to be 5000 Wm\(^{-1}\)K\(^{-1}\) and the value is independent of temperature. Two side heat sinks are attached to graphene heat spreader to support heat escape. We consider a power of 1.2 mW in channel and total 15 mW in interconnect layer. The maximum temperature in the hot spots is decreased by 68 K with the incorporation of graphene heat spreaders. The effect of graphene heat spreaders is more pronounced in the chip with more active devices and interconnects.

The growth and fabrication of Few Layer Graphene (FLG) is technologically feasible than Single Layer Graphene (SLG). It is known that the thermal conductivity of graphene is a strong function of lateral dimension\[15,16\]. Again cross plane coupling with changes in the phonon Umplakk scattering causes thermal conductivity of FLG to decrease and the value varies between 2800 Wm\(^{-1}\)K\(^{-1}\) ~ 1300 Wm\(^{-1}\)K\(^{-1}\) when atomic layer varies between 2 to 4 \[16,21\] and approaches to that of bulk graphite. We have explored the relation between maximum temperature and the variation of different thermal conductivity of FLG and simulated results are plotted in fig. 6. This figure illustrates that when both the atomic layer and thermal conductivity are larger, the maximum temperature is lower.

4. Conclusions

Our developed model and simulation results showed the role of graphene in thermal management of 3-D chip. The maximum temperature within the chip is reduced with graphene lateral heat spreaders placed underneath the device and interconnect layers. We carried out simulation for a wide range of thermal conductivities of graphene and few layer graphene.
result showed that even with lower thermal conductivity, a substantial amount of maximum temperature is reduced within the chip with FLG. This will help us to use few layer graphene as heat spreaders which might be more technologically feasible. Our developed model and simulation results are important for the heat management of the growing industry of nanoelectronics.

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All four authors have equal contribution to this paper.

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