Wet-chemical treatment for improved surface passivation of textured silicon heterojunction solar cells

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Abstract

Silicon heterojunction (SHJ) solar cells constantly gain more attention due to their low cost and relatively high efficiency. An important aspect of these solar cells is the incorporation of intrinsic hydrogenated amorphous silicon (a-Si:H) layers at each side of the c-Si wafer, which has increased the efficiency potential due to the excellent surface passivation. By applying a randomly textured instead of a double-side polished wafer, optical enhancement is achieved resulting in significant reflection reduction and high short-circuit current densities ($J_{sc}$). However, texturing-induced defects lead to an a-Si:H/c-Si interface with increased recombination, which limits the open circuit voltage ($V_{oc}$) of the SHJ device after using the same cleaning treatment as for the flat wafer. Thus, a one-to-one transfer of process parameters from flat to textured c-Si substrate is not necessarily appropriate and a different wet-chemical treatment is needed. In this work, a chemical treatment is demonstrated, which leads to an improved surface passivation.

Keywords: Silicon heterojunction; passivation; nitric acid; cleaning; wafer texturing

1. Introduction

Silicon heterojunction (SHJ) solar cell technology is very promising for the future compared to other PV technologies, due to the high conversion efficiencies achieved and the low processing thermal budget [1]. For both

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conventional SHJ solar cells and interdigitated back contact (IBC) solar cells the use of textured wafer substrates is a requirement in order to enhance light trapping and achieve high short-circuit current densities \(J_{sc}\) after device fabrication. Recently, the HIT cell reached an efficiency of 24.7% for which a 98 μm textured wafer substrate has been used [2]. At the same time the use of textured substrates can lead to devices with poor interface quality of the amorphous/crystalline silicon (a-Si:H/c-Si) junction. The high surface defect densities at this interface can significantly increase the recombination losses and therefore limit the open-circuit voltage, \(V_{oc}\). In order to reduce the interface defect density an efficient pre-deposition treatment is required to remove any possible contamination and nano-roughness from the c-Si substrate [3, 4, 5]. The term nano-roughness refers to structural irregularities on the c-Si surface induced from texturing. It has been shown that any possible contamination can be completely removed after applying a wet-chemical oxidation step and a subsequent dip in hydrofluoric acid (HF) [6]. In this case the surface defect density will strongly depend on the nano-roughness of the surface [6, 7]. Therefore, a non-aggressive pre-treatment that can remove any possible contamination and minimize surface roughness becomes necessary.

In this work, widely used wet-chemical cleaning procedures have been applied on textured c-Si substrates. In addition, an approach of subsequent oxidation and removal steps of the oxide has been tested. The oxidation has been realized by immersion of the c-Si substrate in nitric acid (HNO\(_3\)) solutions. In this way an approach similar to the nitric acid oxidation of silicon (NAOS) method [8] has been used, followed by stripping of the silicon oxide layer using an HF solution. In this work we will refer to this treatment as nitric acid oxidation cycle (NAOC). Repeating NAOC, i.e. oxidation and stripping of the oxide, is expected to help remove any surface structural irregularities in a controlled way. After the treatment the samples were subsequently passivated with approximately 40-nm thick intrinsic hydrogenated amorphous silicon (i a-Si:H) and the effectiveness of the pre-treatment in removing textured-induced defects has been evaluated using lifetime measurements. The NAOC treatment has been also applied in a device structure. Finally, SHJ solar cells were fabricated.

2. Experimental details

For the investigation of the pre-deposition cleaning procedures n-type FZ c-Si <100> wafers, with resistivity 1-5 Ωcm and thickness of 280±20 μm, were textured in an etching mixture consisting of high purity deionized water (DIW) and commercial solutions of 25% tetramethyl ammonium hydroxide (TMAH) and 99.9% IPA. The RCA, Piranha, and Nitric Acid Oxidation Cycle (NAOC) cleaning treatments, as well as combinations of those, were applied to the samples. RCA consists of two standard cleaning (SC) steps, SC-1 and SC-2. SC-1 and SC-2 steps were performed with a 1:1:5 solution of NH\(_4\)OH (ammonium hydroxide), H\(_2\)O\(_2\) (hydrogen peroxide), DIW (deionized water), and a 1:1:6 solution of HCl (hydrochloric acid), H\(_2\)O\(_2\), DIW, respectively at 80°C for 10 min each. As an intermediate step between SC-1 and SC-2, wafers were dipped in 0.5% HF at room temperature (RT) in order to remove the oxide layer grown previously in SC-1. SC-1 and SC-2 were prepared by mixing commercial solutions of 35% NH\(_4\)OH, 30% H\(_2\)O\(_2\) and 37% HCl. Piranha treatment was realized in a 1:3 solution of concentrated H\(_2\)SO\(_4\) (sulfuric acid) and 30% H\(_2\)O\(_2\) at approximately 120 °C for 20 min. Finally, NAOC consists of a 10-min step in concentrated HNO\(_3\) at RT, a second 10-min step in 69% HNO\(_3\) at 110 °C and stripping of silicon oxide layer in HF. Using spectroscopic ellipsometry, on a <111> polished substrate, the silicon oxide layer due to the immersion in HNO\(_3\) was found to be 1-2 nm. Every treatment step was followed by rinsing the textured substrate in DIW. Last step of every process before a-Si:H deposition was the H-termination of the Si surface in 0.55% HF at RT. After every treatment i a-Si:H layers were grown in a RF-PECVD reactor on both sides of the wafer to a thickness of approximately 40 nm. The reason for using thicker layers than commonly used in devices is that ultrathin i a-Si:H layers with a thickness of < 10 nm unprotected by the doped (n and p) layers are quite unstable when exposed to air and are considered unsuitable for investigating the effect of the cleaning procedure. The effect of the cleaning treatments was investigated by measuring the effective lifetime of the stacks using a Sinton Consulting WTC-120 lifetime tester in transient mode [9]. During the second stage of the experimental work solar cells were fabricated, for which approximately 5-nm thick i a-Si:H layers were used.
3. Results and discussion

3.1. Evaluation of the pre-treatments in double side passivated layers

In Fig. 1 the results for the various treatments used are summarized. It can be seen that the lowest lifetime is obtained when the piranha solution is used. Although sulfur contamination cannot be excluded, this can be attributed to some nano-roughness caused by the decomposition of H₂O₂ [10]. For this reason, we see that when the NAOC cleaning is applied after the piranha treatment, the lifetime increases. In a similar way, although the RCA results in a higher lifetime, an improvement is observed when it is followed by the NAOC treatment. The high contamination removal efficiency of RCA is mainly associated with the continuous oxidation and oxide removal by H₂O₂ and NH₄OH agents respectively in SC-1. Therefore, also in this case a limitation of the lifetime can be associated with nano-roughness from H₂O₂ decomposition. In the case of NAOC treatment one cycle seems to be able to yield similar lifetime with the RCA, while repeating the experiment for two and three cycles shows the best lifetime. This is comparable to the lifetime obtained on flat double side polished substrate, which in this case, serves as a reference. For the polished substrate only a slight decrease is observed when two cycles are used.

![Fig. 1. Effective lifetime of passivated i a-Si:H/c-Si/i a-Si:H stacks for different cleaning treatments, at injection level 1×10¹⁵ cm⁻³. Green markers are used for polished c-Si substrates, while blue and red markers are used for textured substrates. NAOC treatment is indicated with 'x' (number of repeated cycles).](image-url)

The fact that all treatments should be able to remove any possible contamination indicates that the differences observed are due to the change in nano-roughness on the facets of the pyramidal surface of the wafer. Interestingly, more than three cycles resulted in a decrease of the lifetime. It was expected after reaching an optimum, every step of oxidation and removal of the oxide would result in similar roughness and therefore similar lifetimes. A second series of samples in which the NAOC treatment has been applied can be seen in Fig. 1 (red) and is compared with the polished samples. Also, in this case an improvement is observed when repeating the NAOC treatment cycles, reaching an optimum at three cycles and slightly decreasing for more cycles.

After the cleaning procedure and the a-Si:H deposition all samples were annealed at 170 °C for 1 h in ambient air. It has been shown that post-deposition low temperature annealing can reveal information regarding the quality of the interface [11]. Annealing is expected to improve passivation by film relaxation when the transition from c-Si substrate to the a-Si:H layer is abrupt. In case an epitaxial layer is grown, annealing can even be detrimental for the passivation [11].
Fig. 2. Relative change in lifetime of passivated i a-Si:H/c-Si/i a-Si:H stacks for NAOC cleaning treatments, at injection level 1×10^{15} cm^{-3}. Green markers are used for polished c-Si substrates, while blue and red markers are used for textured samples shown in Fig. 1. NAOC treatment is indicated with ‘x’ (number of repeated cycles).

In Fig. 2 the relative change in lifetime of all the samples can be seen. Interestingly, only samples cleaned by the NAOC treatment exhibit a significant increase in lifetime compared to the other treatments, similarly to the flat samples. We argue that this is related to the efficient removal of the nano-roughness through the subsequent steps of oxidation and oxide removal. Initial roughness on the surface of the c-Si substrate might effectively result in similar interface properties as in the case of an epitaxial grown layer. However, this is expected to be strongly dependent on the initial morphology of the substrate after the texturing, as well as the deposition conditions for the a-Si:H layers. In case of the two NAOC cycles for the first series we observed no change during annealing, however the effective lifetime, measured after deposition, was already comparable with the ones obtained for the polished substrates.

### 3.2. Evaluation of the pre-treatments in device structure

The cleaning treatment that yielded the best results, i.e. NAOC, was also applied to make devices with the following structure: p a-Si:H/i a-Si:H/c-Si/i a-Si:H/n a-Si:H. Also in this case we found an optimum lifetime when 3 NAOC cycles are used, as can be seen in Fig. 3(a). Note that the lifetime measured is very similar to the lifetime obtained for a solar cell on a flat substrate. However, in this case much shorter lifetimes are measured, limited by the presence of the p-doped layer and the thickness of the a-Si:H. The effect of the layer thickness in device structure is demonstrated in Fig. 3(b). In Fig. 3(b) the values are estimated based on the expected thickness of the layer on a polished substrate and by using a factor of 1.73 to account for the pyramidal surface [12]. We think that the extremely low values of the effective lifetime for layers thinner than 4 nm are related with the insufficient coverage of the substrate. This can be enhanced by any roughness on the facet of the pyramidal structures that will shade the substrate during the deposition and result in non-conformal passivation layers.
3.3. Performance of SHJ devices

Finally, SHJ solar cell devices (area 4 cm\(^2\)) were fabricated independently on a flat and polished substrate. The structure of the devices can be seen in Fig. 4(a), while the performance is summarized in Fig. 4(b).

For the SHJ solar cells the intrinsic layer at the back has been omitted as we observed that the lifetime is mainly limited by the front interface and at the same time we observe an improvement in the FF [13]. For the polished and textured devices we used one and three NAOC, respectively, as these treatments proved to result in the best passivation for each case. Although, the device on a polished substrate has slightly higher \(V_{oc}\) and FF the textured device has much higher current density due to the effective light trapping resulting in an active-area efficiency of 20.8%.

4. Conclusion

We have investigated the effectiveness of commonly used cleaning procedures for the conditioning of textured c-Si substrates and we have applied an approach of wet-chemical oxidation using HNO\(_3\) and subsequent removal. The cleaning procedure after the texturing is an important step to achieve high efficiency SHJ solar cells. However, the
cleaning can also introduce roughness depending on the chemical solution used. For our textured samples, repeated cycles of nitric acid oxidation procedure are able to improve the passivation quality significantly. We expect that this improvement is directly related to the efficient removal of contamination and nano-scaled roughness, induced from the texturing, on the facets of the pyramidal structures.

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References