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Single crystal diamond wafers for high power electronics

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ABSTRACT

According to international energy proposal, about 25% of the total CO2 reduction should come from "end use efficiency". Hence, low loss power devices are an important technology for the 21st century. Diamond-based devices have the potential, but this would require fast development in order to contribute to the CO2 reduction plan early in this century. Here, we present a clear target for the R&D of diamond wafer. According to the expected applications of diamond devices with a vertical structure, the required target properties for first stage diamond wafers are; a killer defect density less than 0.1 cm^{-2}, resistivity less than 0.005 Ω cm and a size of 4 in. For the final commercialization stage, targets of zero killer defects, resistivity of 0.001 Ω cm and a size of 6 in. are proposed. The challenges and proposal solutions are reviewed for each technology.

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1. Introduction

The threat of global warming is becoming more and more critical; recently CO2 concentrations observed in Hawaii exceeded 400 ppm [1]. In the recent "Conference of Parties (COP)" 21 climate meeting, the participating countries submitted and adopted "Intended Nationally Determined Contribution (INDC)" [2] targets for CO2 reduction, for example, 40% in 2030 (vs. 1990) for EC, 26–28% in 2025 (vs. 2005) for US, and 26% in 2030 (vs. 2013) for Japan. According to the latest report by the International Energy Agency (IEA), "World Energy Outlook", the world temperature is likely to rise 5.3 °C by the end of the 21st century if new CO2 reduction policies are not implemented. To follow the "delayed" 450 ppm CO2 scenario, several technical policies are expected and the largest contribution is obligatory "end use efficiency" target that is intended to be responsible for 49% of the total worldwide emission reduction by 2030 [3]. This is three times larger than the "Renewable energy" target of 17%. Undoubtedly, the low loss power electronics will play a major role in improving "end use efficiency".

In 2013, Mitsubishi Electric delivered a practical railcar power supply system that incorporated the world's first silicon carbide (SiC) power modules using Schottky barrier diode (SBD). Very fast and low power loss device allows the system to achieve many advantages of 30% less power loss, with the additional advantages of 20% smaller and 15% lighter power module. The Mitsubishi system also reduces transformer noise by 4 dB due to a 35% improvement in the distortion rate of output voltage waveforms [4]. In December 2015, the full SiC power modules consisting of SBD and metal oxide semiconductor field effect transistors (MOSFET) were introduced into "Yamanote line" railway; saving 17% power losses during powered operation [5]. The full SiC modules are currently under testing for use in Shinkansen in the near future [6]. For automotive applications, Toyota has announced their plan to introduce full SiC modules in 2020 in hybrid electric vehicle (HEV) systems [7]. Since the beginning of R&D of SiC devices, the achievement of low loss was expected however, many additional advantages were observed, such as power regeneration during high speed running and very light weight modules. These characteristics come from the high frequency operation of SiC due to very small "charge transfer" of unipolar device, and the small sizes of the reactive L and capacitor C.

Diamond is also a hopeful candidate material for next generation power devices due to its favorable properties such as a high breakdown field, high thermal conductivity, high mobility and low dielectric constant [8,9]. There are several big material challenges to overcome for the practical application of diamond devices. In particular, the fabrication of a single crystal wafer with large size, dislocation free, and low resistivity. In addition, there are some drawbacks such as deep acceptor (B: 0.37 eV) and donor (P: 0.57 eV) level with imperfect doping for donor. However, at elevated temperatures such as from 200 to 250 °C; that is the self-heating temperature of the power devices, increased numbers of activated carriers with high mobility such as 240 cm^2/Vs at 250 °C contribute to a reduction in conduction losses [10]. This is based on a new concept of unipolar power devices that do not require "cooling systems". The present status of the R&D on diamond materials for power devices is somewhat disjointed; it is considered beneficial to discuss definite target with diamond devices in order to accelerate research and contribute to the global CO2 reduction plan. In this paper, we review the current status of

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diamond wafer R&D and propose targets with respect to the existing challenges for fabricating large size wafers with low dislocation density and low resistivity [11].

2. Applications of diamond power devices and specifications of diamond wafer

The wafer specifications for power device applications differ depending on the application. In this section, the expected applications for the diamond devices are reviewed before discussing the detailed specifications. Possible applications are summarized with respect to current–voltage map, as shown in Fig.1. As described in the introduction, the recent replacement of Si by SiC devices suggests a future transition to diamond devices.

Firstly, we predict applications for diamond devices in the high voltage field, such as high power generators and inverters for trains, ships, renewable energy systems, and power trunk line systems. The realization of SiC unipolar devices using both SBD and MOSFET for high voltage applications enabled low loss devices compared to previous Si bipolar devices. This is due to the accumulation and recombination of minority carriers in the bipolar device, whereas the charge transfer in unipolar devices only depends on the depletion and transferred charges. In the higher voltage region, wide bandgap bipolar devices suffer high forward loss of Von × Ion, due to high "on voltage" such as over 4 V for SiC. Hence, diamond unipolar devices with low losses might find applications in the high voltage field.

Another important factor that allows SiC devices to realize low losses is the fast switching or high frequency operation, typically several microseconds [12]. This fast switching enables electric power regeneration during the high speed running mode of trains that avoids using the mechanical break system. Low loss unipolar diamond power devices may have faster switching compared to SiC devices; this has been partly verified by SBD [13]. Additionally, fast switching also implies smaller power module with small size capacitor C and reactor L of high frequency operation. A total volume reduction for SiC module of 55% can be attained compared to Si IGBT and pn diode modules [12].

For extremely high voltage applications over 10 kV device, wide bandgap bipolar devices are expected to open up new opportunity in the future [14], diamond bipolar devices are a hopeful candidate owing to their favorable characteristics. Diamond that uses deep energy level carriers has increased numbers of carriers at high temperature. The tradeoff in carrier increases with the mobility decrease brought by "carrier scattering", resulting in a constant current between 150 and 250 °C [15]. This characteristic has inspired new type of high output power device module operating at self-heating temperatures; which are thermally insulated without cooling. In addition, there exist numerous applications in lower voltage range including ultra and super high frequency fields. Here, AlGaN/GaN HEMT devices are already used for many applications incorporating high mobility two dimensional electron gas (2DEG) channel.

Some applications and their corresponding device structures are shown in Fig.2. For the low power devices including high frequency applications, the lateral structure is adopted for the devices such as field effect transistors (FET). AlGaN/GaN HEMT power devices are commercialized for high frequency application using insulating substrates. Dislocations are not critical for this application, because of the lateral current flow. On the other hand, the vertical structure is adopted for high power applications to meet the requirements for high current densities. In the vertical structure, current flows from the substrate surface to the electrode at the back surface, thus the majority of the substrate acts as a resistive power loss layer and simultaneously a thermally resistive layer. In order to fabricate low loss devices for high power devices, a low resistivity substrate is essential, often requiring a final back-lap process to thin the substrate.

The parasitic resistivity of devices as a function of substrate resistivity and thickness are shown in Fig.3. The dotted lines show data for substrate thicknesses of 300 μm, 100 μm, 50 μm and 10 μm after the back lap process. A thickness of 50 μm is technically possible for the R&D purposes; however, 100 μm is considered as the limit for mass production. 10 A and 100 A lines only show conventional standard image of resistivity. A final target for substrate resistivity could be 0.001 Ω cm, corresponding to the devices over 100 A with a substrate thickness of 300 μm. A first target could be 0.005 Ω cm corresponding to 100 A device with a substrate thinned down to 100 μm; this resistivity is comparable to that of present SiC wafers. Doping with B to achieve a resistivity of 0.01 Ω cm is already possible using conventional MPCVD for thin films, and thicker films grown up to 50 μm can correspond to 100 A class devices.

Another critical property of the substrate for power devices is the dislocation density, as the current flows from the substrate surface to the back electrode in the case of a vertical structure device. The dislocation density of current 4H SiC wafers [16] compared to the expected final target is shown in Table 1. Micro pipes (MP), threading screw dislocations (TSD) and basal plane dislocations (BPD) are the critical dislocations to device performance, where these dislocation densities are <1, 300–600 and 1–10 for the typical commercially available wafers, respectively. In particular, MPs are the famous killer defects in SiC, the existence of which is inevitable for all types of devices. The numbers of

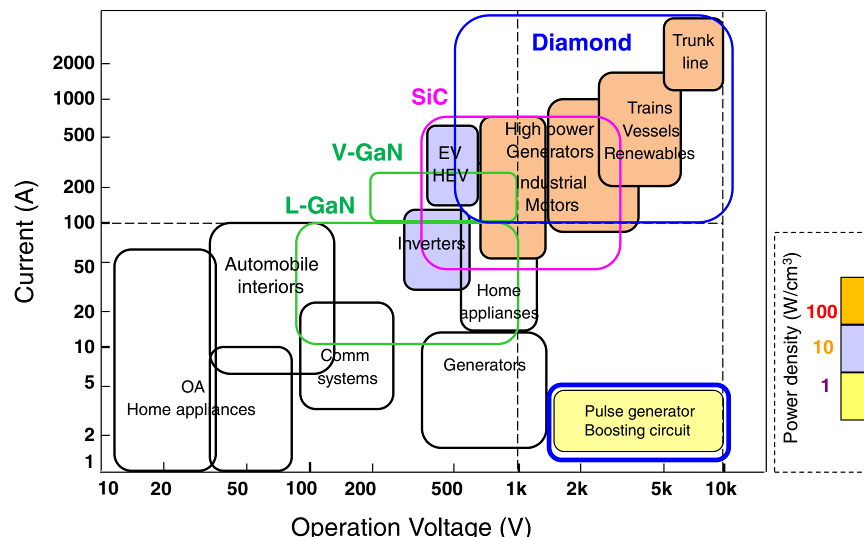

Fig. 1. Application possibilities in current- voltage map.

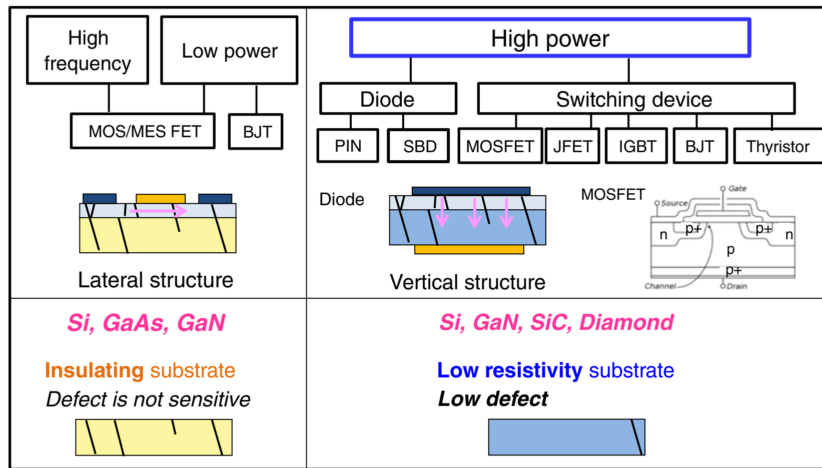

Fig. 2. Device applications and corresponding device structures and wafer.

malfunction device is influenced by the numbers of killer defects as well as the device active area. It is given by the following Murphy plot for killer defects and it is extremely effective when the chip size is large, that is, a high current for the power device, as shown in Fig.4.

$$Y = \exp(-AD) \quad (1)$$

Here, Y is the yield of device, A is the area of the device and D is the defect density. As can be seen from the figure, the devices yield decreases significantly, even at the lowest defect densities. For the first target, a defect density of 0.1 cm^{-2} is assumed, that is a 90% yield for a 10 mm × 10 mm size chip, corresponding to > 100 A device. The final target is of course, zero killer defects. The final target dislocations densities have been concluded as a result of private communications with many researchers in the SiC field; zero dislocations are expected for MP and BPD with small numbers remaining for TSD. Considering the aforementioned circumstances in SiC that is capable of supplying the first stage devices in the market suffering present wafer defects, it is reasonable to set the first target for dislocation numbers in diamond to the present value for SiC, that is, <500 cm^{-2}. In addition, the final target for diamond might follow that of SiC, <10 cm^{-2}. In the early stages of R&D, testing of 10 A devices is important for the verification of the properties of diamond devices, thus dislocation densities <5000 cm^{-2} might be a suitable criterion in this case. To summarize, the expected specifications of diamond wafers, such as resistivity, dislocation density, and wafer size are shown in Table 2. Here, R&D target implies the wafer target to support R&D for a 10 A class power device that is suitable for evaluating the properties of the diamond devices. The first target is set considering the expected characteristics of wafers for small scale mass production of devices comparable to present SiC wafer fabrication. The final target is based on a full mass production case.

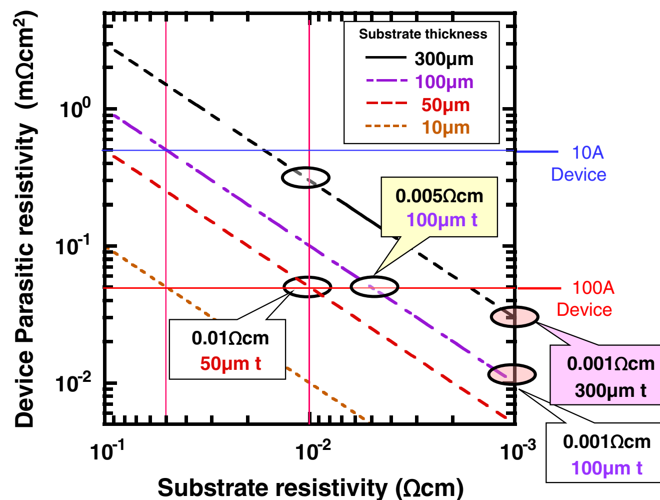

Fig. 3. Device parasitic resistivity dependence of substrate resistivity with varieties of final substrate thickness.

3. Large size wafers

Recent development of diamond wafers has been summarized in a special issue of MRS journal [17]. Hetero-epitaxial growth techniques using large hetero-substrates such as MgO [18], $SrTiO_3$ [19], Al2O3 [20] and YSZ/Si [21] are hopeful for its original substrate size. A drawback of hetero-epitaxial growth is the high dislocation density, far beyond that of single crystals, that originates from the coalescence of crystal plates. Several trials are now underway trying to resolve this problem. Using a sophisticated growth technique on Ir/YSZ/Si for thick films up to 1 mm, the dislocation density reduced three orders of magnitude, from $10^{10}cm^{-2}$ to $10^{7}cm^{-2}$ [18], where an order of magnitude increase in thickness corresponded to an order of magnitude reduction in the dislocation density. Another method likely to reduce dislocation density is the epitaxial lateral overgrowth (ELO) of diamond on Ir(001) / MgO(001) substrates, as it was demonstrated using the patterned nucleation and growth method [22]. The reduction of dislocation density down to the order of 10^3 cm^{-2} is expected for hetero-epitaxial growth technique in the future.

Another promising technology to realize large wafer production is the mosaic wafer fabrication method [23–25]. The size of present mosaic wafers fabricated by AIST is from 2 × 2 cm^2 to 4 × 6 cm^2, where the largest one is a little larger in area than a 2 in. f wafer. Mosaic wafers are consist of several plates of approximately 1 cm^2 single crystal diamond fabricated by a copying technique using ion implantation and lift-off [26]. Power device fabrication is avoided on the crystal boundary of the joined region; therefore, unusable area of a mosaic wafer may be very high when the

Table 1
Dislocation density image of present 4H SiC wafer and expected final target.

	Typical comm. available wafer (cm^{-2})	Final target (cm^{-2})
Micropipe	0–0.02	0
Threading screw	300–600	<10
Basal plane	1–10	0
MP + TS + BP	301–610	<10
Threading edge	3 k–6 k	

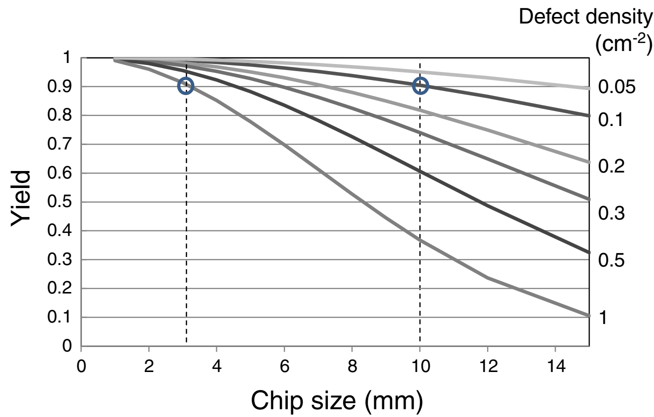

Fig. 4. Killer defect density dependence of the device yield. (Assuming the square chip).

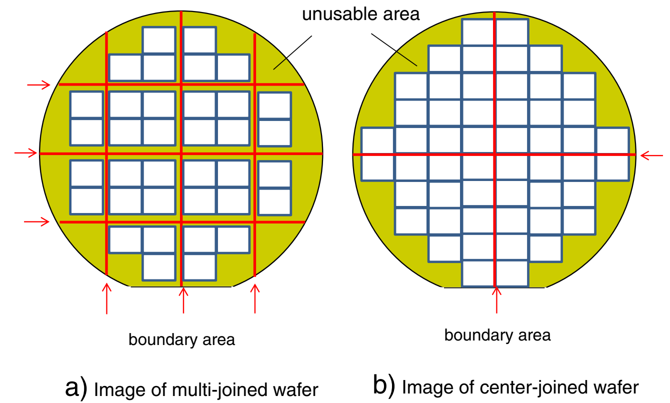

Fig. 5. Diamond wafer images using mosaic technique.

device size differs from the plate size. In the worst case, up to 40% of the wafer area will not be used for the device. This is schematically shown in Fig.5a). Accordingly, such a "multi-joined wafer" cannot be used for mass production. However, the center-joined wafer shown in Fig.5b) can be used as conventional wafer, because the joint boundary area exists on the dicing lines of the center chips. In this case, the size of the plate is half the wafer size, e.g. a 1 in. plate for 2 in. wafer, and a 2 in. plate for 4 in. wafer. Thus the enlargement of single crystal plate size associated with the low dislocation density is very important for the mosaic wafer.

To realize large plates up to 1–3 in., the vertical growth of bulk crystal is an urgent challenge to be addressed. This is directly associated with the low dislocation density growth as it is in the case in Silicon Carbide; well known as the repeated A face (RAF) bulk crystal growth method [27]. The largest drawback for bulk growth of diamond is the non-equilibrium growth accompanied by very large temperature gradients of 900 °C within the diamond crystal, that is; 1000 °C on the growth front of bulk edge facing high temperature plasma ball of up to 2800 °C, and 100 °C on the other bulk edge which is adjacent to water cooled holder. This large temperature gradient introduces large strain in the bulk diamond. During the last ten to twenty years, several techniques have been investigated that might be applicable for diamond wafers, such as pulsed plasma processing and electron cyclotron resonance (ECR) plasma processing. Pulsed plasma processing can provide variations in the electron temperature, electron density, and gas temperature by changing the frequency and duty ratio of an input pulse [28–32], and high quality diamond was reported using this technique [29]. The pulsed operation method was also employed in ECR mode plasma processing, where a high growth rate was observed with low temperature deposition [33]. Currently, research activities using pulsed plasma are not common for the growth of large diamond wafers, because the input plasma power is not large enough to cover the low duty ratio conditions. For instance, 3 kW deposition with 10% duty ratio requires initial power of 30 kW for the generator, which is not yet achieved for 2.45 GHz. However, the recent development of devices including "all solid" generators using semiconductor high frequency amplifiers will find a possible method to meet the requirements of high power generators. Most of the plasma CVD systems used in diamond growth use 915 MHz and 2.45 GHz ISM (Industrial, Scientific and Medical) bands for microwave-based growth equipment. Several trials scaling up the plasma size demonstrated the possibility for large scale deposition [34]. However, additional bands were allocated for ISM band by ITU [35] for lower frequencies such as 862-875 MHz, 433.05–434.79 MHz and 312-315 MHz. These bands provide longer wavelengths that can respond to larger size plasma excitation, such as a wavelength of 69.1 cm for 433 MHz plasma. Of course, some of the non-plasma systems reviewed in the previous paper [36] are also good candidates and further research into these methods is highly required.

Table 2
Expected specification of single crystal diamond wafer for power device application.

	R&D target	First target	Final target
Wafer size	2 inϕ	4 inϕ	>6 inϕ
Resistivity	0.01 Ω cm	0.005 Ω cm	0.001 Ω cm
Dislocation density	<5000 cm^{-2}	<500 cm^{-2}	<10 cm^{-2}
Killer defect density	<1 cm^{-2}	<0.1 cm^{-2}	0 cm^{-2}

To realize large area single crystal diamond plates up to 1–3 in., both lateral growth and vertical growth are important. In Fig.6, two figures are shown, which are reproduced from papers on CVD bulk crystal growth by AIST [37] and Michigan State University [38]. In both cases, the bulk diamond growth rate in the lateral direction is similar to that in the vertical direction; such as 1.17 times the lateral growth during 1 mm vertical growth and 1.4 times the lateral gain during 2.5 mm of vertical growth. The limitation in the growth rate is due to the polycrystalline rims that grow in periphery of the single crystal region. Use of recessed holders [39,38] will be helpful to reduce this polycrystalline rim. For further improvements, reduction of gas turbulence and the concentration of plasma near the crystal edge, as well as optimization of the growth parameters are the new challenges [39–41].

4. Low dislocation density wafers

We can learn the history of SiC wafer development to find solutions for the challenges in the development of vertical structure high output power diamond devices. The commercialization of 1 in. SiC wafers occurred in 1991, and that of 2 in. in 1996, both by a US company CREE. It took 8 years further to commercialize Schottky barrier diode (SBD) of 3 to 6 A class devices for power factor correction (PFC) circuit applications in 2003 by the German company SICED. This period coincided well with the development of compound semiconductors such as GaAs and InP. 2 inch diameter GaAs devices began a small-scale mass production in 1981, and the AlGaAs/GaAs high electron mobility transistor (HEMT) was introduced in receivers for satellite broadcast systems in 1987. Also, 1.55 μm DFB lasers became popular for optical fiber communication systems in 1989 using 2 in. InP wafers that achieved small scale mass production in 1981 [43,44]. Both AlGaAs/GaAs HEMT and DFB lasers are small lateral type device sand they suffer in a very small way from the influence of wafer dislocations and defects. However, the first introduction of over 100 A class SBD high output power devices to train systems was in the Tokyo Metro in 2013 [4]. This was 17 years after the commercialization of 2 in. wafer. To emphasize this again, the R&D time to apply 3 A device and 100 A devices was 8 years and 17 years, respectively. This is mainly due to the R&D time required for the reduction of the dislocation densities. In the early age of SiC, it suffered from "micro-pipe" defect around 100 cm^{-2} in 1996, and it took 7 years to achieve a micro-pipe free wafer by "Repeated A Face (RAF)"

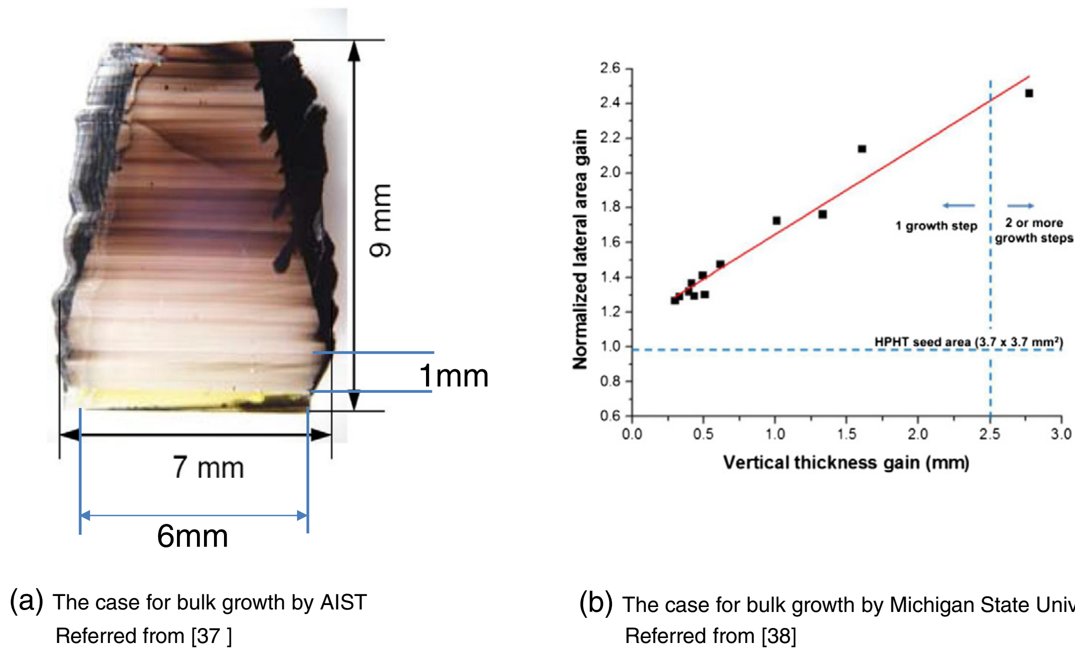

Fig. 6. Lateral growth of diamond.

method in 2003 [42]. After the reduction of micro-pipes, it took 10 years to realize 100 A class vertical devices by reducing dislocations and other defects that negatively influence the device characteristics. Of course, other dislocations and defects were also important issues in SiC wafer development during this period. TSD and BPD dislocations are very critical for MOSFET characteristics [45], TSD leads to lower breakdown voltages [46] and BPD influences the forward characteristics in bipolar devices [47,48]. Some residual BPDs can be converted to TEDs, by high temperature annealing of epitaxial layers [49]. In addition, it is known that some of the TSDs can be converted to Frank partial dislocations by sophisticated epitaxial growth technology [50]. Many TEDs exist in SiC wafers; however, this is not very critical to the device performance.

For diamond devices, research activities on dislocation reduction are currently in a very early stage. Since the methods of X ray topography were first applied to diamond in 1944 [51], other methods have been proposed [52–54] and some studies have been carried out for dislocation analysis. A study on CVD homo epitaxial layers on HPHT substrate showed that large numbers of dislocations originate from the interface [55], resulting from the immature CVD technique presently used for diamond growth, in particular the surface treatment prior to the growth. The analysis of Burger's vector of dislocations was carried out using X ray topography with synchrotron radiation (SR) for the HPHT substrates and CVD films, and “edge” and “mixed” type dislocations were identified [56–58]. By comparing the data with cathode-luminescence (CL) mapping results, the well-known “band A” emission showed good agreement with the “mixed” type dislocation in p- layer deposited on Ib HPHT crystal [57]. Dislocation densities of conventional HPHT substrates have been estimated to be from 10^3 cm^{-2} to 10^8 cm^{-2}, most likely from 10^4 cm^{-2} to 10^6 cm^{-2} [59], however it is difficult to quantify the exact numbers because of the existence of dislocation bundles. Defect observed by birefringence appeared as bundles of ten or more defects after etching by O2/H2 plasma [60]. Dry etching with various gases such as CO2/H2, is used to evaluate dislocation densities [61], however, there are no standard methods for evaluating the density. The lack of an effective wet etchant for diamond is making the evaluation and understanding of dislocations very difficult. It is important to establish a standard dry etching procedure in order to understand and promote the R&D for the reduction of dislocations. In addition, the studies on the relationship between the dislocation detected by topography and dry etched pits are very much required to understand the types of dislocations and their density.

There are several emerging methods for reducing dislocation densities. The first is to reduce dislocation densities of HPHT seed crystals, and using low density area as the seed crystal in second HPHT growth, IIa type crystal with very low dislocations has been developed with a dislocation density estimated to be as low as 47 cm^{-2} [62,63]. Using a low dislocation density crystal as the seed, copying by CVD using ion implantation and the lift-off method was undertaken [59]. Starting from a < 100 cm^{-2} mother crystal, the dislocation density of an obtained daughter wafer was 400 cm^{-2}. There was some increase in dislocation density; however, the value obtained was far below that of conventional CVD substrates. This increase in dislocation density is presumably due to the downfall of particle from the chamber as well as the surface scratch occurred during surface polishing and cleaning. In the early days of GaAs and SiC epitaxial growth, macro-defects induced by particles falling on the substrates were commonly observed. To eliminate downfalls, sophisticated deposition system well equipped with sophisticated gas flow, slow leak, and the “load-lock type” chamber is required. For the surface polishing and cleaning, techniques to reduce dislocations originating from the epitaxial layer and bulk interface are important. A recently developed fine polishing technique is nominated as one of the candidate techniques. This technique is assisted by UV light and has been shown to reduce the dislocation originating from the interface that certainly [62–66]. During this polishing process, CO and CO2 gases were detected, presumably generated from the ozone which are developed from O2 under UV exposure. Also, the plasma etching using RIE has been demonstrated to improve diamond quality and reduce dislocation density [67,68].Further techniques for surface finishing are required for the reduction of dislocation densities.

The leakage current analysis of SBD have been studied and compared with the dislocation types, however, we cannot make decisive conclusions at this stage [69,68]. Further research activities on the influence of dislocations to the device performance for both unipolar and bipolar devices are very important in order to distinguish the characteristics of the dislocations. It may change the research target of dislocation density in the future.

5. Low resistivity wafer

B doped single crystals grown by HPHT have been realized by several companies in Russia and other countries, with the largest size of 8 mm had been realized [70]. A study on the crystallinity of such crystals indicated that there are many stacking faults and dislocations [71]. The dislocation density investigated by X ray topography was high up to 5×10^4 cm^{-2}. The doping concentration of the commercially available substrate is not high, with a resistivity around 0.06 Ω cm. The initial B doped bulk grown by CVD from B doped HPHT seed crystal was very interesting due to the small difference in lattice constants that led to small residual strains in bulk crystal. Thus, the development of high quality B doped HPHT crystal is expected in the near future.

Growing thick bulk materials by CVD is an essential technique to obtain B doped substrates, regardless of the initial HPHT crystal. To achieve a low resistivity substrate for the power devices, there are two major technological challenges to overcome, the high doping concentration required and the subsequent soot formation during processing.

The first challenge is the high concentration doping required to obtain the final target resistivity of 0.001 Ω cm, with high crystallinity and low dislocations. High doping is usually accompanied by high strain, which needs to be reduced to produce quality devices. The highest B doping concentrations that have been achieved by microwave plasma CVD are 0.0015 Ω cm at 2.4×10^{21} cm^{-3} [72] and 0.003 Ω cm at 8×10^{20} cm^{-3} [73]. In the high B containing gas phase, B concentrations incorporated in the film tend to reduce with increasing B concentration, which limits reduction of the resistivity [74]. Recently, an experimental trial was carried out for high B doping using hot filament (HF) CVD and a low resistivity of 0.0012 Ω cm at 12,820 ppm in B/C gas ratio was observed [75]. The dependence of the resistivity on the dopant gas for HFCVD growth is linearity at higher concentrations, indicating possibility to realize 0.001 Ω cm. The resistivity dependence measured at RT of the B doped films produced using MPCVD and HFCVD is shown in Fig.7 with the linear relationship indicated by the trend line. High doping of B also induces lattice constant mismatch to the substrate, known as Vegard's law [76], especially in the case of using undoped diamond as the seed crystal. Thus, high quality and highly doped HPHT seed crystals are important to realize low resistivity diamond wafers.

The second challenge is the continuous growth of a thick bulk layer to overcome the technical drawback of soot formation from introducing a high concentration boron source in the chamber. Very thick CVD grown layers with high B doping have been carried out by the CNRS group using 40 W/cm^3 microwave plasma CVD and they succeeded in fabricating bulk diamond more than 300 μm in thickness [77–79]. The B doping concentration was 5000 ppm and the resistivity was expected to be several tens of m Ω cm. Long deposition times with high concentrations of B result in soot formation in the chamber, especially at the surface of the quartz window where the microwave is introduced [80, 81]. This phenomenon leads to an increase of microwave reflection at the quartz window that induces a malfunction of the growth system. In addition, time consuming cleaning of the chamber is required to remove the soot after deposition, which lowers the productivity of the machine. Instrumental improvements are required for microwave plasma CVD systems. The developments of other kinds of CVD methods including HFCVD are required for this purpose.

6. Conclusion

According to the IEA energy proposal, about 25% (49% in total 50% reduction is expected for end use efficiency) of CO2 reduction should come from "end use efficiency", and energy savings with the use of low loss power device modules could be an important technology for achieving this goal. Following the success of replacing Si by SiC devices for low loss, high frequency operation at high voltage, the fast development of diamond devices is required to produce improved modules with lower losses.

The expected applications for diamond devices are high voltage, high output power devices with the possibility of high temperature operation. The vertical device structure is inevitable for these applications, and corresponding diamond wafer is necessary. For the killer defects, we propose the defect density of 0.1 cm^{-2} for the first target that corresponds to 90% yield for 10 mm × 10 mm size 100 A device chips. The final target is of course, zero killer defects. For the less critical dislocations, the targets were set as to follow those presented for SiC. For vertical structure devices, there is a trade-off between substrate resistivity and thickness. To achieve a device over 100 A, a resistivity of 0.001 Ω cm with a 300 μm thick substrate is a reasonable target. A target of a 6 inch. wafer size is desirable using the center-joint for the case of mosaic type wafers.

The market size of power device modules is expected to be 30 trillion US dollars in 2020 and is also expected to increase every year. Diamond has the considerable advantage of consisting of carbon, hence it is free from natural resource depletion problems and are truly an important material of the 21st century.

Prime novelty

25% of the global CO2 reduction should come from "end use efficiency", and diamond-based power devices will play an important role early in this century. However, the research focused on diamond materials for

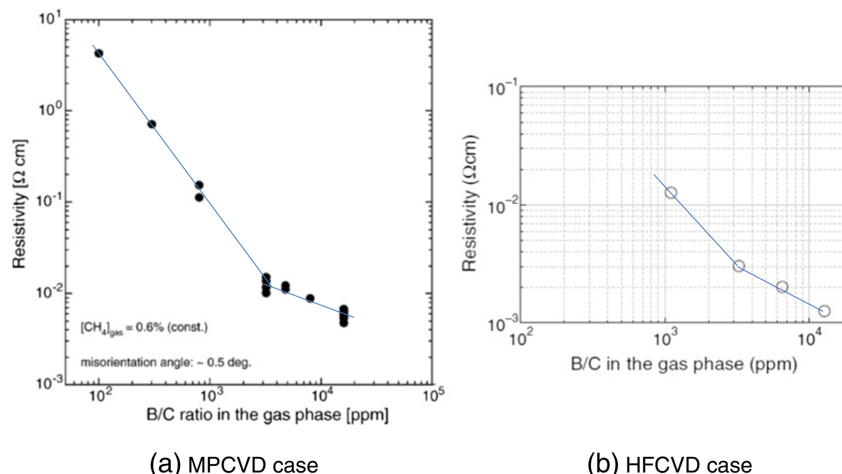

Fig. 7. High B doping for (001) by MPCVD and HFCVD method [75,76] Blue lines are given in this paper.

power devices is somewhat disjointed and it is considered beneficial to define clear target in order to accelerate research. In this paper, we reviewed the current status of diamond wafer R&D and proposed clear targets with respect to the existing challenges for fabricating large size wafers with low dislocation density and low resistivity.

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