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A Fourth-order Sigma-Delta Interface Circuit for Closed-loop Micromachined Accelerometer

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Abstract

A single-loop fourth-order sigma-delta ($\Sigma\Delta$) interface circuit for closed-loop micromachined accelerometer is presented in this work. Two additional electronic integrators are cascaded with the micromachined sensing element to form a fourth-order loop filter to eliminate quantization noise. A switched-capacitor (SC) charge integrator and correlated double sampling (CDS) are applied to reduce input-referred electronic noise. Matlab and Hspice simulation results indicate that signal-to-noise-and-distortion ratio (SNDR) is 86.5dB, effective number of bits (ENBO) is 14.08 bits when over sampling ratio (OSR) is 128, the sensitivity of the system is 0.65V/g, the full measurement range can be achieved from -5g to +5g.

Keywords: Sigma-Delta, Accelerometer, Closed-loop

1. Introduction

High precision accelerometers with microgravity (ug) resolution, high sensitivity, high linearity and low bias drift are needed in many applications, including inertial navigation and guidance, microgravity measurements in space, tilt control and platform stabilization, seismometry and GPS-aided navigators for the consumer market\[1\]. Sigma-delta ($\Sigma\Delta$) interface is attractive for micromachined accelerometer since it is simple, provides a digital output, has a large bandwidth, can be easily implemented in high density CMOS technologies and its one-bit feedback can solve the problem of nonlinear electrostatic forces\[2\]. The sensing element can be used as a loop filter to form a second-order micromachined $\Sigma\Delta$ modulator. However, due to very low dc gain at low frequencies of the mechanical integrator, and analysis of this system shows that the in-band quantization noise at the output always dominates over the electronic noise, regardless of the oversampling ratio\[3\]. Thus adopting higher order $\Sigma\Delta$ modulator to enhance the system performance is an effective approach. In this work, a fourth-order $\Sigma\Delta$ interface circuit for closed-loop micromachined accelerometer is presented.

2. System analysis and design

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A single loop structure is applied in this design, two additional electronic integrators are cascaded with the micromachined sensing element to form a fourth-order loop filter providing additional noise shaping. However, stability is a major problem in high order single loop \(\Sigma\Delta\) modulator\([4]\), in order to stabilize the system, a lead compensator which introduces some phase shift at higher frequency is inserted between the C-V converter and electronic integrators. The transfer function of lead compensator is given by
\[
H(z) = K(1 - \alpha z^{-1})
\]

\(\alpha\) reflects the compensation degree, with \(\alpha\) become larger, the system is more steady, but meanwhile, performance of the system will degrade. In this design, based on parameters of sensing element, \(\alpha\) is chosen to be 0.6 to obtain maximum SNDR. To ensure linearity, a one-bit quantizer is employed and a one-bit digital-to-analog converter (DAC) which provides the electrostatic force feedback on the proof mass is used in the feedback loop. The system model of the fourth-order \(\Sigma\Delta\) accelerometer is shown in figure\(1\). \(K_{dc}\) is the gain from proof mass displacement to change in capacitance, \(K_{cv}\) expresses the gain of C-V converter, and \(K_{fb}\) is the gain from feedback voltage to feedback electrostatic force.

There are three main noise sources affecting the overall resolution of the accelerometer system: Brownian noise originating from the constant movement of air molecules, electronic noise from the C-V converter and quantization noise from the analogue to digital conversion process\([5]\). The electronic noise has different components including the front-end amplifier noise, \(kT/C\) noise, modulation signal noise and clock jitter noise. Referring to figure 1, the transfer function of the system is given by
\[
V_{out} = \frac{K_{cv}H(z)KqG(z)(F + F_b)}{1 + K_{cv}H(z)KqG(z)K_{fb}} + \frac{K_{cv}H(z)KqN_q}{1 + K_{cv}H(z)KqG(z)K_{fb}} + \frac{N_q}{1 + K_{cv}H(z)KqG(z)K_{fb}}
\]

Where \(G(z)\) is the z domain expression of the sensing element, \(H(z)\) the transfer function of the lead compensator and 2order electronic integrator. It can be seen from equation (2) that the quantization noise is shaped by the sensing element and second-order electronic integrator considerably. And meanwhile, electronic noise is also shaped by the sensing element. Only the Brownian noise will not be shaped by the \(\Sigma\Delta\) modulator, and be directly exported to the output. In this design, the sensing element is fabricated in bulk silicon technology, its mechanical noise is smaller than 1ug/Hz\(^2\).

3. Circuit implementation

The interface circuit is composed of C-V converter, lead compensator, second-order electronic integrator, quantizer and one-bit DA converter. The schematic diagram of the \(\Sigma\Delta\) interface circuit is shown in figure\(2\). The switched-capacitor (SC) charge integration method is used for the C-V converter owing to the same foundation on which the SC circuit operates, and the sensed signal is insensitive to parasitic capacitance and undesirable charging. As indicated in reference 6, increasing integrator capacitance and sampling frequency can reduce front-end circuit
noise, but it also decreases the sensitivity of the charge integrator and decreases the signal-to-noise ratio even though it improves the absolute voltage noise. Therefore, the integration capacitance and the sampling frequency should be optimized. 5pF integration capacitance and 256KHz sampling frequency are applied to achieve desired resolution. A high performance operational amplifier is designed to ensure the speed and resolution of signal establishment, and avoid broadband noise folding induced by correlated double sampling (CDS). An additional switch that will open before every sensing phase is introduced to the C-V converter to discharge the accumulating charge at sensing point, which avoids badly offset of operational amplifier. In order to compensate finite gain of operational amplifiers, reduce 1/f noise and offsets of operational amplifiers, CDS technique is introduced. A high speed comparator and low power lead compensator are also designed in this work. The repetitive cycle of clock includes four phases: charge-discharging phase, sensing phase, sampling phase and feedback phase. By the arrangement of clock, the system can realize closed-loop function under the condition without feedback electrode.

Fig. 2. Schematic diagram of the fourth-order ΣΔ interface circuit for micromachined accelerometer

4. Results and conclusion

The Matlab/Simulink simulation results are shown in figure3. As a comparison, the model of second-order ΣΔ accelerometer is also established. The simulation results indicate that in fourth-order system SNDR is 86.5dB, ENBO is 14.08bits when OSR is 128. As a comparison while in second-order system SNDR is 72.6dB, ENBO is 11.76bits. The results reflect that compared with a second-order micromachined ΣΔ modulator which only uses the sensing element as a loop filter, the fourth-order architecture leads to a better quantization noise shaping and achieves higher SNDR.

Fig. 3. The output spectrum of micromachined ΣΔ accelerometer (a) fourth-order; (b) second-order
An elaborate layout design with 0.5um CMOS process was completed. In order to ensure analog and digital parts do not disturb each other, the two parts are arranged with a larger distance, and separated analog and digital power supplies are arranged to reduce coupling noise from digital part. The sensing nodes are protected to shield from noise sources. Meanwhile in order to protect weak signals from affecting by environment noise, all important weak signals are shielded by guarding rings. Layout of the interface circuit is shown in figure 4, the area is 4.6mm × 3.7mm.

Simulation and post-simulation are carried out with Hspice. The simulation results indicate that the sensitivity of the system is 0.65V/g, the full measurement range can be achieved from -5g to +5g, supply voltage is ±5V and the power dissipation is 40mW.

An interface circuit of fourth-order ΣΔ accelerometer has been presented in this paper, in order to improve its performance, SC charge integration, CDS and one-bit quantization are employed in this design, the schematic and layout design are completed, the simulation results indicate that the closed-loop accelerometer has 14-bit resolution, and can be used in many applications.

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References