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The study of Si(5 5 12) cleaning in the ultra-high vacuum conditions

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Abstract

The LEED patterns, electronic structure and morphology of Si(5 5 12) substrate surface were studied after different temperature cleaning procedures: high temperature (1250 °C), low temperature (900 °C) and cleaning at 800 °C in low silicon atom flow. The low temperature annealing without using of Si flow has been determined as the optimal cleaning procedure for Si(5 512) substrate.

Keywords: silicon; vicinal surface

1. Introduction

According to literature data [1-3] the silicon surface (5 5 12) represents the one-dimensional periodical rows along [-110] direction. In Baski model [2] an unit cell consist of two equivalent (337) cells and one (225) cell with unit cell sizes 0.77x5.35 nm^2. Authors in work [3] have used high temperature annealing (T=1250 °C) and slow cooling from 900 °C to room temperature with rate about 1°C per minute for a creation of atomically clean Si(5 5 12)2x1 surface. It is known the type of majority carriers in Si n-type

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substrates change on holes in the subsurface layer after high temperature annealing that influences on the transport properties of a substrate and nanostructures grown on it. It is necessary to choose the cleaning conditions of Si(5 5 12) surface so that to receive an atomically smooth surface and minimize a transfer of dopants.

In present work the atomic and electronic structures and morphology of Si(5 5 12) surface are studied after temperature annealing at different temperatures in ultra-high vacuum conditions with and without additional silicon deposition at 850 ^{o}C.

2. Experiment

A cleaning of Si(5 5 12) substrate were made in ultrahigh vacuum OMICRON system equipped with AES (Auger electron spectroscopy), EELS (electron energy loss spectroscopy) and LEED (low energy electron diffraction) facilities, sample holder and silicon sources. Atomic force microscopy (AFM) investigations of samples morphology were performed using multimode scanning probe microscope Solver P47.

3. Results and discussions

For cleaning of Si(111) and Si(100) surfaces the low temperature annealing (T=800-850 ^{o}C) in silicon atom flow (Si deposition rate of about 0.05 nm/min) is usually used [4] for the formation of SiO volatile compound. The silicon dioxide (SiO_2) is removed at this procedure and a formation of atomically clean surface is occurred. This method we firstly used for Si(5 5 12) substrates. After the cleaning with Si rate of 0.02 mn/min at 800 ^{o}C the bulk and surface plasmons by EELS data (Fig. 1a) correspond to the atomically clean Si(5 5 12) surface, but by AES data the intensity of AES oxygen peak is reduced only in two times. Only reflections in the direction [66-5] with high background were observed on LEED patterns at Ep= 60 eV. The substrate surface after cleaning procedure consisted of smooth area and conglomerates of islands by AFM data. The smooth area corresponds to the non-remote SiO_2 layer, but island – to the deposited silicon. The poor cleaning is occurred due to small Si deposition rate. In the second experiment a Si rate was increased up to 0.2 nm/min at the same substrate temperature. On the LEED patterns the point reflections were observed with low background that testifies to the better ordering of a surface. AES peak of oxygen did not observed after a cleaning procedure that confirms the total remove of SiO_2. But by EELS data (Fig. 1a) the sample is characterized by a broad surface plasmon that corresponds to complex surface sample structure and is confirmed by AFM data. So, during the Si(5 5 12) surface cleaning the SiO_2 do not fully destroyed in small Si flow, but at higher Si flow the surface relief is increased.

To determine the temperature of SiO_2 destroy on Si(5 5 12) surface we carried out the next experiment: a sample was heated at the selected temperature during 2 minutes and after that it was cooled to the room temperature. The substrate temperature was increased from 400 ^{o}C with step 20 ^{o}C till then the Mg oxide layer did not started destroying by EELS and AES data. During the experiment it was observed that a layer of own oxide start to destroy at substrate temperature 860 ^{o}C.

For a comparison of LEED patterns obtained in the work [3] the additional experiment with high temperature cleaning of Si(5 5 12) surface was carried out: the substrate temperature was increased up to 900 ^{o}C and after that 5 flashes at 1250 ^{o}C during 1 second were done. At the end of the experiment the sample was cooled during 20 minutes down to room temperature. No other chemical elements except silicon attend on the sample surface after cleaning. By EELS data (Fig. 1a) the sample is characterized by plasmons, which positions correspond to atomically clean silicon surface. But the intensity of bulk plasmon is small as compared with the intensity of surface plasmon. The LEED pattern has point reflections and low background intensity (Fig 1b). As opposed to LEED pattern presented in work [3] in

our experimental LEED pattern six extra reflections were observed in [-110] direction, but not two. On LEED pattern it is also possible to mark out the direction of translation, which is located under the angle of 60° to the [66-5] direction. This reflection symmetry reminds of the Si(111)7x7 reconstruction, but as opposed to our case six main reflections do not form a regular hexagon.

According to AFM data (Fig. 1c) the Si(5 5 12) sample surface after high temperature cleaning consists of elongated one-dimensional rows with islands on their ends (root mean square roughness is 2.8 nm). Thereby, at high temperature cleaning it is possible to obtain enough smooth surfaces, but the surface reconstruction by LEED data is differed from data of work [3].

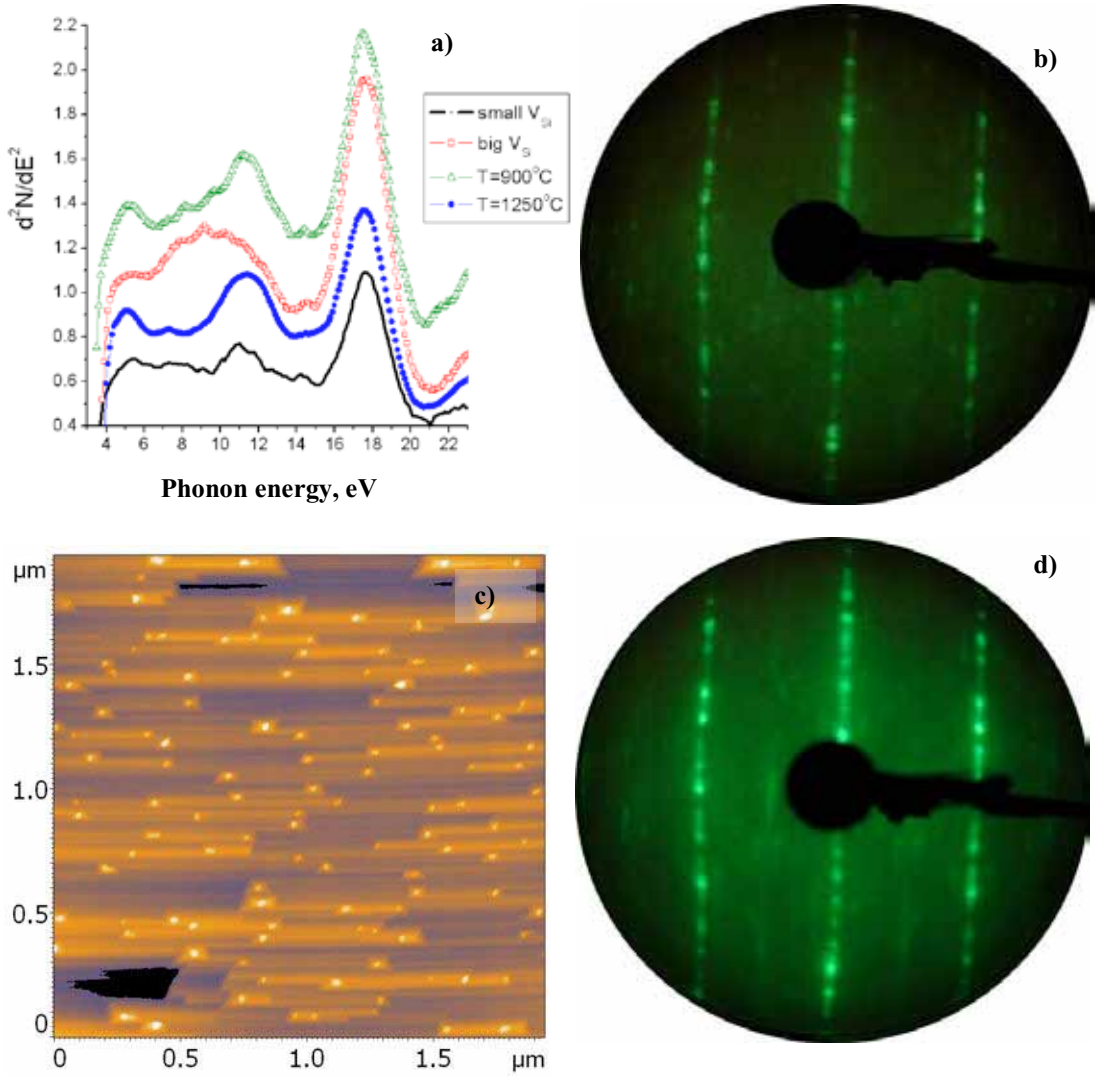

Fig. 1. (a) EELS spectra of Si(5 5 12) surface after cleaning at two Si deposition rates and two substrate temperatures; LEED pattern at E_p=60 eV (b) and AFM image of topography (c) after a cleaning procedure of Si(5 5 12) surface at high temperature flashes (T=1250 °C); (d) LEED pattern at E_p=60 eV after cleaning procedure of Si(5 5 12) sample surface at the annealing temperature T= 900 °C.

As the own oxide is destroyed at temperature 850 ^{o}C, the additional experiment on sample cleaning was else carried out. But the sample temperature did not increased higher 900 ^{o}C: a sample was annealed at 900 ^{o}C during 5 minutes, after that it was cooled down to room temperature during 20 minutes. By EELS data (Fig. 1a) the sample is characterized by plasmons, which positions and intensities correspond to atomically clean silicon surface By LEED data (Fig. 1d) reflections in the direction [66-5] are clearly seen than at high temperature cleaning. By AFM data the surface topography is identical to the one after high temperature cleaning.

4. Conclusions

Using three different cleaning procedures: high temperature (1250 ^{o}C) and low temperature (900 ^{o}C) annealing at 800 ^{o}C in the silicon atom flow the formation of atomically clean Si(5 5 12) surface has been investigated. It was established that low temperature (900 ^{o}C) annealing is the best procedure for Si(5 5 12) surface cleaning.

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References

[1] Wei J, Wang XS, Goldberg JL, Bartelt NC, Williams ED. Step-height mixtures on vicinal Si(111) surfaces. *Phys. Rev. Lett.* 1992; **68**: 3885-4.

[2] Baski AA, Erwin SC, Whitman LJ. A Stable High-Index Surface of Silicon: Si(5 5 12). *Science* 1995; **269**: 1556-5.

[3] Kumar M, Palival VK, Joshi AG, Govind, Shivaprasad SM. Formation of Sb submonolayer phases on high index Si(5 5 12) surface. *Surf. Sci.* 2005; **596**: 206-6.

[4] Galkin NG, Chusovitin EA, Goroshko DL, Bayazitov RM, Batalov RI, Shamirzaev TS, Zhuravlev KS. Morphological, structural and luminescence properties of Si/β-$FeSi_2$/Si heterostructures fabricated by Fe ion implantation and Si MBE. *J. Phys. D: Appl. Phys* 2007; **40**: 5319-8.