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Stacked Dual Oxide Nano MOS Parameter Optimization For 3-D IC Realization

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Abstract

With advent of nano technology, a threshold voltage of a MOSFET can be engineered. In order to increase the packing density of the transistors on multicore processor/ SOC with FPGA and processor, and 3-D IC realization, stacking of materials are necessary with lesser parasites like capacitance, voltage drop etc. In this paper, we present Silicon as a base material and metal like TiN (Titanium Nitride) as top layer is analyzed. The parameters of the different stacked materials are optimized to achieve required C_{Stack} (Stack Capacitance) and $V_{Th.}$ It is used explore the behavior of dual oxide MOS parameters like oxide material, electron affinity, bandgap, dielectric constant, and thickness.

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*Keywords:*TiN;Stack capacitance;stacked material;electron affinity;bandgap;dielectric constant;thickness.

1. Introduction

A CMOS circuit has been achieved throughout the last decades by scaling the geometric dimensions of the metal oxide-semiconductor field-effect-transistor (MOSFET). This scaling had to be accompanied by a decrease in the gate oxide thickness in order to maintain electrostatic control of the charges induced in the channel.

The silicon industry has been scaling SiO_2 aggressively for the past 15 years for low power, high performance CMOS logic applications. SiO_2 thin films as thin as 1.2 nm have already been utilized, however tunneling current increases exponentially for decreasing dielectric thickness, becoming significant for SiO_2 films thinner than 3 nm. Another problem for ultra-thin SiO_2 dielectric layers, when p+ polysilicon is used as gate contact in P-MOSFET's, is the low barrier against boron diffusion which causes a shift in the device threshold voltage. To overcome these problems, much research is directed to the substitution of SiO2 by high – κ materials making possible the use of

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thicker films. An alternative material, in spite of its relatively low dielectric constant, is SiO_xN_y because it is totally compatible with the silicon MOS technology and has improved properties, such as enhanced resistance to high field stress, enhanced hot carrier immunity, resistance against boron penetration, higher dielectric strength and higher dielectric constant, over conventional SiO2 . This material, obtained through a thermal oxynitridation, is already utilized in the MOS technology.

However, according with the international Technology Roadmap for Semiconductors, to meet the scaling goals. and at the same time keep the gate leakage current within tolerable limits (10 A/cm2) a dielectric constant higher than 25 will be needed. There are numerous challenges associated with implementing such an advanced gate stack, including ensuring adequate channel carrier mobility with the new high-κ dielectric, and reducing to tolerable levels the defects, charge trapping, and instabilities at the high-κ/ Si interface. Its important to observe that electric permittivity is not the unique criterion for dielectric performance, it is also desirable that the material present the following properties: to be amorphous, in order to eliminate leakage along grain boundaries, have a large optical bandgap, have a large band offset between its conduction/valence band and Si conduction/valence band, be thermodynamically stable and a good barrier against boron diffusion and present a good silicon dielectric interface quality

2. MOS Capacitors Fabrications

Two sets of MOS Capacitors were fabricated on p-type – oriented silicon wafers with resistivity in the 1-10 Ω.cm range. The silicon substrates were chemically cleaned by standard RCA procedure and subsequent etching in diluted HF solution to remove the native SiO2 layer. In sequence ~ 58 nm of TiN insulating layer was deposited by reactive sputtering from Ar (60%) and O2 (40%). In the case of the double gate layer, firstly a SiO2 thin film was thermally grown at 1000°C in O2. ambient following by the TiN film deposition. In the table I, are shown the set of fabricated MOS capacitors and studied in this work. The metallic contacts for all of the studied capacitors were obtained by the sputtering technique depositing 300 nm of Al. The 9x10-4 cm2 capacitor contact area was defined by photolithography and subsequent chemical etching; the contacts were annealed in forming gas atmosphere (4% of H2 and 96% of N2) at 450°C for 30 min. The high (1MHz) frequency C-V measurements.

3. Parameters and Its Varaiation

The parameters of MOS capacitors like energy, potential, electric field and charge density to measured. These parametyers are to be measured with respect to the distance. A threshold voltage of a MOSFET can be engineered. In order to increase the packing density of the transistors on multicore processor/ SOC with FPGA and processor, and 3-D IC realization, stacking of materials are necessary with lesser parasites like capacitance, voltage drop etc. In this paper, we present Silicon as a base material and metal like TiN (Titanium Nitride) as top layer is analyzed. The parameters of the different stacked materials are optimized to achieve required C_{Stack} (Stack Capacitance) and V_{Th}

4.Results

A.Energy

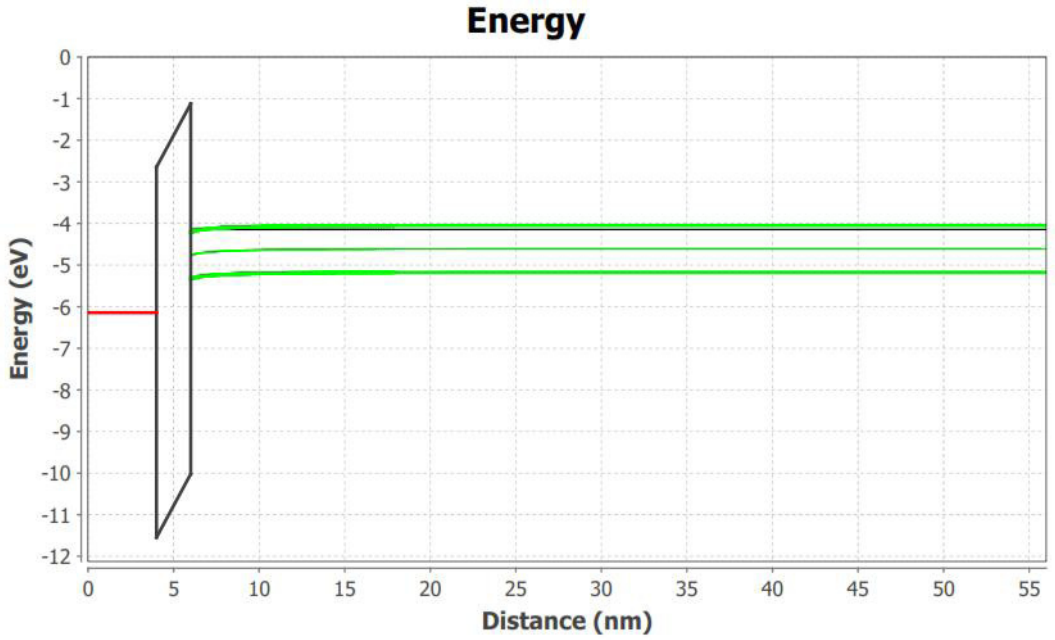

Figure 1.Energy verses Distance(nm).

B.Potential

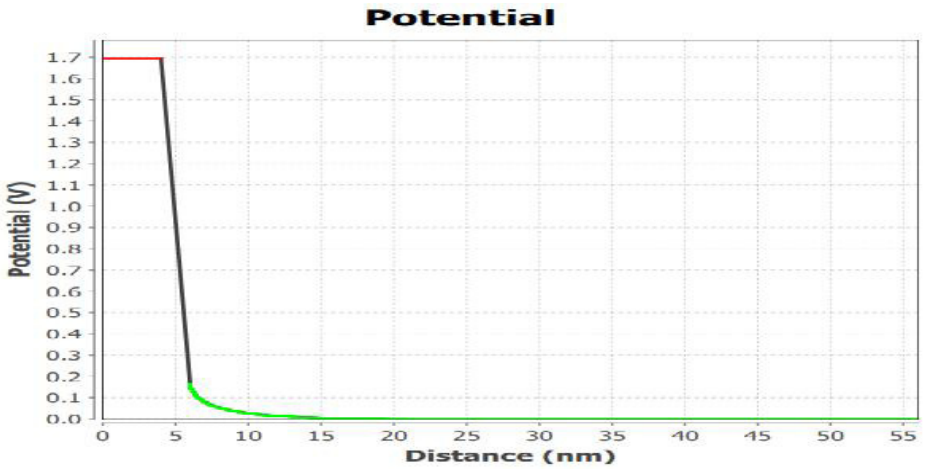

Figure 2.Potential verses Distance(nm)

C.Electric Field

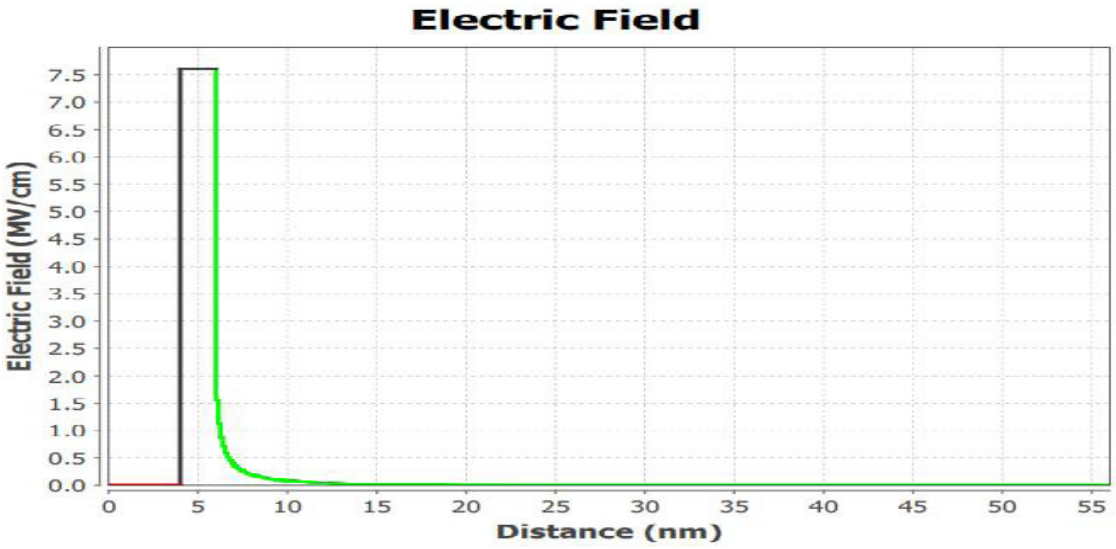

Figure 3.Electric Field verses Distance(nm)

D.Charge Density

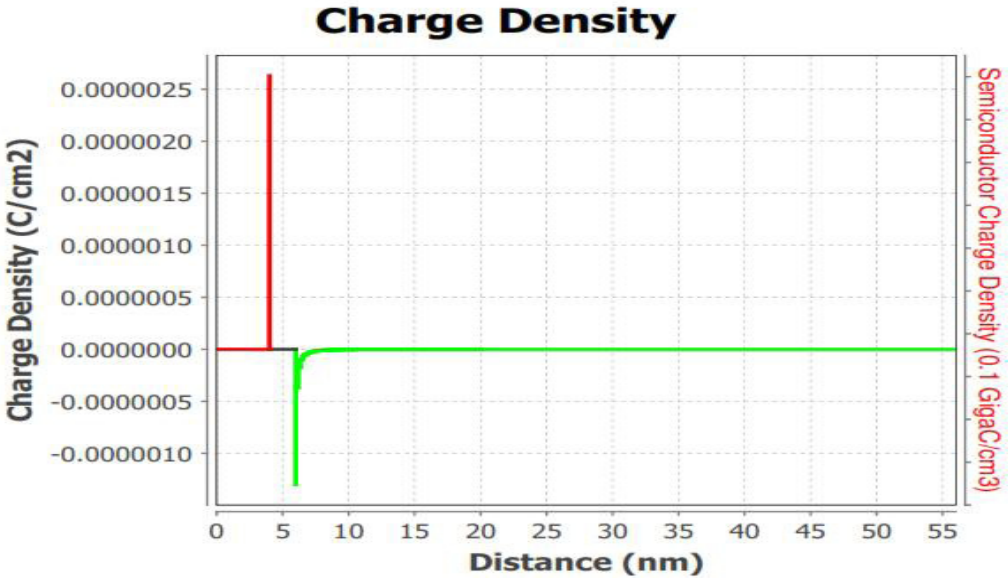

Figure 4.Charge Density verses Distance(nm)

5. Conclusions

The parameters of the different stacked materials are optimized to achieve required C_{Stack} (Stack Capacitance) and $V_{Th.}$ First result gives the information about energy levels.Second result explains the potential. Third result about electric field. Fourth result is the variation of charge density.

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