A Comparative Study of Sinusoidal PWM and Third Harmonic Injected PWM Reference Signal on Five Level Diode Clamp Inverter

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Abstract

This paper presents the comparative modulation of Sinusoidal PWM and Third Harmonic Injected PWM Reference signal with carrier signal PD, POD, and APOD on 5 Level Diode Clamp on a R-L load. All of these processes are simulated using the computer program MATLAB/Simulink. The result of simulation has shown the value of THD of line-line output voltage on both SPWM inverter and Third Harmonic Injection modulation inverter is generated with PD carrier signal generate a minimum THD.

Keywords: DC-MLI; SPWM; Harmonic Injected PWM; PD; POD; APOD; THD

1. Introduction

Multilevel inverter is a most popular for the industrial and electric power systems, because of it is high performance and low Harmonics. There are various types of Multi-Level Inverters such as Neutral-point clamped (NPC) or Diode Clamped (DC) inverter, Flying capacitor inverter and Cascade inverter. The difference among these kinds is as follow, when level of output voltage of Neutral-point clamped (NPC) or Diode Clamped inverter is

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increased, a number of diodes is also increased accordingly. When level of output voltage of Flying capacitor inverter is increased, a number of capacitor is also increased. It leads into higher cost and more switching losses. Cascaded multilevel inverters have advantages and benefits than the other, because it need no require in balancing capacitors and diodes, in another way it just need a separate DC source for each H-Bridge. [1]

Therefore, in this paper, Diode Clamped Inverter is used for comparative study, especially in carrier based SPWM and HIPWM. However the configurations of their modulation techniques are PD, POD and APOD as shown Fig.1.

2. Background

2.1. Diode Clamped Inverter

The first invention in multilevel converters was called as a neutral point clamped inverter. It was initially proposed of a 3 phase three level inverter. [2]

The main benefits and drawbacks of this topology are:
- The performance of its output waveform is high, especially at fundamental frequency.
- The whole capacitors have to be pre-charged at the beginning of the operation.
- Output voltage level depends on the capacitor voltage. In which, the equality of their capacitor is needed in order to keep the balancing of the 3 phase output voltage.

2.2 Reference Signal

SPWM

To generate Sinusoidal PWM signal a sine wave is provided as a reference signal. The frequency of a sine wave is equal to the frequency of the desired output voltage to the modulation of the carrier signal. The switching frequency of carrier signal must be higher than reference signal frequency as triple-N number. When both signals are modulated, it will generate the signal pulse for the switching devices for the inverter [3] as shown in Fig.2
In order to generate a Harmonic injection PWM signal, it may considered in a reference signal. The frequency of a reference signal must be the same of the desired output frequency. The reference signal is composed of fundamental and third harmonic frequency components as following equations. [4]

\[
V_{mA} = m_1 \sin(\omega_0 t) + k \sin(3\omega_0 t)
\]

\[
V_{mB} = m_2 \sin(\omega_0 + 120^\circ) + k \sin(3\omega_0 t)
\]

\[
V_{mC} = m_3 \sin(\omega_0 + 240^\circ) + k \sin(3\omega_0 t)
\]

\[
V_{mK} = k \sin(3\omega_0 t)
\]

Amplitude of k is between 0.15 and 0.2. As a result, the waveform shown in Fig.3

The reference signal that is a Harmonic injection signal which will be modulated with carrier signal as shown in Fig.3. After modulation, it will generate the signal pulse to the switching devices in the inverter as shown in Fig.4
2.3. Modulation Techniques

The modulation techniques that used in this paper are in 3 models Phase Disposition (PD), Phase Opposition Displacement (POD), and Alternative Phase Opposition Displacement (APOD) [5].

Phase Disposition (PD) modulation technique means that all of the carrier signals are in phase as shown in Fig.5.

![Fig. 5 Phase Disposition (PD) modulation technique for Five Level DCMLI](image)

Phase Opposition Disposition (POD) modulation techniques means that the carrier signals above the zero line of sinusoidal modulating waveform are $180^\circ$ out of phase, comparing with the carrier signal below the zero line as shown in Fig.6.

![Fig.6. Phase Opposition Disposition (POD) modulation technique for Five-Level DCMLI](image)

Alternative Phase Opposition Disposition (APOD), modulation techniques means that each carrier signal is phase shifted by $180^\circ$ from its adjacent carriers as shown in Fig.7.

![Fig.7. Alternative Phase Opposition Disposition (APOD) modulation technique for Five-Level DCMLI](image)
3. Simulation Results

3.1. Modulation signal

A modulation signal a carrier based SPWM and HIPWM on various methods such as PD, POD, and APOD are shown as Fig.8 to Fig.13. By the way, these simulation results are done by using MATLAB/Simulink program.

Fig.8. Modulation signal of SPWM Inverter on PD modulation technique

Fig.9. Modulation signal of SPWM Inverter on POD modulation technique

Fig.10. Modulation signal of SPWM Inverter on APOD modulation technique
Fig. 11. Modulation signal of HIPWM Inverter on PD modulation technique

Fig. 12. Modulation signal of HIPWM Inverter on POD modulation technique

Fig. 13. Modulation signal of HIPWM Inverter on APOD modulation technique
3.2. Five Level Diode Clamped Inverter

Therefore, this modulation method as described above has done by a five level diode clamp inverter which supported modulation and compare the values from section 3.1. The parameters from Table 1 is used with the circuit of 5 level DC-MLI as shown in Fig.14.

Table 1. Experimental parameters.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specifications</th>
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<tbody>
<tr>
<td>Output Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>4850 Hz</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>540 Vdc</td>
</tr>
<tr>
<td>C1 ,C2 ,C3 ,C4</td>
<td>22,000 µF</td>
</tr>
<tr>
<td>Load RL</td>
<td>1kW ,PF 0.8</td>
</tr>
</tbody>
</table>

Table 2. Switching states for Five Level DCMLI

<table>
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<tr>
<th>$V_L$</th>
<th>Sa1</th>
<th>Sa2</th>
<th>Sa3</th>
<th>Sa4</th>
<th>Sa’1</th>
<th>Sa’2</th>
<th>Sa’3</th>
<th>Sa’4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}/2$</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_{dc}/4$</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
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</tr>
<tr>
<td>-$V_{dc}/2$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>-$V_{dc}/4$</td>
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<td>1</td>
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</tbody>
</table>
3.3. **FFT Analysis of THDV**

This paper will study impact of the THDV of the output voltage of the five level diode clamp inverter. Either no-load and RL load a 1kW and PF = 0.8 with modulation signal from section 3.1.

As a result, the THDV value of $V_{ab}$ of each modulation scenario has shown as Fig.15 to Fig.26.

![Fig.15. THDV of output voltage (Vab) of SPWM Inverter on PD modulation technique at no load condition](image1)

![Fig.16. THDV of output voltage (Vab) of SPWM Inverter on POD modulation technique at no load condition](image2)

![Fig.17. THDV of output voltage (Vab) of SPWM Inverter on APOD modulation technique at no load condition](image3)
Fig.18. THD$_V$ of output voltage (Vab) of HIPWM Inverter on PD modulation technique at no load condition

Fig.19. THD$_V$ of output voltage (Vab) of HIPWM Inverter on POD modulation technique at no load condition

Fig.20. THD$_V$ of output voltage (Vab) of HIPWM Inverter on APOD modulation technique at no load condition
Fig. 21. THD_v of output voltage (Vab) of SPWM Inverter on PD modulation technique at 1 kW, PF 0.8 load condition.

Fig. 22. THD_v of output voltage (Vab) of SPWM Inverter on POD modulation technique at 1 kW, PF 0.8 load condition.

Fig. 23. THD_v of output voltage (Vab) of SPWM Inverter on APOD modulation technique at 1 kW, PF 0.8 load condition.
Fig. 24. THDV of output voltage (Vab) of HIPWM Inverter on PD modulation technique at 1 kW, PF 0.8 load condition

Fig. 25. THDV of output voltage (Vab) of HIPWM Inverter on POD modulation technique at 1 kW, PF 0.8 load condition

Fig. 26. THDV of output voltage (Vab) of HIPWM Inverter on APOD modulation technique at 1 kW, PF 0.8 load condition
4. Conclusion

A comparative modulation of Sinusoidal PWM and Third Harmonic Injected PWM Reference signal with carrier signal PD, POD, and APOD on 5 level diode clamp with a R-L load=1kW PF=0.8 and no load are studied in this paper. The result of simulation shown that a PD carrier signal have a minimum value of THD$_v$ line-line output voltage on Third Harmonic Injection modulation

References


