Even Circuits in Planar Graphs

P. D. SEYMOUR

Merton College, Oxford, England

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We prove that a planar graph can be partitioned into edge-disjoint circuits of even length, if and only if every vertex has even valency and every block has an even number of edges.

1. Introduction

It is elementary that if \( G = (V, E) \) is a graph, a necessary and sufficient condition for \( E \) to be expressible as an edge-disjoint union of circuits is that every vertex has even valency. (For convenience, we call such a graph Eulerian, even if it is not connected.) We study a variation of this problem, viz., when can \( E \) be partitioned into even circuits? It is certainly necessary that \( G \) should be Eulerian, and that every block of \( G \) should have an even number of edges, but this is not in general sufficient. However, it is sufficient for planar graphs. This is our main result and we prove it in Section 3.

One reason for interest in even circuits is a connection with the four-colour theorem. That implies that in every cubic 2-connected planar graph there is a set of even circuits in which each edge occurs twice. We might therefore hope that even circuits in planar graphs have other nice properties. (Extra motivation came from a claim of Szekeres [4], that any cubic graph with such a "2-covering" by even circuits is 3-edge-colourable. However, Szekeres' result turns out to be incorrect—see Section 4.) There is another "even circuit" consequence of the four-colour theorem as well, which we discuss in Section 2, and which we use for our main proof.

For non-planar graphs the problem about partitions into even circuits is still open. The condition of our theorem is no longer sufficient; for example, \( K_5 \) is not expressible in the required way, although it is Eulerian, 2-connected, and has an even number of edges. Another counterexample may be obtained as follows: take the Petersen graph; let \( F \) be a 1-factor; for some edge \( e \in F \), replace \( e \) by two edges in series; and for each \( f \in F \), add a new
vertex of valency 2, adjacent to the ends of \( f \). We shall therefore confine ourselves to planar graphs.

Let us clarify some terminology. Graphs are finite, undirected, and may have loops or multiple edges. It will be convenient sometimes to identify subgraphs such as paths and circuits with their edge-sets, when there is no risk of confusion. We denote the vertex- and edge-sets of \( G \) by \( V(G) \), \( E(G) \), respectively. Paths and circuits have no "repeated" vertices, and their length is the number of edges in them. (The path with one vertex and no edges is recognised, but circuits must have non-zero length.) Paths and circuits are, loosely, even (or odd) if they have even (or odd) length. A block of a graph is a maximal subgraph with the properties that it is connected and any two distinct edges are in a circuit. \( G \) is \( k \)-connected if the result of deleting any set of \( k' < k \) vertices is connected. A cut is the set of edges with one end in \( X_1 \) and the other in \( X_2 \), where \( (X_1, X_2) \) is a partition of \( V \). An isthmus is an edge \( e \) such that \( \{e\} \) is a cut. \( G \) is \( k \)-edge-connected if it is connected and has no non-empty cut of cardinality \( < k \). The valency of a vertex is the number of edges incident with it; loops are counted twice. If \( v \) has valency 2, and is incident with distinct edges \( e_1, e_2 \), we say that \( e_1, e_2 \) are in series.

A 1-factor \( F \) of \( G \) is a subset of \( E \) such that each vertex of \( G \) is incident with exactly one edge in \( F \). A circuit partition \( (C_1, \ldots, C_r) \) is a partition of \( E(G) \) into sets \( E(C_1), \ldots, E(C_r) \), which are the edge-sets of circuits \( C_1, \ldots, C_r \). An even circuit partition is one in which every circuit \( C_i \) is even.

2. SOME LEMMAS

We shall need the following result.

(2.1) Let \( G = (V, E) \) be a planar 2-edge-connected cubic graph, and let \( F \) be a 1-factor. Then there is a set of circuits of \( G \) so that each \( f \in F \) is in exactly two of them and each \( e \in E - F \) is in exactly one.

(Incidentally, this may be regarded as a theorem about even circuits; for every circuit in such a set consists of edges alternately in \( F \) and in \( E - F \), and so is necessarily even.)

Proof. From the four-colour theorem, \( G \) is 3-edge-colourable, and so has three edge-disjoint 1-factors \( F_1, F_2, F_3 \). Then for \( i = 1, 2, 3 \), \( (F_i - F) \cup (F - F_i) \), is expressible as a disjoint union of circuits, and by taking all these circuits for \( i = 1, 2, 3 \) we obtain a set satisfying (2.1).

It is also possible to prove (2.1) without assuming the four-colour theorem, for it is a corollary of the following (difficult) theorem of Fleischner [1], as he observed in that paper.
(2.2) Let $G = (V, E)$ be a planar Eulerian graph, and let $\mathcal{D}$ be a set of unordered pairs of adjacent edges of $G$, so that for any $v \in V$ and $e \in E$ incident with $v$, there is at most one $f$ incident with $v$ so that $\{e, f\} \in \mathcal{D}$. Suppose that no cut $\{e, f\} \in \mathcal{D}$. Then there is a circuit partition $(C_1, \ldots, C_r)$ of $G$ so that $D \subseteq C_j$ for $1 \leq i \leq r$ and $D \in \mathcal{D}$.

To derive (2.1) from this, let $\mathcal{D}$ contain all pairs of adjacent edges of $G$ not in $F$, contract all edges in $F$, and apply (2.2) to the result.

Fleischner observed that this proof shows also that (2.1) is true if we replace the "planar" hypothesis by the weaker condition that the result of contracting $F$ is planar. However, it does not hold for all 2-edge-connected cubic graphs; for example, if $G$ is the Petersen graph and $F$ is any 1-factor, it is false.

Incidentally, (2.1) was given the following extension in [3]. (The proof there does assume the four-colour theorem, however.)

(2.3) Let $G = (V, E)$ be a planar graph, and for each $e \in E$ let $p(e) \geq 0$ be an integer. Then there is a list of circuits of $G$ using each edge $e$ $p(e)$ times, if and only if for each cut $D$, $\sum_{e \in D} p(e)$ is even and is not less than $2p(f')$ for any $f' \in D$.

A fortiori, (2.3) does not extend to non-planar graphs in general.

We have discussed the background to (2.1) at some length, because it seems to be of interest in itself, being fairly deep and capable of several different generalizations. (Theorems (2.2) and (2.3) above are two such generalizations, and our main theorem is a third. To see this, take $G, F$ as in (2.1), for each $f \in F$ add a new vertex of valency 2 adjacent to the ends of $f$, and if $|E|$ is odd replace some $e \in E - F$ by two edges in series. Then application of our main theorem to the graph produced yields the assertion of (2.1) for $G, F$.)

In fact, for our application, we need a slight extension of (2.1), as follows.

(2.4) Let $G = (V, E)$ be a planar 2-edge-connected graph with maximum valency 3, and for each edge $e$ let $p(e)$ be 1 or 2. Suppose that for each $v \in V$, 

$$\sum (p(e) : e \text{ incident with } v)$$

is equal to 2 or 4. Then there is a set $\mathcal{C}$ of circuits using each edge $e$ $p(e)$ times.

Proof. $G$ has no isthmus. If $e_1, e_2 \in E$ are in series then $p(e_1) = p(e_2)$, since $p(e_1) + p(e_2)$ is even by hypothesis, and so the result holds for $G$ if and only if it holds for the graph obtained by contracting $e_2$. But $G$ has
maximum valency 3, and we may therefore assume that $G$ is cubic. Then 
\{e: p(e) = 2\} is a 1-factor of $G$, and the result follows from (2.1).

In order to apply (2.4) we also need the following technical lemma.

(2.5) Let $G, p$ be as in (2.4), let $\mathcal{C}$ be such a list of circuits, and let $F = \{e: p(e) = 2\}$. Suppose that $|E|$ is even. Then there is a function $t: F \to \mathcal{C}$ such that

(i) $f \in t(f)$ for each $f \in F$,

(ii) $|\{f \in F: t(f) = C\}| + |C|$ is even for each $C \in \mathcal{C}$.

Proof. Let $H$ be a graph with vertex set $\mathcal{G}$ and with edge set $F$, where $f \in F$ is incident with $C \in \mathcal{C}$ just when $f \in C$. We claim that $H$ is connected. For if not, there is a partition $(\mathcal{G}_1, \mathcal{G}_2)$ of $\mathcal{G}$ such that $\mathcal{G}_1, \mathcal{G}_2 \neq \emptyset$ and such that no $f \in F$ is contained both in a member of $\mathcal{G}_1$ and in a member of $\mathcal{G}_2$. Let

$$E_i = \bigcup_{C \in \mathcal{G}_i} E(C) \quad (i = 1, 2).$$

Then $E_1 \cap E_2 \cap F = \emptyset$ by choice of $\mathcal{G}_1, \mathcal{G}_2$; and $(E_1 \cap E_2) - F = \emptyset$ by choice of $\mathcal{G}$. Thus $E_1 \cap E_2 = \emptyset$. But $E_1 \cup E_2 = E$, and yet each $E_i$ is a non-trivial union of circuits of $G$, and $G$ is connected and has maximum valency 3. This is impossible.

Thus $H$ is connected. Let $\mathcal{G}^* \subseteq \mathcal{G}$ be the set of circuits $C \in \mathcal{G}$ with $|C|$ odd. Then $|\mathcal{G}^*| \equiv |E - F| \mod 2$, and so by hypothesis $|\mathcal{G}^*| \equiv |F| \mod 2$. We claim that the edges of $H$ can be directed so that $C \in \mathcal{G}$ has odd out-valency if and only if $C \in \mathcal{G}^*$. To see this, direct the edges of $H$ so that as many vertices of $H$ as possible have out-valency with correct parity. Since $|E(H)| = |F| \equiv |\mathcal{G}^*| \mod 2$, there are an even number of vertices of $H$ with out-valency of incorrect parity. Assume for a contradiction that there are at least two. $H$ is connected, and so there is a path in $H$ joining two such vertices. By reversing the direction of all edges in this path, we increase the number of vertices with out-valency of correct parity, a contradiction. Thus the edges of $H$ can be directed in the required manner.

For $f \in F$, define $t(f)$ to be the tail of $f$ in $H$, in this directing. Then $t$ satisfies (2.5).

There is another lemma worth extracting from the main proof. If $X, Y$ are disjoint subsets of the vertex set of a circuit $C$, we say that $X, Y$ interlace on $C$ if the vertices of $C$ in $X \cup Y$ are alternately in $X$ and in $Y$. (Thus if $X, Y$ interlace on $C$ then $|X| = |Y|$.)

(2.6) If $C, C', C''$ are three circuits of a planar graph, and $C', C''$ have precisely one vertex $v$ in common, and $C$ does not pass through $v$, and
$|V(C) \cap V(C')| \geq 2$, $|V(C) \cap V(C'')| \geq 2$, then $V(C) \cap V(C')$, $V(C) \cap V(C'')$ do not interlace on $C$.

The proof is clear but awkward to write out, and we omit it.

3. PROOF OF THE THEOREM

The theorem is the following.

(3.1) Let $G = (V, E)$ be a planar graph. Then $G$ has an even circuit partition if and only if $G$ is Eulerian and every block of $G$ has an even number of edges.

Proof: The "only if" part is clear. We prove the "if" part by contradiction. Suppose that it is false. Then we can choose a graph $G = (V, E)$ with properties (1),..., (5) below:

(1) $G$ is planar, Eulerian, and every block of $G$ has an even number of edges.

(2) $G$ has no even circuit partition.

(3) Subject to (1), (2), $G$ has $|E|$ minimum.

(4) $G$ has no isolated vertices.

(5) Subject to (1),..., (4), $G$ has $|V|$ maximum.

(6) $G$ has no loops.

For if $e$ is a loop, incident with $v \in V$, then the subgraph $\langle \{v\}, \{e\} \rangle$ is a block of $G$ with an odd number of edges, contrary to (1).

(7) $G$ is 2-connected.

Some block $B$ of $G$ has no even circuit partition, because $G$ does not. However, $G$ has a circuit partition, and hence so does $B$; thus $B$ is Eulerian. By (3) and (4), $B = G$. Thus $G$ is 2-connected.

A 2-separation of $G$ is a partition $(E_1, E_2)$ of $E$ so that $|E_1|, |E_2| \geq 2$ and so that there are at most two vertices incident both with an edge in $E_1$ and with an edge in $E_2$. Since $G$ is 2-connected and loopless, it follows that when $(E_1, E_2)$ is a 2-separation there are exactly two such vertices $u_1, u_2$ say. We classify 2-separations into four types, as follows. Since $|E|$ is even, there exists $c_1 \in \{0, 1\}$ so that

$$|E_i| \equiv c_1 \mod 2 \quad (i = 1, 2)$$

and since $G$ is Eulerian, there exists $c_2 \in \{0, 1\}$ so that

$$|\{e \in E_i: e \text{ incident with } u_j\}| = c_2 \mod 2 \quad (i = 1, 2, j = 1, 2).$$
We say that \((E_1, E_2)\) is a 2-separation of type \((c_1, c_2)\) at \(\{u_1, u_2\}\). (In fact we are only concerned with those of type \((1, 0)\).)

(8) If \((E_1, E_2)\) is a 2-separation of type \((1, 0)\) at \(\{u_1, u_2\}\), then there is a vertex \(v \neq u_1, u_2\) of valency 2 in \(G\) and three edges \(e_1, e_2, e_3\) joining the pairs \((v, u_1), (v, u_2), (u_1, u_2)\), respectively, so that \(E_i = \{e_1, e_2, e_3\}\) for some \(i\).

For \(|E_1|\) is odd and \(|E_1| \geq 2\) by hypothesis. If \(|E_1| = 3\), the result follows easily. We may therefore suppose that \(|E_1| \geq 4\), and similarly that \(|E_2| \geq 4\), for a contradiction. Delete all edges in \(E_1\), take a new vertex \(v'\), and add new edges \(e'_1, e'_2, e'_3\) joining the pairs \((v', u_1), (v', u_2), (u_1, u_2)\) respectively, forming a graph \(G_1\). Clearly \(G_1\) is a planar Eulerian block with an even number of edges. Moreover, it has fewer edges than \(G\), and so by (3) \(G_1\) has an even circuit partition \((C_1, \ldots, C_r)\) say. One of these circuits \((C_i\) say\) uses \(e'_1\), and a different one \((C_j\) say\) uses \(e'_2\), \(e'_3\). Thus in \(G\) there are two paths \(P_1, P_2\) and circuits \(C_3, \ldots, C_r\), with the following properties:

(i) \(P_1\) is odd, and \(P_2, C_3, \ldots, C_r\) are even,
(ii) \(P_1, P_2\) both join \(u_1, u_2\),
(iii) \(P_1, P_2, C_3, \ldots, C_r\) partition \(E_1\).

Similarly we may obtain such a partition \(P'_1, P'_2, C'_3, \ldots, C'_r\) for \(E_2\). But then if \(C, C'\) denote the circuits of \(G\) made by \(P_1 + P'_1\) and \(P_2 + P'_2\), then \(C, C', C_3, \ldots, C_r, C'_3, \ldots, C'_r\) are all even circuits, and give an even circuit partition of \(G\), a contradiction. This proves (8).

If \(e_1, e_2 \in E\) join the pairs \((x, y), (x, z)\) where \(x, y, z \in V\) are distinct, and \(y, z\) are adjacent in \(G\) and one of \(y, z\) has valency 2, we say that \(e_1, e_2\) are near-parallel.

(9) For any \(v \in G\) and edge \(e\) incident with \(v\), there is at most one edge \(f\) incident with \(v\) so that \(e, f\) are near-parallel.

For suppose that \(e\) is near-parallel with \(f_1, f_2\). Let the other ends of \(e, f_1, f_2\) be \(u, u_1, u_2\), respectively. There are two cases:

(i) \(u_1 \neq u_2\). Then \(u\) has valency \(\geq 3\) in \(G\), and so \(u_1, u_2\) both have valency 2. The graph obtained from \(G\) by deleting \(u_1, u_2\) is 2-connected, Eulerian, planar, and has an even number of edges, and so by (3) it has an even circuit partition. By adding to this the circuit \(uu_1uu_2(v)\) we obtain an even circuit partition of \(G\), which is impossible.

(ii) \(u_1 = u_2 = w\) say. Then \(f_1, f_2\) are parallel, and \(w\) has valency \(\geq 3\) in \(G\), and so \(u\) has valency 2. The graph obtained by deleting \(f_1, f_2\) is 2-connected, etc., and we obtain a contradiction as before.

To apply the results of Section 2, we need to show that every vertex of \(G\)
has valency 2 or 4, and that each vertex of valency 4 is incident with a pair of near-parallel edges. Therefore, let \( v \) be any vertex of valency \( k \geq 4 \), and let \( e_1, e_2, \ldots, e_k, e_{k+1} = e_1 \) be the edges incident with it, in clockwise order in some drawing of \( G \) in the plane. Choose this numbering so that if any consecutive pair of \( e_1, \ldots, e_{k+1} \) are near-parallel, then \( e_2, e_3 \) are.

Let the ends of \( e_1, \ldots, e_k \) different from \( v \) be \( v_1, \ldots, v_k \) respectively. Let \( G' \) be a graph obtained from \( G \) as follows. Delete \( e_1, e_k \); take a new vertex \( v' \) and two new edges \( e'_1, e'_2 \); and let \( e'_1 \) be incident with \( v', v_i \) \((i = 1, 2) \). Then \( G' \) is planar, Eulerian, has the same number of edges as \( G \) but more vertices, and has no isolated vertices.

(10) Every block of \( G' \) has an even number of edges.

For it is easy to see that \( e'_1, e'_2 \) are in the same block \( B_1 \), that \( v_3, \ldots, v_k \) are in the same block \( B_s \) for some \( s \geq 1 \), and that the remaining blocks can be labelled \( B_2, \ldots, B_{s-1} \) so that for \( 1 \leq i, j \leq s \), \( B_i \) and \( B_j \) are vertex-disjoint unless \( |j - i| \leq 1 \), and if \( |j - i| = 1 \) then \( B_i \) and \( B_j \) have exactly one vertex in common. If some block has an odd number of edges, then at least two do (since \( G \) has an even number of edges) and so we may choose \( i < s \) minimum so that \( B_i \) has an odd number of edges. Then

\[
((B_1 - \{e'_1, e'_2\}) \cup \{e_1, e_2\} \cup B_2 \cup \cdots \cup B_i, B_{i+1} \cup \cdots \cup B_s)
\]

is a 2-separation of \( G \) of type \((1, 0)\) (since each \( B_i \) is Eulerian). By (8), either \( e_1, e_2 \) are near-parallel, or \( k = 4 \) and \( e_3, e_4 \) are near-parallel. Thus \( e_2, e_3 \) are near-parallel, by our numbering of \( e_1, \ldots, e_k \), contrary to (9).

(11) \( G \) has a circuit partition \((C_1, \ldots, C_r)\), where \( r \geq 3 \), \( C_1, C_r \) are odd, \( C_2, \ldots, C_{r-1} \) are even, \( C_1, C_r \) have precisely the vertex \( v \) in common, and \( e_1 \in C_1, e_2 \in C_r \).

For by (5), \( G' \) has an even circuit partition \((C'_1, \ldots, C'_{r-1})\) say, where \( e'_1, e'_2 \in C'_1 \). But \( G \) has no even circuit partition, and so \((C'_1 - \{e'_1, e'_2\}) \cup \{e_1, e_2\}\) is not the edge-set of an even circuit of \( G \), nor can it be expressed as the union of the edge-sets of two edge-disjoint even circuits. Thus \( C'_1 \) passes through \( v \), and there are two odd circuits \( C_1, C_r \) of \( G \) with precisely the vertex \( v \) in common, and with \( e_1 \in C_1, e_2 \in C_r \), so that

\[
(C'_1 - \{e'_1, e'_2\}) \cup \{e_1, e_2\} = C_1 \cup C_r.
\]

The result follows, taking \( C_i = C'_i \) \((2 \leq i \leq r - 1)\).

(12) We can reorder \( C_2, \ldots, C_{r-1} \) so that for \( 1 \leq i, j \leq r \), \( C_i \) and \( C_j \) have a vertex different from \( v \) in common if and only if \( |j - i| \leq 1 \).
For $G - v$ is connected, and so for some $r' \geq 3$ there is a sequence

$$C_1 = D_1, D_2, \ldots, D_{r'} = C_r,$$

where each $D_i$ is one of $C_1, \ldots, C_r$ and for $1 \leq i \leq r' - 1$, $D_i$ and $D_{i+1}$ have a vertex different from $v$ in common. Choose a minimal such sequence. Then for $j > i + 1$, $D_i$ and $D_j$ have no vertices in common, and for $i \neq j$, $D_i \neq D_j$.

Let $E'$ be the union of the edge-sets of the $D_i$'s. Then the graph $G' = (V, E')$ (with the same incidences as $G$) is 2-connected except for isolated vertices, and is Eulerian and planar and has an even number of edges. If $E' \neq E$ then by (3) $G'$ has an even circuit partition, and by adding to this all those $C_i$'s not in the sequence $D_1, \ldots, D_{r'}$ we obtain an even circuit partition for $G$, a contradiction. Thus $E' = E$, and so each $C_i$ is one of $D_1, \ldots, D_{r'}$, and $r' = r$, and (12) is proved.

Henceforth, we shall assume $C_1, \ldots, C_r$ ordered in this way.

(13) Every vertex distinct from $v$ has valency 2 or 4.

For from (12), any vertex distinct from $v$ is in at most two $C_i$'s, and so has valency at most 4.

(14) All vertices of $G$ have valency 2 or 4.

For $v$ is an arbitrary vertex of $G$ with valency $\geq 4$, and certainly $G$ has at least two such vertices, by (1) and (2). Thus (14) follows from (13).

(15) None of $C_2, \ldots, C_{r-1}$ pass through $v$.

For $C_1, \ldots, C_r$ are edge-disjoint, and $C_1, C_r$ pass through $v$, and yet by (14), $v$ has valency 4.

We now begin the second part of the proof, that $e_2, e_3$ are near-parallel. For $1 \leq i \leq r$, let $V_i$ be the vertex set of $C_i$.

(16) If $e_2, e_3$ are not near-parallel, then for $1 \leq i \leq r - 1$, $|V_i \cap V_{i+1}| \geq 2$.

For if $|V_i \cap V_{i+1}| = 1$, then $(C_1 \cup \ldots \cup C_i, C_{i+1} \cup \ldots \cup C_r)$ is a 2-separation of $G$ of type $(1,0)$. Thus by (8) two edges incident with $v$ are near-parallel, and by our numbering of $e_1, \ldots, e_k$, we have that $e_2, e_3$ are near-parallel.

(17) If $e_2, e_3$ are not near-parallel, then for $2 \leq i \leq r - 1$, $V_i \cap V_{i-1}$ and $V_i \cap V_{i+1}$ do not interlace on $C_i$.

For let $P$ be a path of $G$ with no edges in $C_{i-1}, C_i$ or $C_{i+1}$, but with one end in $C_{i-1}$ and one in $C_{i+1}$, and no other vertices in $C_{i-1}, C_i$ or $C_{i+1}$. (P
necessarily passes through \( v \); it has zero length if \( r = 3 \), but non-zero length otherwise.) Delete all edges of \( G \) not in \( P, C_{i-1}, C_i, C_{i+1} \), and contract all edges in \( P \); then (17) follows from (2.6) applied to the graph produced.

\[ (18) \quad e_2, e_3 \text{ are near-parallel.} \]

For suppose not. Choose \( i \) with \( 2 < i < r - 1 \). By (17) we may assume that there are two vertices of \( V_{i-1} \) on \( C_i \) with no vertex of \( V_{i+1} \) between them, by reversing the order \( C_1, \ldots, C_r \) if necessary. But \( C_i \) has at least two vertices of \( V_{i+1} \), and so there exist \( x, y \in V_i \cap V_{i+1} \), distinct, which divide \( C_i \) into two paths \( P_1, P_2 \), so that \( P_1 \) passes through at least two vertices of \( V_{i-1} \) but no vertices of \( V_{i+1} \) except \( x, y \). Let \( R \) be a path in \( C_{i+1} \) joining \( x, y \), not passing through \( v \). Then \( P_1 + R \) is a circuit of \( G \).

Let \( G_0 \) be the subgraph of \( G \) consisting of the vertices and edges in the circuits \( C_1, \ldots, C_{i-1}, P_1 + R \). Then \( G_0 \) is planar and Eulerian, and has at most \(|E| - 2 \) edges; and it is 2-connected, since any consecutive pair of \( C_1, \ldots, C_{i-1}, P_1 + R \) have at least two vertices in common. Replace some edge of \( R \) by two edges in series if \( G_0 \) has an odd number of edges, and otherwise do not; let the result be \( G_1 \). Then \( G_1 \) is planar, Eulerian, 2-connected, has an even number of edges and has fewer edges than \( G \), and so by (3) it has an even circuit partition \( (D_1, \ldots, D_s) \), say, where \( D_1 \) passes through \( x, y \). Let \( x, y \) divide \( D_1 \) into paths \( Q_1, Q_2 \). Then clearly just one of \( Q_1, Q_2 \) meets \( V_1 \cap \cdots \cap V_{i-1} ; Q_1 \), say. \( Q_2 \) is thus either \( R \) or \( R \) with one edge subdivided.

Let \( G_2 \) be the subgraph of \( G \) consisting of the vertices and edges in \( P_2, Q_1, C_{i+1} \ldots, C_r \). Then \( G_2 \) is planar and Eulerian, and \(|E(G_2)| < |E(G)| \) (since \( C_{i-1} \notin Q_1 \)). Moreover, \( G_2 \) is 2-connected; for consecutive pairs of \( C_{i+1}, \ldots, C_r \) have at least two vertices in common, and \( P_2, Q_1 \) are both paths joining \( x, y \). And \( G_2 \) has an even number of edges; for

\[ |Q_1| = |Q_2| = |R| + |E(G_0)| = |P_1| + 1 = |P_2| + 1 \mod 2 \]

and

\[ |E(G_2)| = |P_2| + |Q_1| + 1 \mod 2. \]

By (3), \( G_2 \) has an even circuit partition \( (D'_1, \ldots, D'_s) \). But then

\[ (D_2, \ldots, D_s, D'_1, \ldots, D'_s) \]

is an even circuit partition of \( G \), a contradiction.

We have therefore proved

\[ (19) \quad \text{If } v \text{ has valency } 4 \text{ in } G \text{ then two edges incident with } v \text{ are near-parallel.} \]
We can now apply the results of Section 2. Let \( F \) be the set of all edges \( f \) of \( G \) such that there is a vertex, \( v_f \), say, of valency 2, adjacent to both ends of \( f \). By (9), \( v_f \) is unique. Delete all vertices \( v_f \) (\( f \in F \)), forming a graph \( H \), say. Then \( H \) is 2-connected and 2-edge-connected and has an even number of edges. Every vertex of \( H \) has valency 2 or 3, by (14). If \( H \) is a circuit then it is an even circuit (since \( |E(H)| \) is even) and \( F = E(H) \) since \( G \) is Eulerian; but then \( (E(H), E - E(H)) \) is an even circuit partition of \( G \), which is impossible. Thus \( H \) is not a circuit, and so has maximum valency 3. Define \( p(e) = 2 \) (\( e \in F \)), and \( p(e) = 1 \) (\( e \in E(H) - F \)). By (2.4), there is a set \( \mathcal{C} \) of circuits using each edge \( e \) \( p(e) \) times, and by (2.5) there is a function \( t: F \to \mathcal{C} \) such that \( f \in t(f) \) for \( f \in F \), and

\[
|\{ f \in F : t(f) = C \}| + |C|
\]

is even for \( C \in \mathcal{C} \). For each \( C \in \mathcal{C} \), construct a circuit \( g(C) \) of \( G \) containing the following edges:

- if \( e \in C - F \), or \( e \in C \cap F \) and \( t(e) \neq C \) then \( e \in g(C) \)
- if \( e \in C \cap F \) and \( t(e) = C \) then \( g(C) \) contains the two edges of \( G \) incident with \( v_e \).

Then \( g(C) \) is a circuit of \( G \), and is even, and \((g(C): C \in \mathcal{C})\) is an even circuit partition of \( G \), a contradiction. This completes the proof.

4. Remarks

Even circuits in planar graphs seem to be quite well behaved; for as well as (2.1) and our Theorem (3.1), there is the following.
(4.1) If $G$ is a planar 2-connected cubic graph, there is a set $\mathcal{C}$ of even circuits using each edge twice.

Proof. By the four-colour theorem, $G$ has a 3-edge-colouring. Take such a colouring, and let $\mathcal{C}$ contain all two-coloured circuits.

These three results suggest that there may be a common generalization, something like (2.3) for even circuits. Indeed, it was the search for a common generalization of (2.1) and (4.1) that led me to (3.1) in the first place. However, it seems difficult even to find a reasonable conjecture.

Incidentally, Szekeres [4] claimed that

\begin{equation}
(4.2) \text{A cubic graph is } 3\text{-edge-colourable if and only if there is a set of even circuits using each edge twice.}
\end{equation}

But there is a mistake in Szekeres' proof, and regrettably, the result is false; the graph of Fig. 1, due to Sousselier (see [2]) is a counterexample. It is not 3-edge-colourable, but the six circuits consisting of the edges with labels $1, \ldots, 6$, respectively, are even and use each edge twice.

Finally, we have seen that the "planar" hypothesis in (3.1) cannot be omitted. However, one might hope that if (3.1) was expressed in terms of the geometric dual of $G$ the "planar" hypothesis would then be redundant. But that is not so. The graph of Fig. 2 is a counterexample, since it is bipartite, 2-connected, and has an even number of edges, and yet has no 'even cocircuit partition." (A cocircuit is a minimal non-empty cut, and for a planar graph corresponds to a circuit of the geometric dual.)

References

