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Procedia Engineering 53 (2013) 607 – 615

Procedia Engineering

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Malaysian Technical Universities Conference on Engineering & Technology 2012, MUCET 2012

Part 2 – Mechanical And Manufacturing Engineering

CONWIP Based Control of a Semiconductor End of Line Assembly

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Abstract

Advancement of technology and trends in globalization has resulted in higher customer demands and expectations. Manufacturers now offer mass customization to stay competitive. In the semiconductor industry, where product mix and volume are high, production is further complicated by the different process routes and processing times for different product families. Coupled with rapid changeovers of products, it is essential to keep the work in process (WIP) low in order to reduce the inventory level on the shop floor. CONWIP is a production control strategy applicable in many manufacturing environment, that uses cards to control WIP level. In this paper, discrete event simulation models for processes at the End of Line (EOL) assembly in a semiconductor manufacturing company were developed. Experiments were conducted using these models to compare the current system with the single loop and multi loop CONWIP control mechanisms. Performance parameters of throughput, cycle time and WIP level were compared in all experiments. The result, firstly, shows that, generally, CONWIP production control is more effective to reduce WIP level compared to the current system. The reduction in WIP is accompanied by corresponding improvements of cycle times. Secondly, the multi-loop system performs better than the single loop system with higher cycle time reduction. Multi loop control is also more robust and provides a better control mechanism compared to the single loop system.

Selection and peer-review under responsibility of the Research Management & Innovation Centre, Universiti Malaysia Perlis

Keywords: CONWIP, Production Control, Semiconductor, End of Line, Simulation.

1. Introduction

The semiconductor industry is characterized by high product mix and high production volume. The processes in this industry are typically complicated and time consuming [1,2]. At the End of Line (EOL) of semiconductor manufacturing, the assembly process is further complicated by the different, routes and processing times for the numerous product families. The accumulations of WIP and control policies are often a challenge to the semiconductor industry over the years. To be competitive, WIP in EOL assembly needs to be effectively controlled in order to minimize inventory and reduce cycle time.

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Selection and peer-review under responsibility of the Research Management & Innovation Centre, Universiti Malaysia Perlis
doi:10.1016/j.proeng.2013.02.078

Production control systems are typically categorized as the push and pull systems. Example of push system includes MRP, MRP II, whereas examples of the push system include kanban and CONWIP. Some advantages of implementing pull over push system include the reduction of cycle time variability and the flexibility to make any engineering and design changes. Comparing between the two main pull systems, kanban maintain a tighter WIP control through individual cards at each workstation whereas CONWIP is generally easier to implement and regulate as only one set of production cards are used to manage WIP.

This study was conducted in a case company, which is a local semiconductor manufacturer. Data collection was focused on the EOL assembly that involved six main processes namely, moulding, curing, tie bar cut, manual inspection, trim and form, and test, as shown in the Fig 1. One major product family is considered for the purpose of this study. Currently, the production control employed is by using the conventional push approach and the company wishes to improve cycle time and reduce high WIP at the EOL assembly.

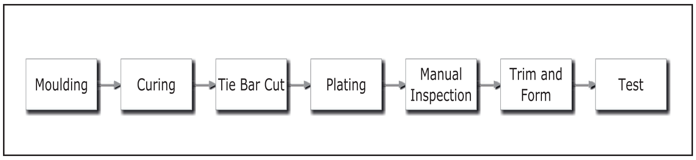


Fig. 1. EOL assembly process flow.

The remainder of this paper is organized as follows. In Section 2, the relevant literature review will be discussed. In section 3, the details for model development, verification and validation are presented. In section 4, the result and discussion of the experiments are provided. Finally in Section 5, the conclusion and future research opportunities will be discussed.

2. Literature review

Industries have been consistently putting in effort to reduce WIP as it incurs the inventory cost. These efforts can be seen from the numerous past researches on WIP issues. For instances, Bertrand and Ooijen [3] have conducted research on work release order to study the influence on the throughput, throughput time and WIP. In this study, they aim to reduce the sum of the cost for these three factors. The job shop is examined by manipulating the WIP as compared to the total cost under instant release of arrival orders. From the experiment, the results indicated that cost reduction is considerable for small shops and for high ratios of WIP cost to lead time costs.

Accumulation of the WIP is a kind of waste for company especially for the semiconductor industry. Product cycles of semiconductor are short as the changeovers of the product are very fast. Qiu [4] researched the semiconductor company by using simulation to assess the WIP control system. The WIP control algorithms were tested by applying real time operation, where WIP levels, and machine utilization were evaluated in this study.

Sharma and Agrawal [5], employed AHP-algorithm in the control policy under different demand situation for the manufacturing system. The policy that they studied included, KANBAN, CONWIP and hybrid versions. Different demand patterns were studied by applying different control policies in order to obtain the behavior of each performance level. Other than this, Lin et al. [6] focused on finding an optimal WIP value of wafer fabrication processes by developing an algorithm integrating an artificial neural network (ANN) and the sequential quadratic programming (SQP) method. In this research paper, these methods offered an effective and systematic way to identify an optimal WIP level. Lin and Lee used queuing network-based algorithm to determine total standard of WIP and used a fixed WIP to implement the release control policy. The fixed controls WIP achieved the targeted throughput rate and the cycle times were kept relatively low. Isakow and Golany. [7], Yang et al. [8], and Li et al. [9] presented the study on constant work in process (CONWIP). The study proposed a model with the closed loop queue network and an approximate method was proposed in order to evaluate the system's performance. As the results were fairly precise, the genetic algorithm was designed to the proposed model to obtain the optimal results. In the review paper of Framinan et al. [10], a comprehensive and extensive of application CONWIP at the shop floor to control the WIP were discussed. Ip et al. [11] compared single loop and multi loop of CONWIP control for the lamp assembly production line which produce different kinds of products with discrete distribution processing time and demand. With respect to total cost and service level, a model was constructed with a novel rule-based genetic algorithm approach to determine the optimum parameter setting for multi loop CONWIP system. Results of the experiment showed that the single loop have better efficiency control than the multi loop system whereby the total cost can be greatly decrease and WIP with zero shortage probability.

For developing and executing complex WIP models, the simulation approach has been the favored option for many researchers. Leitch [12] used the simulation approach to study the effect of stochastically, capacity, lead time on WIP and throughput. In his paper, it was found that these factors led to the cost drivers effect on WIP and throughput. Mirbirjandian and Wong [13] compared Kanban, CONWIP and Base-Stock in two kinds of essentially different production lines by using simulation study. In the simulation results, CONWIP showed the fewest average WIP and average WIP holding time as compared to the other systems. While for Morrice et al. [14] simulation analysis was used to count and predict the effect of internal on-time delivery, inventory and WIP change on the customer order fulfillment service level. In this way suitable control levels at various stages in a semiconductor supply chain, based on inventory and service level metrics can be identified.

From past researches, it was observed that most work was done for the wafer fabrication, and backend of the manufacturing line. There is not much work done to study WIP control at EOL Assembly of the semiconductor industry. In this paper, the analysis and study on the CONWIP based system in the EOL assembly is presented. The objective of this research is to identify the suitable level of WIP float in the EOL in order to decrease the holding of WIP and improve the cycle time. As the system to be studied is too complicated for analytical methods, models were developed an analyzed using the WITNESS simulation software.

3. Model Development, verification & validation

In the semiconductor industry, the products are high mix with each product family undergo different process routes. These product route, process times, machines are included in the simulation models. Setup time, breakdown time and conversion time for each of the machine are also defined. The distribution patterns for the unit per hour (UPH) of each machine for different products and material handling times are analyzed using the Minitab statistical software.

The input data for the base model were collected from the shop floor of the company. The base model was verified using the process flow diagram and by personnel in the shop floor. This is followed by the validation process. Operational validity is important to ensure the model's output behavior has the accuracy required for the models intended purpose [15].The throughput from a total of 10 replications runs were collected and tested with the Minitab statistical software to validate the model. The duration for each replication run is for a period of nine months. The warm up period is estimated to be six months.

Once the base model has been verified and validated, the experiments to test the CONWIP control policy were developed. Some assumptions made for the experimentations were that operators and material transportations were not included in the models and that all machines were available for all products.

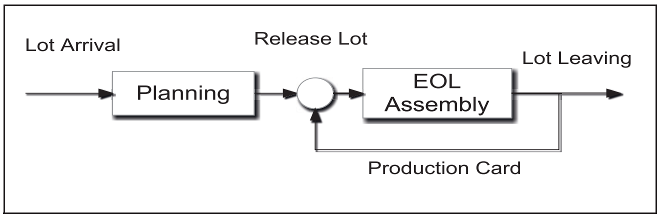


Fig. 2. CONWIP control system.

In Fig 2, the movements of the lots in the CONWIP system are shown. When a job arrives at the planning department, decision will be made as to whether to release the job for production. In this CONWIP system, the numbers of lots to be released to the EOL assembly is limited to the number of production cards available at the beginning of EOL assembly.

The logic flow diagram for the CONWIP system is shown in Fig 3. Based on the targeted throughput rate the numbers of production card are determined by the simulation model. The number of cards determines the WIP level for the assembly line. The study consists of two experimental models i.e. single loop and multi-loop CONWIP models.

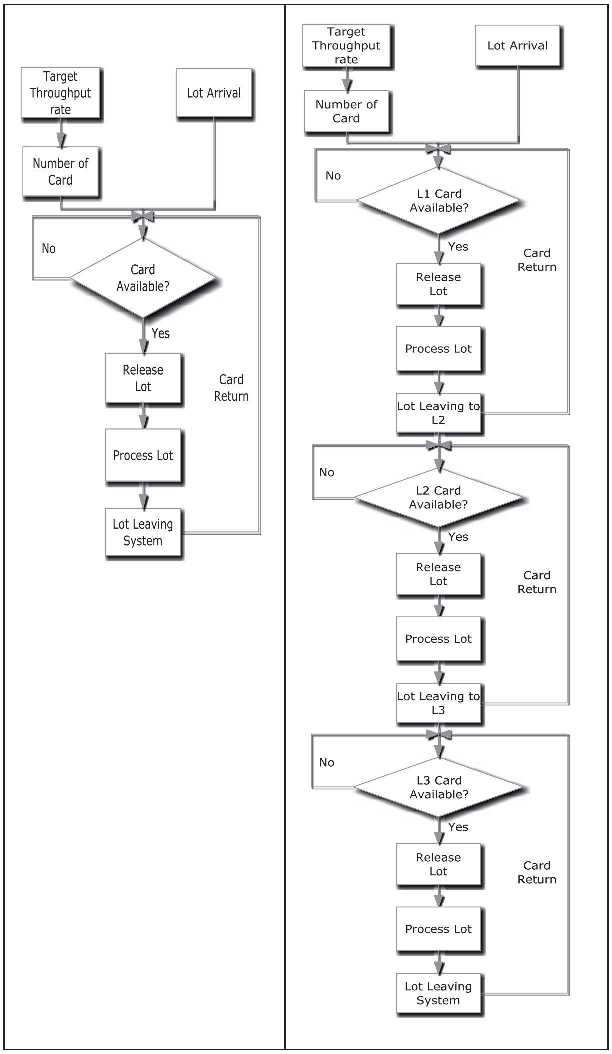


Fig. 3. Framework of CONWIP flow 3(a) single loop CONWIP 3(b) multi loop CONWIP

For Fig 3(a) shows the single loop control which a uses single universal card in the system. Every machine or buffer shares and uses the same card. So when a lot arrive, the system will check if there are any cards available to authorize the lot to enter into the system. Each production card can only authorized one lot to be released into the system. The card is released back to the front the EOL assembly once the lot is withdrawn from the system. If there a queue in the buffer, the precedence will give to the same product family first.

Fig 3 (b) illustrates the multi loop CONWIP system. In this example there are 3 loops with 3 different production cards. Each card only can only be released back to the beginning of the respective loop once the lot leaves that specific loop.

It shares the same concept as the single loop system but with each loop utilizing its own set of cards which cannot be used at other loops. For both the single and multi-loop system, there are a limited numbers of cards circulating to control the amount of WIP allowable in the system at any one time.

The objective for single loop experiment is to determine the appropriate CONWIP level for a targeted throughput rate. A CONWIP level ranging from 400 to 650 were analyzed.

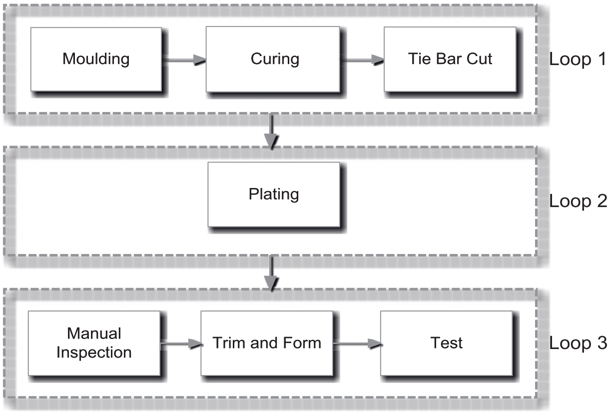


Fig. 4. Processes of multi loop in CONWIP system.

While for the multi loop CONWIP experiment, three different loops are developed in the EOL assembly. The first loop includes the Moulding, Curing and Tie Bar Cut processes. While Loop 2 includes process by the curing process only and the last loop will includes the Manual Inspection, Trim & Form and Test processes. Figure 4 illustrates the processes in each loop.

The WIP in each loops are controlled at different levels and adjusted to find the best combination to meet the targeted throughput. For loop 1, the WIP are controlled from 200 to 220 lots, and the loop 2 controlled from 220 to 220 lots, and the last loop from 50 to 70 lots. The throughput rates are maintained at around 193 lots based on the production data. The screen capture of the developed base model in Witness simulation software is shown in fig 5. The results of the experiments are discussed in the next section.

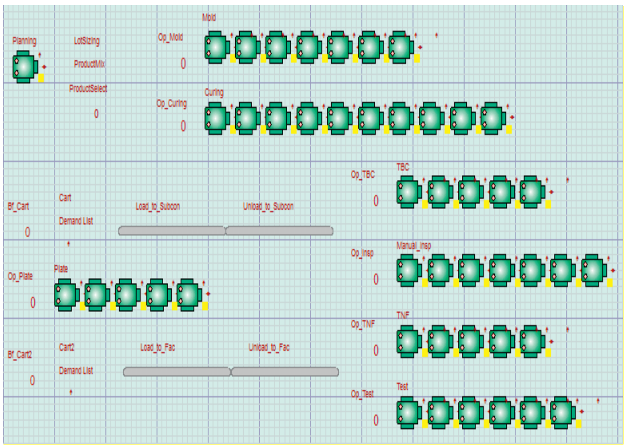


Fig. 5. Witness simulation representation of the base model.

4. Result And Discussion.

For both experiments, the models were executed for ten replications runs. For each experiment, the average reading will be taken from each of the ten replication run. Different level of CONWIP will result in different output performance. The performance criteria for both experiments are: Work In Process (WIP), Cycle Time (CT), and Throughput (TH).

From the Table 1, single loop CONWIP level is represented by the number of production cards (ranged between 400 to 650). In the base model, average WIP was 575 lots, with CT of 3984 minutes and TH of 193 lots. This throughput rate is set as the target for the experimental models.

From the single loop CONWIP experiment, the WIP and CT increased with the numbers of production cards (please refer to Table 1 and Fig 6). The result is consistent with Little's law. However at the WIP of 440 levels, the throughput target is achieved. The CT is 3265.621, an 18.1% improvement from the base model. The improvement of WIP is 23% lower compared to the base model.

Table 1: single loop conwip results

No. of Production Cards	TH	CT	WIP
400	192.2489	2981.763	400
410	192.5044	3051.663	410
420	192.7437	3121.006	420
430	192.9148	3192.657	430
440	193.0148	3264.621	440
450	193.1396	3336.135	450
500	193.2826	3695.78	500
550	193.3004	3922.818	545
600	193.3074	3976.837	568.7
650	193.3004	3983.964	574.9

(a)

(b)

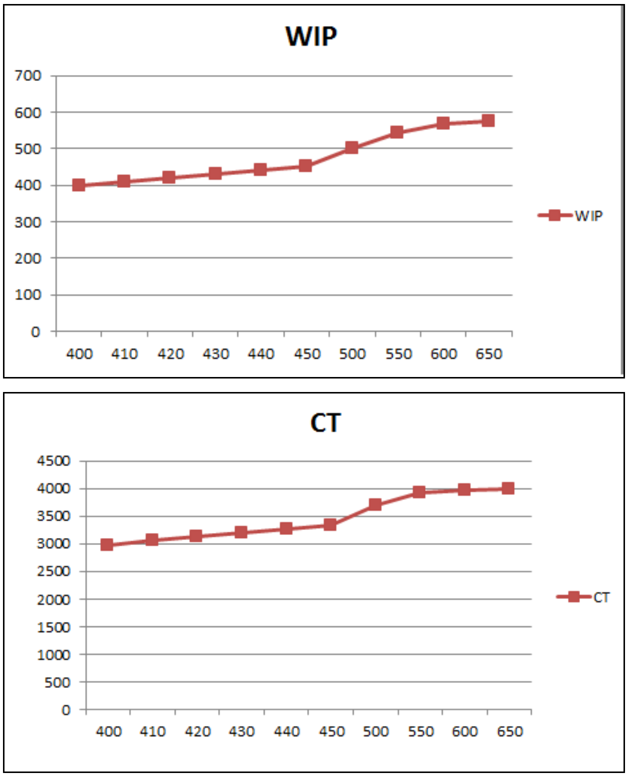


Figure 6: Throughput and cycle time versus WIP. (a) Throughput versus WIP level in the CONWIP system. (b) Cycle time versus WIP level in the CONWIP system.

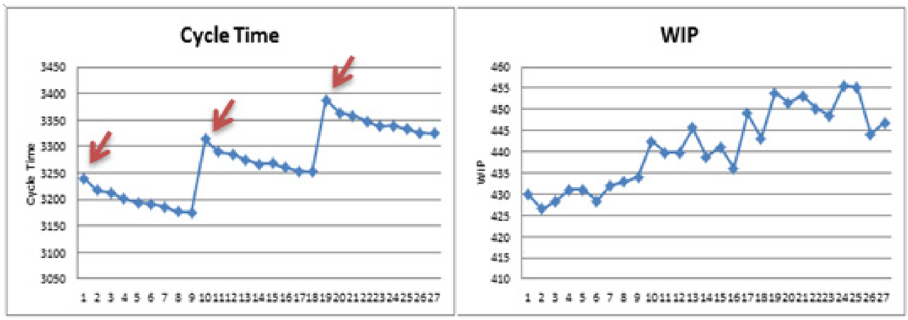
Table 2 shows the result from the multi loop CONWIP model. Production Card in first 3 columns of table 2 represents the initial setting of WIP level for each loop while the average number of cards used is shown in columns 4-

6. For instances, the first 3 columns at the first row in table 2, the number of cards were set at 200, 200 and 50 for loops, L1, L2, L3 respectively.

The average number of cards used is actually 200, 190, and 39 respectively. Hence when L2 achieved WIP level 190, the remaining 10 cards are not utilized.

Table 2 Multi loop conwip result

Production Card (initial setting)			**Average Number of Cards Used (output from model)**			**Output Parameters**		
L1	**L2**	**L3**	**L1**	**L2**	**L3**	**CT**	**WIP**	**OUT-PUT**
200	200	50	200	190	39	3240.46	430	190.75
200	200	60	200	189	38	3216.84	427	192.08
200	200	70	200	189	40	3212.93	428	192.29
200	210	50	200	192	40	3200.84	431	192.68
200	210	60	200	190	42	3194.15	431	192.78
200	210	70	200	190	38	3190.96	429	192.8
200	220	50	200	190	42	3185.59	432	192.84
200	220	60	197	192	44	3177.18	433	192.83
200	220	70	196	194	44	3175.97	434	192.84
210	200	50	210	190	42	3313.65	442	191.13
210	200	60	210	194	36	3290.16	440	192.4
210	200	70	210	190	40	3286.09	440	192.65
210	210	50	210	193	43	3274.31	446	192.9
210	210	60	210	188	40	3266.71	439	192.94
210	210	70	210	186	45	3267.33	441	192.84
210	220	50	210	182	45	3260.3	436	192.99
210	220	60	210	198	41	3254.3	449	193.04
210	220	70	210	191	42	3251.11	443	193
220	200	50	220	194	40	3387.23	454	191.36
220	200	60	219	198	35	3364.29	452	192.6
220	200	70	220	192	41	3359.1	453	192.79
220	210	50	220	187	43	3347.71	450	192.95
220	210	60	220	189	39	3337.57	449	193.04
220	210	70	220	192	44	3339.47	456	193
220	220	50	220	191	44	3331.82	455	193.13
220	220	60	216	184	44	3325.52	444	193.07
220	220	70	212	189	46	3324.24	447	193.09



(a) (b)

Figure 7: Throughput and cycle time versus WIP. (a) Throughput versus WIP level in the CONWIP system. (b) Cycle time versus WIP level in the CONWIP system.

The graph pattern for CT and WIP for multi loop CONWIP is shown in fig 7. For the CT graph, a series of peaks were observed for each setting of loop 1 when the WIP level of loop 3 is at minimum setting point (refer to labels in Table 2 and corresponding points in Fig 7). The values of peaks point in the fig 7 are highlighted in Table 2. This phenomenon occurs when there are queue in front of the loop 1 and loop 3 are limited to lesser WIP level to process the lots. These reasons caused to the waiting times of the part resulting in the increased cycle time. For the multi-loop experiment, the results show that at combination of 210, 220, 70 at loop 1, 2, 3 respectively, the CONWIP achieved the targeted throughput at CT of 3251.111. At this CONWIP level the CT is better than the CT of the base model (improvement of 18.4%). The improvement of WIP is 23% compared to the base model. For both the experiments, the results show the increasing upward trend of WIP and CT with the increase of production cards. As more cards are allowed in circulation the buffer size will become lager resulting in longer cycle times.For a fixed throughput of 193 lots, we compared the best average cycle time readings for the single loop (3264.621 min) and the multi loop (3251.111 mins.). Results show that the multi loop CONWIP performed better with a slightly lower CT (by 13.5 minutes) when compared to the best result for single loop system.

5. Conclusion and Recommendation

This study focused on the process in the EOL for a semiconductor company. As the manufacturing process is complex and involved a high mix of products, discrete-event simulation models using the WITNESS software were developed to evaluate the performance of the single loop and multi loop CONWIP systems. From the simulation results, both CONWIP systems outperform the existing system, by effectively controlling the WIP level and reducing the cycle time at the current throughput level. However the multi loop system performs better to reduce the CT as compared to the single loop system. The multi loop system is also more robust and easier to implement and control in the production line as compared to the single loop CONWIP system. In a multi loop system, cards are returned faster and the starvations due to bottleneck loops are minimized. As recommendations for future study, the multi loop CONWIP systems can be further subdivided for bottleneck processes or a hybrid control system can be embedded for better control of the production cards.

Acknowledgments

The authors wish to acknowledge that this project was supported by UTeM under grant number PJP/2011/FKP/(22B) S00922.

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