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The Design and Realization for a Multiplex Time Sequence Controller

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Abstract

In order to meet the demand of activating several devices at different moments, a multiplex time sequence controller is developed in this paper. When the controller receives the trigger signal for starting, the time sequential control circuit module, consisting of the microcontroller and the FPGA, it can generate a delay trigging signal according to the preset delay value, which will activate the testing device after being driven. The delay value is import by the computer or the dial on the panel. The real firing results show that the time sequence controller can realize the delay of 20-channel independently, one of which is able to be adjustable within 0～10s, the maximum amplitude of output delay trigging signal is 12V, the width of the signal is 5ms and the error of the delay time is less than 2μs. The multiplex time sequence controller can satisfy the requirements of technical specifications of testing system in conventional shooting range, and it can meet the demand of activating several testing devices operating at different moments.

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Keywords: time-sequence control; delay circuit; multi-computer communication

During a test of external trajectory of the weaponry, several (n set of) testing devices are arranged along the trajectory, when a projectile goes through a predetermined position, the testing devices are activated in sequence to measure the performance parameter of the position. Similarly, for a explosive test of warhead, several testing devices shall be provided in the dispersion range of fragments, when a fragment goes through a predetermined position, the testing devices are activated to measure the performance parameters of the position, in general, the number of testing devices is 10 [1,2]. However, the controller had the features of complex internal circuits, large size, narrow range of delay and poor expandability, besides, some researcher developed a multiplex time sequence controller based on CPLD,

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but the controller failed to carry out multiplex delayed channels in a piece of CPLD due to shortage of logic source hereof [3-5]. This paper introduces a 20-channel time sequence controller to solve the foregoing problems, which developed by means of microcontroller together with FPGA chip, wide range of delay and strong capacity of resisting disturbance.

1. Composition and principle of the system

The time sequence controller is composed of a host microcontroller control circuit, four pieces of time sequence control circuit module, the I/O signal isolating circuit and the drive circuit, as shown in Fig.1. The host microcontroller controls the working condition of the complete instrument, receives delayed times and control command transmitted from the master control computer and sends them to corresponding time sequence control circuit modules, which directly read the delayed times and demonstrate them. In order to realize the module design and expandability of the circuit, the optimization design is provided for the time sequence control circuit, and the 5 delayed channels, as a whole, is implemented in one module of time sequence control circuit. The drive circuit will drive the instantaneous delayed trigger signal after the signal is formed to impulse signal with the width of 5ms through mono-stable trigger and output various trigger signal according to the requirements of users.

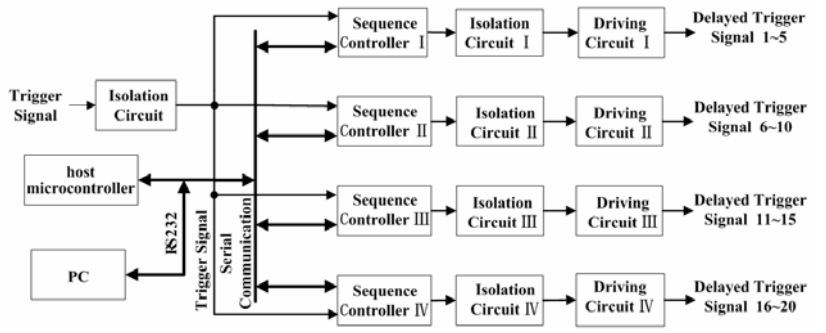

Fig.1 The block diagram of time-sequence controller

2. Design of time sequence control circuit module

2.1 Composition and working principle

The time sequence control circuit module mainly consists of the microcontroller, the FPGA, the level change-over circuit, and the time introducer and indicating circuit. The salve microcontroller controls the working flow of the complete time sequence control circuit and the working time sequence of delayed control logics and transmits the delayed times to data latches of channels of the FPGA through data bus under the control of address command. The internal logics of the FPGA is composed of 5-channel time sequence control logics and address decoding logics. The address decoding logic is comprised of the 74373 and the corresponding decoder and controls the working time sequence of internal logics of the FPGA. The delayed values from data latches of channels are transmitted to input end of corresponding counters under the control of the address command. The level change-over circuit changes the level of data transmitted between the microcontroller and the FPGA. The time introducer and indicating unit carries out the input and indication of the 5-channel delayed times. In order to simplify the system, a toggle switch with five positions shall be provided together with one circuit of time introducer and one circuit of time indicator to carry out the input and indication of the 5-channel delayed times in sequence.

2.2 The realization of counting logic

The counting sequential logic is the core of the whole sequential control logic, and consists of the counting latch logic, the 32-bit preset counter and input logic of trigger signal for outputting the delayed signal, the counting sequential logic schematic diagram is shown in Fig.2, where U1、U2、U3 and U4 are all 8-bit latch, constituting a 32-bit data latch logic, which changes the data between microcontroller and the 32-bit counter and transmits the delayed times to input end of counter under the control of address command. U5 is a 32-bit preset counter generated from the LPM_COUNTER, and can output delayed signal. The trigger signal input the combinational logic circuit, and then it can produce a counting enable signal. When a trigger signal arrives, the U5 starts counting down to 0, the COUT end outputs the delayed impulse OUT0, and the front edge of the signal means the output moment [6]. A simulation figure of the counting sequential logic is shown in Fig.3, and the preset delayed value is 55, the corresponding delayed time is 5.5μs, the time interval between the rising edge of trigger signal after simulation and the rising edge of the delayed signal is 5.5μs, which is in conformity with the preset value [7, 8].

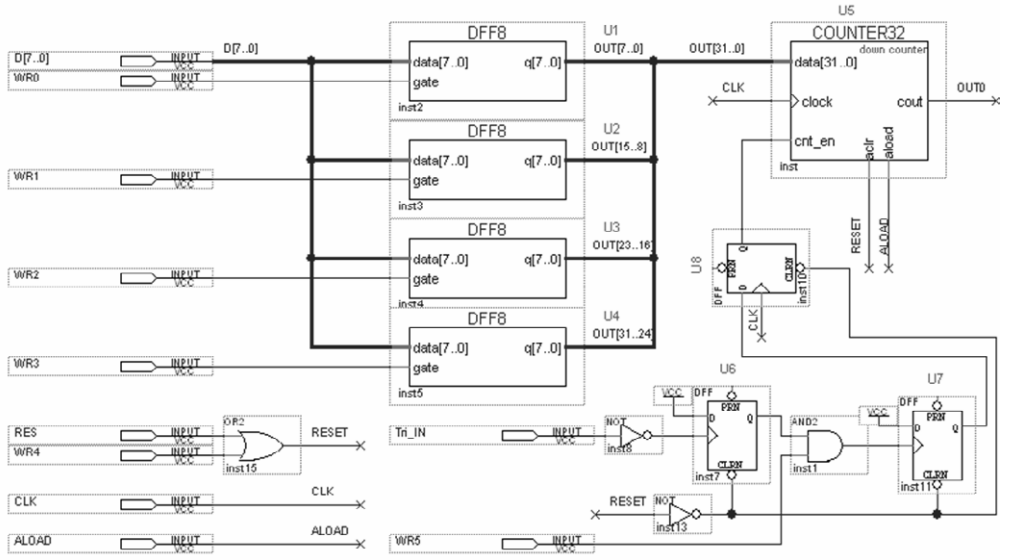

Fig.2 The principle of counting temporal logic

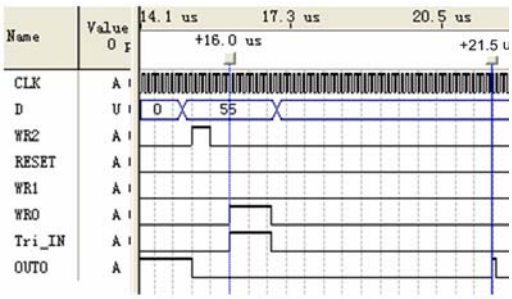

Fig.3 Simulation figure of counting temporal logic

3. Workflow of the host and the salve microcontroller

The microcontroller program is divided into the host and the salve microcontroller programs. The host microcontroller scans the condition of panel in the mode of off-line and controls the working condition of

the whole time sequence controller, and is controlled by host controlling computer in the mode of on-line to read the delayed times of 20-channal and transits them to the four slave microcontrollers in sequence according to the preset time sequence. The host microcontroller initializes and then judges the mode of the time sequence controller, whether it is in the mode of on-line or not. If it is on line, the host microcontroller initializes in serial port and receives the 20-channal delayed times transited from PC and then sends them to each salve microcontroller under the control of address command. However, if it is in the mode of off-line, the host microcontroller scans the condition of panel and sends control command to the four salve microcontrollers, showing their corresponding working conditions.

The salve microcontroller program can control the working sequence of the logic circuit, including the acquisition of delayed times from the data bus and sends them to the data input end of counter involved in the logic circuit. Firstly, the slave microcontroller initializes and receives the control command from the host microcontroller and then determines whether it receives the delayed data from the host microcontroller on the basis of the control command, if the delayed data is required to be received, it will judge whether the address from the mater microcontroller is the local address or not, if it is, the salve microcontroller will receive 5-channel delayed times, if not, the salve microcontroller will reset to receive control command from the host microcontroller again. If the salve microcontroller does not receive the delayed data from the host microcontroller, it will read a delayed data input from corresponding dial switch. After the salve microcontroller acquired the delayed times, it applies the delayed times to the FPGA to waiting for the interruption instructions of delayed termination, if the interruption instructions are in force, the salve microcontroller will reset the FPGA and itself and backs to the initialization.

4. Test results and analysis

The designed time sequence controller is verified by tests in the lab, and the input trigger signals are produced in the mode of manual triggering in the process of the test, and the interval time between the input trigger signal and the delay trigger signal is measured by means of a XG-2002 electronic chronometer to check and verify whether the delayed time is equal to the input delayed time in advance or not. The clock frequency of the chronometer is 10MHz. Only one time sequence controlling circuit module is required to be tested, and the same testing method can be applied to other circuits modules, please refer to Table 1 for further test data, where the theoretical values are the input delayed time, and the measured values are the actual delayed time measured by the chronometer. The working condition of the time sequence controller can be determined by comparison of the difference between the theoretical values and measured values.

Table 1 The test data of time-sequence controller

No.	Delayed Channel	Theoretical Values (μs)	Measurement Values (μs)	Deviation Values (μs)
1	1	50.0	50.2	0.2
2	2	100.0	100.3	0.3
3	3	500.0	500.1	0.1
4	4	1000.0	999.7	0.3
5	5	25000.0	24999.9	0.1
6	1	1000.0	999.6	0.4
7	2	2000.0	1999.7	0.3
8	3	5000.0	4999.7	0.3
9	4	50000.0	50000.1	0.1
10	5	1000000.0	1000001.5	1.5

By analyzing the data shown in Table 1, it is clear that the theoretical values are similar to the measured values, and the deviation of output time of the instantaneous delayed trigging signal is less than

2μs, which is in conformity with the technical specification, namely, the delayed time of the instrument in service is not more than 5μs. The errors are attributable to the items below:

(1) The delay available in the transmission line and the circuit for the input trigging signal;

(2) The delay available in circuit, in particular, the drive circuit, for the instantaneous delayed trigging signal;

(3) The delay available in transmission line for the instantaneous delayed trigging signal;

(4) The influence caused by the delay generated by the inconsistency of rising edge of the trigging signal.

5. Conclusion

(1) The instrument meets the requirements of technical specifications of testing system.

(2) The relevant shielding measures are taken to satisfy the demand of the EMC, and accommodate the instrument to ambient temperature by means of sealed case complete with control circuit of constant temperature.

(3) The instrument operates stably and reliably, and the time sequence controller can provide services for conventional shooting range where needs several testing devices operating at different moments.

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