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Characterisation of CdS/CdTe Heterojunction Solar Cells by Current-Voltage Measurements at Various Temperatures under Illumination

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Abstract

Heterojunction CdS/CdTe thin film solar cells were fabricated with a superstrate structure consisting of the successive layers: soda lime glass/ITO/CdS/CdTe/back contact. ZnTe:Cu films were deposited on the back surface of the CdTe layer presenting as ohmic back contact. The substrate was soda lime glass coated with ITO films by rf magnetron sputtering serving as the transparent front contact. A thin layer of CdS with thickness about 80 nm was applied by chemical bath deposition. Close-spaced sublimation of the CdTe films was accomplished by placing a CdTe source in a close proximity (6 mm) to the substrate in vacuum chamber with low pressure about 3×10^{-2} mbar. The source was heated to 550 ^{o}C and the substrate to 450 ^{o}C. This arrangement causes Cd and Te to sublime from source and diffuse to the substrate. The fabricated cells were investigated using current-voltage (I-V) in the temperature range 20-300 K under a standard AM1.5 illumination in order to define the transport mechanism in the heterojunction. Tunnelling enhanced interface recombination has been found to dominate carrier transport mechanism in the junction at all investigated temperatures.

Keywords: CdS/CdTe solar cells; I-V measurements; tunnelling enhanced recombination

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1. Introduction

Cadmium telluride (CdTe) is considered as a promising material for several applications like photovoltaic cells, high performance electro-optic modulators and photorefractive devices. CdTe has a direct bandgap of 1.5 eV at room temperature, which is an ideal match to the solar spectrum for photovoltaic absorber. The function of cadmium sulphide (CdS) is to allow energetic short-wavelength photons to pass for the incidence at the hetero-interface with minimum absorption loss. The high optical band gap of CdS (2.4 eV) assists in this function. The other use of CdS is to provide a junction field for separation of photogenerated minority carriers before recombination. CdS/CdTe based solar cell have a theoretical photovoltaic conversion efficiency higher than 29% [1]. CdS/CdTe solar cells are p-n hetero-junction devices in which a thin film of CdS forms the n-type window layer. The structure is of superstrate type in that the transparent conductor and window layer are first deposited onto a transparent substrate such as glass. The absorber in this case CdTe layer is deposited over the window layer. In this work, CdS/CdTe heterojunction solar cells were prepared from CdS deposited by chemical bath deposition technique, and CdTe deposited by CSS, both cost-effective scalable techniques. The solar cell is of the front-wall configuration, i.e. films of CdS, *p*-type CdTe, and an ohmic contact are subsequently deposited onto a transparent conducting oxide-coated soda-lime glass. Bayhan and Kavasoglu [2] studied dark I-V characteristics of CdS/CdTe solar cells at low temperature. They proposed that the I-V data can be analysed by tunnelling enhanced bulk and interface recombination. In this work, we study I-V charac-teristics of typical CdS/CdTe solar cells under standard AM1.5 illumination at various temperatures. The carrier transport mechanism in the heterojunction can be well explained by tunnelling enhanced interface recombination.

2. Solar cell fabrication

CdTe/CdS/ITO/ slide glass solar cells were fabricated in form of thin films. CdS thin film layer was deposited onto ITO thin film layer sputtered on slide glass by chemical bath deposition (CBD) using 0.01M $CdSO_4$, 0.05 M $SC(NH_2)_2$ and 1.5 M NH_3 as the starting materials in deionised water with total volume 150 ml at constant temperature 80 °C and the pH was about 11.4. Then CdTe thin film layer was coated by close-spaced sublimation (CSS) technique. The CSS growth assembly contains two graphite with the precursor and substrate sandwiched separated by 6 mm space under substrate temperature 450 °C and the precursor temperature 550 °C. $CdCl_2$-treatment was carried out at 400 °C for 30 min. Finally, ZnTe:Cu films were deposited on the back surface of the CdTe layer presenting as ohmic back contact. The structural properties of thin films were determined by X-ray diffraction using a Bruker D8 Advance with CuK_α ($\lambda = 1.5418$ Å) radiation. Grain size and surface morphology were revealed in accordance to scanning electron microscopy (SEM). The I-V characteristic curve was measured under a standard AM1.5 illumination at various temperatures by using a computer interfaced Keithley 236 current/voltage source.

3. Tunnelling enhanced recombination model

If current transport is dominated by any of the thermally activated like injection, interface or space charge recombination, the forward current density of a heterojunction is generally determined by

$$J = J_0 \, exp(qV/nkT) = J_{00} \, exp(-E_a/nkT) \, exp(qV/nkT) \qquad (1)$$

where V is the applied voltage, n is the diode ideality factor, J_0 is the reverse saturation current density, k is the Boltzmann constant and J_{00} is a pre-factor which depends on the transport mechanism. For tunnelling dominated current transport, the J-V relationship is generally expressed as

$$J = J_0(T)\ exp(AV) \tag{2}$$

The slope of the lnJ-V plot is essentially temperature independent and called as the voltage factor A. At constant voltage, $\ln J_0$ is more nearly a linear function of temperature T than of T^{-1}. Since thermally activated holes make step wise tunnelling into interface states, J_0 is slightly thermally activated. A relatively new approach explaining the tunnelling enhancement of recombination via deep centres in the space charge region or at heterojunction interface provides analytical expression for the forward current transport in CIGS based solar cells [3, 4]. This model namely tunnelling enhanced recombination in the bulk of the absorber or at the buffer-interface, assumes that the forward current of the heterojunction is also determined by Eq. (1). The value of the activation energy E_a can be deduced from experimental data by reorganising Eq. (1) as

$$nln(J_0) = -E_a/kT + nln(J_{00}) \tag{3}$$

Thus, the activation energy E_a of the process can be calculated from the slope of a linear plot of $nln(J_0)$ versus 1/T. According to this model, E_a represents the interface barrier height for holes in the case of interface recombination. Tunnelling of holes from the bulk of the absorber into the interface states and subsequent recombination with electrons available in the window layer leads the temperature dependence of the diode ideality factor as

$$n = (E_{00}/kT)coth(E_{00}/kT)\ , \tag{4}$$

where E_{00} is the characteristic tunnelling energy measuring the amount of tunnelling contribution to the recombination process.

4. Results and discussion

Figure 1(a) shows SEM image of the surface of CBD-CdS film deposited on ITO substrate. Clusters of grains like cauliflower with various sizes are presented in the as-deposited CdS films and the average grain size is approximately less than 50 nm. Figure 1(b) shows SEM image of the surface of CSS-CdTe films deposited on CdS layer before $CdCl_2$-treatment. This SEM image shows large grain size, uniform coverage, non-porosity and well packed faceted grains. Figure 1(c) demonstrates the cross-section of CdS/CdTe solar cells after $CdCl_2$-treatment. The SEM image shows that the grain size of CdTe films is smaller than the one before $CdCl_2$-treatment.

Figure 2 reveals $\ln J_D$-V plot of CdS/CdTe heterojunction at various temperatures under illumination with forward bias voltage range from 0 to 0.8 V. J_D is the diode current density that is found by subtracting the light current from the measured total current [5]. Figure 3 shows $\ln J_D$-lnV plot of CdS/CdTe heterojunction at various temperatures under illumination with forward bias voltage. The slope of $\ln J_D$-V had to be carefully evaluated because it is important in identification of the current transport mechanism. At lower bias voltage (< 0.3 V at 300 K), current density J_D can be expressed by Eq. (1). The reverse saturation current density depends slightly on the temperature and the diode ideality factor values were found to be strongly on temperature and have values n higher than 2 (as shown in Table 1). According to large value of ideality factor n, these results may suggest that the tunnelling plays an important role in the current transport. For CdS/CdTe solar cells, tunnelling enhanced bulk and interface recombination has been recently found to dominate carrier transport under dark I-V measurements [2]. Linam *et al.* [5] investigated the light and voltage dependence of the junction transport of CdS/CdTe solar cells. It was found that a light dependent tunnelling mechanism dominates at low bias voltage. The tunnelling takes place through a defect state whose occupation is charged by light level. At higher bias

voltage the most important current transport mechanism is combination of generation/recombination and diffusion with generation/recombination being the dominant mechanism.
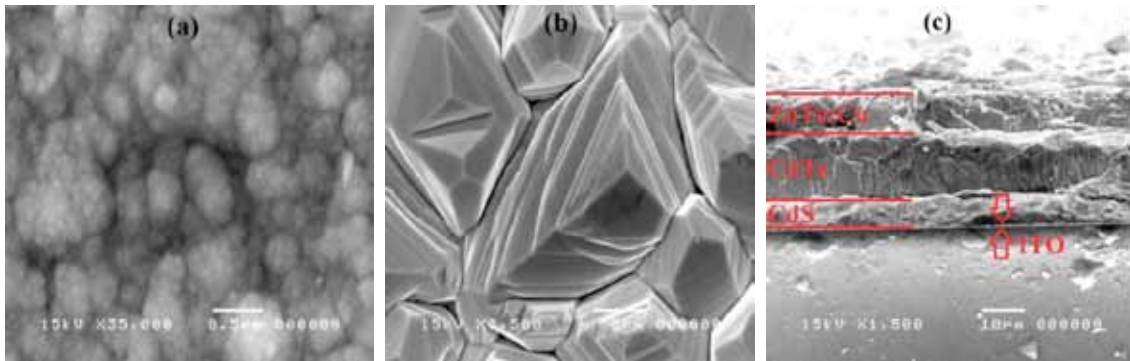

Fig. 1. SEM images of (a) CBD-CdS film surface; (b) surface image of CSS-CdTe films before CdCl$_2$-treatment; and (c) cross-section of CdS/CdTe solar cells after CdCl$_2$-treatment.
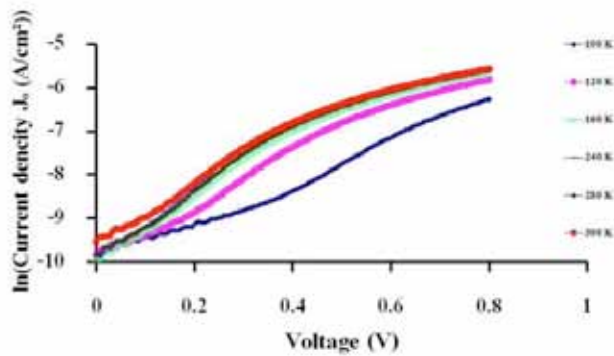

Fig. 2. LnI$_D$-V characteristic curves of CdS/CdTe solar cells made at various temperatures.
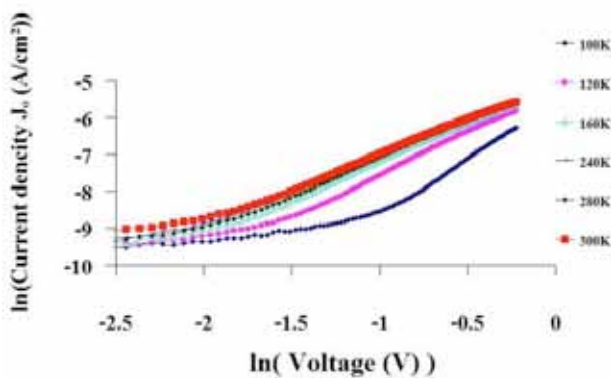

Fig. 3. LnI$_D$-lnV characteristic curves of CdS/CdTe solar cells made at various temperature.

The validity of the proposed recombination path is also checked through the temperature dependence of diode ideality factor. The variation given in Fig. 4 is found to fit very well on the theoretical expression given by Eq. (4) and the tunnelling energy is calculated as about 0.722 eV. This suggests that, in our cells, tunnelling taking place via interface states is strongly aided by light in the lower bias voltage.
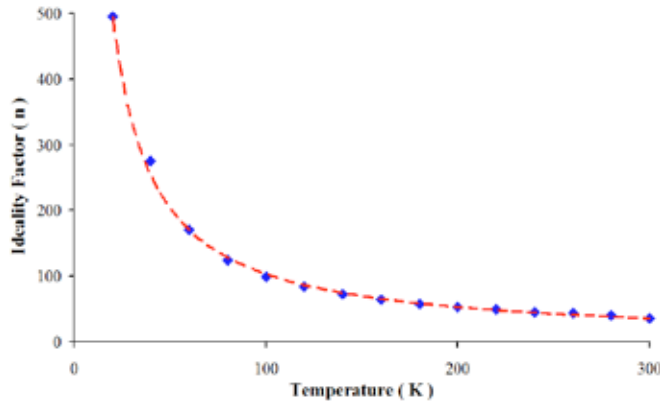

Fig. 4. Ideality factor (n) as a function of temperature (T) and fits to Eq. (4) of CdS/CdTe solar cells.

Table 1. Some parameters of current transports in CdS/CdTe solar cells at various temperatures.

Temperature (K)	J_0 (10^{-5} A/cm^2)	Ideality Factor (n) (Low Bias Voltage)	Exponent Value (m) (High Bias Voltage)
20	1.47	495	2.28
40	1.75	275	2.24
60	1.92	170	2.19
80	2.22	124	2.14
100	2.42	99	2.10
120	2.49	84	2.05
140	2.70	73	2.00
160	2.78	65	1.97
180	2.80	58	1.91
200	2.98	53	1.89
220	3.19	49	1.88
240	3.31	45	1.88
260	3.63	44	1.84
280	3.94	40	1.84
300	4.36	36	1.83

At higher bias voltage (more than 0.3V at 300 K), a straight-line relationship in Fig. 2 had not be obtained. This may be suggested that another mechanism such as space charge limited current (SCLC) can play a role in current transport. The current density of SCLC mechanism is proportional to applied voltage which can express as $J_D = V^m$ and lnJ_D-lnV plot should be a straight line having slope value m (as shown in Fig. 3). Summary of SCLC analysis in higher bias voltage was shown in Table 1. SCLC with the slope value m $\approx$ 2 had been described by Mott-Gurney's law as [6, 7]

$$J = \frac{9\varepsilon_r\varepsilon_0 N_V \mu V^2}{8d^3 N_t} \exp(-E_t/kT) \; ,$$ (5)

where ε_r is the relative dielectric constant, ε_0 is permittivity of vacuum, N_V is the effective density of states, N_t is the concentration of traps with activation energy E_t, d is the film thickness and μ is mobility.

This conduction type can have a pronounced effect on the electrical properties of semiconductor at room temperature and below, because they normally have a low density of free carriers and charge unbalance can be easily produced by an applied voltage [6]. The character and magnitude of space charge limited effects are determined largely by the presence of localised states which can trap and store charge equilibrium with the free charge. Single carrier injected currents are necessarily space charge limited and in a perfect trap-free insulator where all the injected carriers remain free and all contribute to the space charge. The presence of traps generally reduces the current by capturing most of the injected carriers. As the applied voltage increases all the traps will eventually become filled and the current will rise sharply back to the trap-free value [8].

5. Conclusions

The solar cells with CdTe/CdS/ITO/slide glass type structure were fabricated in form of thin films. The fabricated cells have been investigated using current-voltage (I-V) in the temperature range 20-300 K under a standard AM1.5 illumination in order to define the transport mechanism in the heterojunction. Tunnelling enhanced interface recombination has been found to dominate carrier transport mechanism in the junction at all measured temperature values.

Acknowledgements

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