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Low Polarization Voltage and High Sensitivity CMOS Condenser Microphone Using Stress Relaxation Design

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Abstract

In this paper, a CMOS condenser microphone with high sensitivity and low polarization voltage was designed, simulated and fabricated. Due to CMOS process temperature variant and lattice defects, the poly-membrane would be invoked normal stress and gradient stress. These two residual stresses would deform the membrane and increase the membrane's rigidity. For these concerns, an interlace slots design is utilized to reduce the normal stress up to 90%, and the annealing process is applied to decrease the gradient stress. The acoustical sensitivity was increased considerably to -45dBV at 2.7V bias voltage, and, the noise level is -85dBV at 1KHz.

Keywords: CMOS, microphone, gradient stress, stress release

1. INTRODUCTION

Over the last few decades, there has been a dramatic increase in the number of publication on MEMS Microphone research. The study of microphone fabrication has apparently moved from order MEMS process to standard CMOS process. Silicon micromachining technique had been successfully applied to the fabrication of miniature microphones on silicon wafer. The Knowles SiSonicTM microphone has been successfully commercialized for using in cell phones, cameras and other high volume consumer electronics. One major advantage that MEMS microphones over traditional microphones is the capability of handling the heat produced during the reflow soldering processes on a typical surface mount production line. However, the MEMS microphone is wire bond connected to a ASIC chip that will induce additional parasites, The motivation of monolithic integration of sensors with electronic part comes form four requirements, lowing the manufacturing cost and simplifying total process, solving interconnect bottleneck, miniaturizing total size and reducing the parasitic capacitance. One example is the accelerometer made by Analog Device [1]. A piezoelectric microphone with on-chip CMOS amplifier [2] had been demonstrated. The square diaphragm with the size 2mm on a side are fabricated by combining a silicon- nitride diaphragm with ZnO thin film layers. The measured sensitivity is 80uV/Pa at 3KHz and the frequency range is form 800Hz to 30KHz. The capacitive sensing is more widely used to detected membrane vibration Condenser microphone has benefits of high sensitivity, flat frequency response, and low noise level [3]. A FET condenser microphone with sensitivity up to 38mV/Pa had been reported in [4]. Basically, the sensitivity of microphone can be boosted by increasing membrane size and bias voltage, reducing the air gap, and relieving the residual stress. However, it is difficult to eliminate the thin film residual stresses, especially those of CMOS process. It is straightforward to release the residual stress through the boundary of structures [5]

2.   CONDENSER MICROPHONE OVERVIEW

The condenser consists of a high compliant diaphragm, a perforated but rigid backplate, and a back chamber, The acoustic holes in backplate allow the air between the diaphragm and the blackplate freely moving. The capacitance was polarized by a voltage source to a high impendence amplifier. If the distance between diaphragm and the backplate is d and the sound pressure altered sensing capacitance is Cs and the parasitic capacitance is Cp , the area of diaphragm is A, σis membrane intrinsic stress, Km is equivalent spring constants of diaphragm, and Vb is polarization voltage. Form this governing equation[6] we can conclude that high sensitivity can be designed by low intrinsic stress、low diaphragm spring constants、small gap、low parasitic capacitance and large capacitance variant 、higher polarization voltage and large diaphragm area. But when we consider the THD and stability, the gap and polarization voltage would become tradeoff terms. The gap in a MEMS microphone is much smaller so the electric field is on the order of 2-4 V/um [7]. This means that to build a similar sensitivity the diaphragm compliance of the MEMS microphone must larger than that of ECM diaphragm.

$$S_o = \frac{A}{k_m \sigma} \frac{V_b}{d} \frac{C_s}{C_s + C_p} \qquad (1)$$

3.   MICROPHONE DESIGN AND RESULT

Condenser microphone has the benefits of high sensitivity, flat frequency response, and low noise level. The sensitivity of microphone could be boosted by increasing membrane size and bias voltage, reducing the air gap and relieving the residual stress. However, the residual stress is difficult to eliminate especially in CMOS process. The best way to liberate the stress is to free the boundary. The novel design of condenser microphone with interlaced slots for stress relieving was presented. The diagram of our interlace slots design is shown in Fig.1. The radius and angle of the slots are two important parameters that determine the effect of the stress releasing. So the normal stress induced by the foundry process can be effectively relieved. The design parameters are listed in table 1. According to finite element simulation results, the novel interlaced slots structures have the capability of relieving the normal stress up to 90% [8]. This technique can not only enhance performance of microphone but also minimize the effect of process variation. Gradient stress would become an uncertain effect when the overlap slots were released. Because the membrane with slots edge can be treated as free boundary, the gradient stress of membrane would make the membrane convex or concave. In order to have flat plate, we use the monitor key [9] to evaluate the gradient stress, and using Coventorware to evaluate the membrane deformation in Fig.2. Hence we can use this FEM model to define the acceptable resonated frequency and stress range by modifying the annealing temperature of process in Fig3. The novel condenser microphone was implemented by using MXIC 2P2M 0.5μm CMOS process and post process. As shown in Fig4, the diaphragm and back-plate of microphone are realized by Poly2 and Metal layers, and their thicknesses are 0.3μm and 0.9μm, respectively. The gap between those two layers is 1.4μm. Then the acoustic back chamber was formed by back side ICP etching. Finally the sacrificial oxide layer was removed by Silox Vapox III solution and thus the microphone structure was released. The membrane profile was measured by interferometer is shown in Fig.5. Combining the normal stress and gradient stress which we measured into simulation tool, we can minimize the inaccuracy between simulation and experiment below 10%. To measurement the performance of the fabricated microphone, the microphone and interface ASIC were integrated by probing and characterized in the wafer level acoustic test system. With the polarization voltage increasing form 2.5V to 2.7V, the microphone sensitivity at 1KHz tone rises form-56dBV to -45dBV. The background noise duo to open space is about -85dB, according to the experience, the noise should be smaller than -95dB at the anechoic chamber. And die level anechoic chamber testing is ongoing. Fig.6(a) and Fig.6(b) show the measured results. The results indicate the way to design and fabricate of high sensitivity and low polarization CMOS condenser microphones.

Table 1: Design parameters.

	Diameter	Slot width	Slot gap	Slot Plurality	Thickness	1st Frequency
Ring type	350um	1um	5um	24	0.3um	40KHz

Fig.1 (a) 1/12 simply Ring type FEM stress relaxing design (b) half model cross section
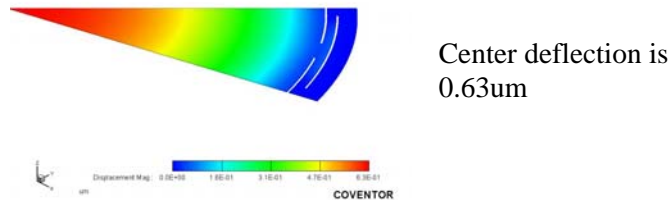

Center deflection is 0.63um

Fig. 2 Coventorware simulation result show the center deflection is 0.63um
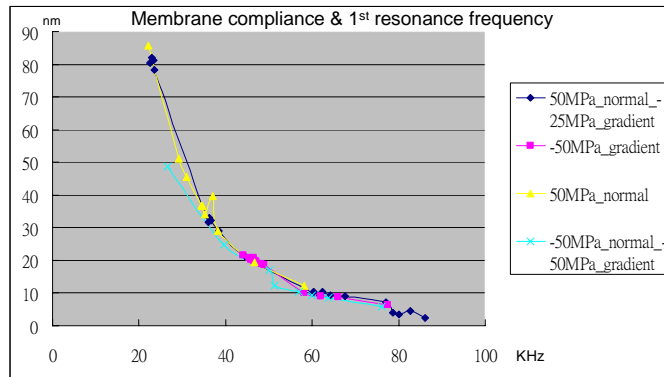

Fig. 3 Coventorware simulation results show the center compliance with membrane resonated frequency in difference stress condition.
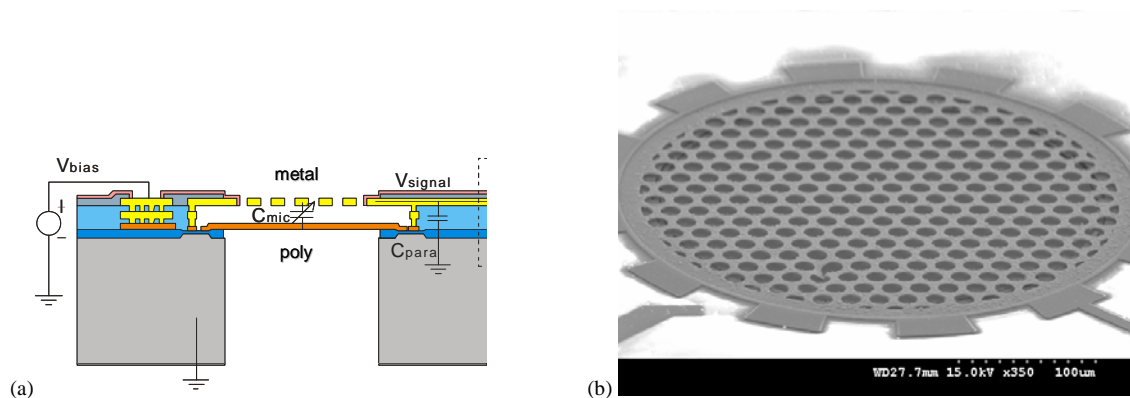

Fig. 4: (a)The diaphragm of Microphone cross section (b) SEM picture of fabricated microphone
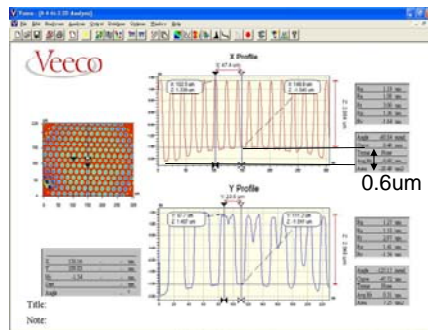
Fig. 5 White light interferometer measurement data, the center deflection of membrane is 0.6um
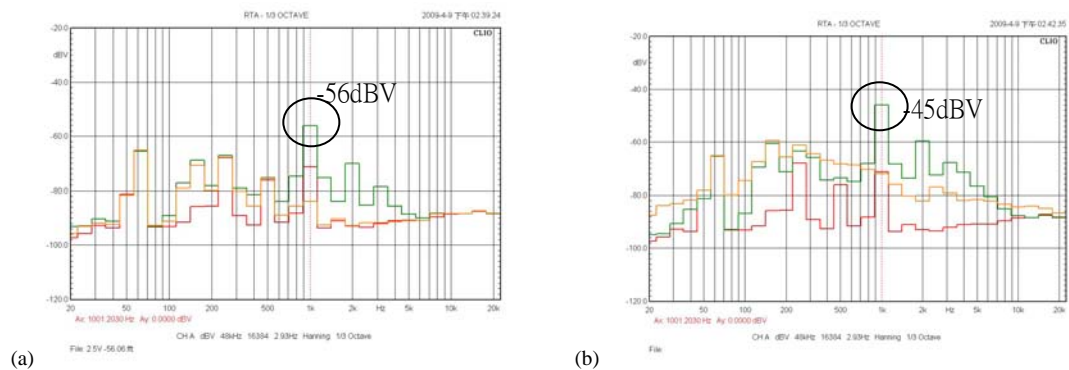

(a)					(b)

Fig. 6(a): The diagram indicates signal tone response of Ring-type design is -56dBV at 2.5V polarization voltage. Green line: 2.5V bias 1KHz single tone excited. Orange line: 2.5V bias . Red line: 0V bias 1KHz signal tone excited (b): The diagram indicates signal tone response of Ring-type design is -45dBV at 2.7V polarization voltage, we can see some nonlinearity tone was excited. Green line: 2.7V bias 1KHz single tone excited. Orange line: 2.7V bias. Red line: 0V bias 1KHz signal tone excited

Acknowledgements

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