Design and Performance Measure of 5.4 GHZ CMOS Low Noise Amplifier using Current Reuse Technique in 0.18μm Technology

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Abstract
A two stage CS-CS low noise amplifier (LNA) centered at 5.4 GHz with a minimum noise figure (NF) 0.423 over a band width of 100MHz is proposed. The current reuse technique is used to construct the main amplifier and LNA is tuned to that particular frequency using the resonant circuit. The designed LNA obtains a gain of 12.554dB, input reflection coefficient of -23.847dB, output reflection coefficient of \(-17.479\)dB, reverse isolation of \(-20.458\)dB and stability factor of 1.425.

Keywords: Low noise amplifier, current reuse, common source, common gate.

1. Introduction
Highly integrated, low cost RF and Microwave circuitry is becoming more and more essential to the proper operation of portable wireless equipment. Mobile cellular, wireless local area network (WLAN) communication and cordless telephones are becoming a part of our daily lives. The sensitivity of the receiver circuit is critical to the range over which the wireless network can operate. The receiver sensitivity depends on its components like filter low noise amplifier, mixer, Analog to Digital Converter. The receiver sensitivity mainly depends on the low noise amplifier (LNA) since it is the first stage of the receiver. The interface between the antenna and the LNA entails an interesting issue that divides analog designers and microwave engineers [2]. Fig.1 illustrates the receiving band distribution of current wireless communication standards in the range of 2.3GHz-6GHz.

The main function of LNA is to amplify the signal received from the antenna and at the same time it has to reduce the noise to provide it to further stages. An LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier.
2. Literature Survey

A CS-CS cascaded LNA has been proposed in [1][10], the second stage reuses the bias current of the first-stage to save power. In Fig.2, a Common Source (CS) second stage is cascaded upon a CS first stage to reuse the bias current. The output of the first stage is connected to the input of the second stage through a coupling-capacitor and bypass-capacitor which is used at the source of M2 to provide an AC ground. The small parasitic substrate impedance seen at node X of M1 degrades the quality factor of the tank connected at this node.

The LNA shown in Fig.3 proposed in [10] uses four on-chip and two off-chip inductors which improves the quality factor. These inductors are not fully integrated and occupy more area.

A transformer $g_m$ (trans-conductance) boosted current reuse CG-CS LNA proposed in [8] with a CG input stage for improving stability having one on-chip spiral inductor, which also improves its ability to be integrated within the chip compared to the other designs. Despite the transformer being a passive device consuming no electrical power, it is not suitable for adoption in UWB applications due to process nonlinearities and the presence of low parasitic resistance that can cause pronounced noise at the output of the amplifier.

A fully-integrated 5 GHz cascode floating-body and body-contacted FET LNA for WLAN applications is presented in [6] and compared and they achieve a NF below 1.0 dB and has 11 dB power gain, while consuming 12 mW of power. Due to the additional poly-silicon gate resistance, the body-contacted FET based LNA is seen to have higher NF. The power consumption is large and the gain is low.

The CG topology is well known for its constant wideband input impedance of $1/g_m$ where $g_m$ is the trans-conductance of the transistor. However, with technology scaling, due to the increase in drain-source conductance, the input impedance of the common-gate stage tends to deviate from the ideal $1/g_m$ and shows stronger dependence on output loading, which makes the wideband matching difficult. Traditionally, the common-gate topology is known to have higher NF than that of the common-source or cascode.
The Noise Figure (NF) of the CG LNA [16] depends on the device size and process parameters, it remains almost constant with frequency. Also, the NF of the CG LNA has a strong coupling with the bias point, or, in other words, the input matching resistance looking into the source. Reduction in the output noise figure of the CG LNA is achieved by using the gm-boosting technique that decouples the input matching and the NF of the CG LNA [13], [14], [15]. Hence we adopt the common source (CS) topology to design the LNA.

The proposed work involves the design of a low noise amplifier with Common Source topology and current reuse technique which can operate at a frequency of 5.4GHz. SECTION.3 describes the current reuse technique, SECTION.4 introduces the LNA design, SECTION.5 explains about the proposed low noise amplifier, SECTION.6 tells about the analysis of the LNA and SECTION.7 shows about the simulation results of the designed LNA and SECTION.8 provides the conclusion.

3. Current Reuse Technique

A current reuse LNA usually comprises a cascade of two amplifiers separated by a network that strategically redirects the AC and DC currents. The DC current flows through both stages and the AC signal is amplified by both [11]. To realize high gain and low power, a cascaded LNA has been proposed, where the second stage shares (reuses) the bias current of the first-stage to save power [8].

In order to achieve lower power consumption and high gain, the current-reuse structure is used. The current-reused structure is the easier topology for the circuit design. In order to achieve a flatness power gain, the inter-stage matching network is designed for gain compensation. The current reuse architecture used in the design of LNA is shown in the Fig.4.

4. LNA Design

The LNA design consists of three parts namely,

1. Input matching network.
2. Main amplifier section.
3. Output matching network.

4.1. Input Matching Network

The role of the input matching network is to minimize the input return loss (S11) without introducing additional noise. From the noise point of view, we may require a transformation network to precede the LNA so as to obtain minimum NF. The LNA is designed to have 50Ω resistive input impedance [2]. Amplifier section ensures a high gain, high linearity, low noise factor and low power consumption and at the same time it provides input impedance that can be conducive to the realization of broadband matching.

Here the input matching network consists of series connection of Z=50 ohms and L1 (2.5nH), which is in parallel with C1 (0.85pF). This is again in series with L2 (1.8nH). The input matching Network is shown in Fig.5. In this the parallel combination of two stage LC components acts as a filter.
4.2. Output Matching Network

The output matching network consists of a capacitor C5 (1.2pF) in series with parallel connection of L6 (0.920nH) and C6 (0.868pF). The output matching network is shown in Fig. 6. The output matching is designed in such a way to achieve a good matching between LNA and the mixer input. This also suppresses the noise as much as possible to provide good matching between LNA and the mixer input.

5. Proposed Amplifier

The target is to design a low cost power efficient CS-CS current reuse LNA which provides high gain, low noise and high stability at 5.4GHZ. The input and output matching networks are discussed in the previous sections. Main amplifier section is described as follows.

The LNA is constructed using common source (CS) with input matching network at its gate terminal, output matching network at its drain terminal of M1. There are two NMOS transistors (M1 and M2) cascaded in such a way that the supply (biasing voltage) is shared between these two transistors to achieve the property of current reuse. M2 acts as first stage and M1 acts as second stage. The RF input is provided to the gate of M2. The main amplifier section consists of a parallel connection of resonant circuit with resistance R1 (3kohm), capacitance C4 (4.2512pF), inductance L5 (0.198nH) connected to drain of M1. The second stage shares (reuses) the bias current with the first stage. The resonant circuit is used to tune the amplifier to that particular frequency. The proposed LNA is shown in Fig. 7. An inductor L4 is connected at source terminal for source degeneration and for improvement of stability.
6. Analysis

6.1. Input Impedance
The input impedance can be derived as follows;

\[ Z_{in} = (Z + X_L) \frac{1}{1} \frac{X_C + X_L}{2} \]  

\[ Z_{in} = \frac{Z + SL1}{1 + SC1(Z + SL1)} \]  

Z=50 ohm

6.2. Stability Analysis
The rollett’s stability factor K is used to specify the stability of the amplifier. This factor can be determined using the scattering parameters (s-parameters) and it is calculated with the formula shown below.

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{12}|^2}{2 |S_{21}| \| S_{12}|} > 1 \]  

Where; |Δ|=|S_{11}S_{22}-S_{12}S_{21}| >1 with \ S_{11} < 1 and \ S_{22} < 1

6.3. Output impedance
The output impedance is derived as follows;

\[ Z_{out} = X \]  

\[ Z_{out} = \frac{1}{SC} \frac{X_L}{1 + S^2 LC^2} + Z \]  

Z=50 ohms

6.4. Figure of Merit (FOM)
The LNA is unconditionally stable with a K- factor > 1. The FOM depends on noise figure (NF), third order interception point (IIP3), gain (G), dc power consumption (P_{dc}), resonant frequency (W_0) and bandwidth (B). FOM is given by,

\[ FOM = NF + IIP3 + G \cdot 10 \log \frac{P_{dc}}{1 mW} + 20 \log \frac{W_0}{B} \]  

6.5. Gain Analysis
The voltage gain is the ratio between output voltage (V_{out}) and the input voltage (V_{in}) and it is derived as follows. The small signal equivalent circuit is shown below in Fig.8 for gain analysis.

The output voltage is given by,

\[ V_{out} = I_{out} \left( \frac{X_L X_C}{X_L} \right) + I_{out} C_5 + I_{out} C_3 + I_r r_0 \]  

\[ I_{out} = - \frac{V_{out}}{R_{10}} \]  

Substitute Eqn.8 (I_{out}) in Eqn.7 (V_{out}).
\[ V_{out} = \left( -\frac{R}{R_0} \right) \left( \frac{V_{in}}{V_{gs1}} \right) + \left( -\frac{R}{R_0} \right) \left( \frac{V_{out}}{C_{s1}} \right) + \left( -\frac{R}{R_0} \right) \left( \frac{1}{C_{1}} \right) \left( \frac{I}{l_0} \right) \] (9)

Determine \( I_{r2} \),

\[ I_{r2} = I_{out} - (g_mV_{bs1} + g_mV_{bs1}) \] (10)

Substitute Eqn.11 (\( V_{s1} \)) & (\( I_{out} \)) Eqn.8 in the above Eqn.10, we get

\[ I_{r2} = \left( \frac{-V_{out}}{V} \right) \left( \frac{V}{X_LX_C} \right) \] (12)

Then substitute Eqn.12 (\( I_{r2} \)) in Eqn.9 (\( V_{out} \)) to obtain the voltage gain as shown below;

\[ V_{out} = \frac{V_{in}}{R_{01}} \left( 1 + \left( \frac{R_{01}X_L}{R_0} \right) + \left( \frac{R_{01}X_C}{R_0} \right) + \left( \frac{R_{01}X_{sc}}{R_0} \right) \right) \] (13)

Where,

\[ R_{01} = \frac{R_0}{Z_{res}} \] (14)

\[ Z_{res} = \frac{1}{L_s} \left( \frac{1}{C_L} \right) \] (15)

\[ X_L = SL_5 \] (16)

\[ X_C = SL_6 \] (17)

\[ X_{sc} = 1 \] (18)

7. **Simulation Results**

The LNA is designed, simulated and parameters are measured using Advanced Design System (ADS) tool in TSMC 0.18\( \mu \)m CMOS technology. The various parameters measured includes gain(Fig.10), input reflection coefficient(Fig.11), output reflection coefficient(Fig.12), reverse isolation factor(Fig.13), stability factor(Fig.15), noise figure(Fig.9), supply voltage, power consumption, standing wave ratio(Fig.14), threshold voltage (of M1/M2), Width/Length ratio (W/L) and gate-source voltage(Vgs). The simulation results of the proposed LNA are tabulated below in Table.1.

The proposed LNA achieves a high gain of 12.554dB at the desired frequency. The matching networks provide good matching, hence the input reflection coefficient of -23.847dB and output reflection coefficient of -17.479dB is obtained. Noise figure is defined as ratio of output signal to noise ratio to the input signal to noise ratio. In the proposed LNA the minimum noise figure obtained is 0.423. The stability factor is another important parameter determined using rollet’s stability factor (K).The stability factor obtained for the proposed LNA is 1.425.

| Table 1. SIMULATED RESULTS OF PROPOSED LNA |
|-----------------|-----------------|
| Frequency       | 5.4GHZ |
| Gain S(2,1)-(dB)| 12.554 |
| Input reflection coefficient S(1,1)-(dB)| -23.847 |
| Output reflection coefficient S(2,2)-(dB)| -17.479 |
| Reverse Isolation S(1,2)-(dB)| -20.458 |
Minimum Noise Figure (NF) | 0.423
---|---
Supply voltage (V) | 1.2
Power Consumption (mW) | 1.62
Threshold voltage (V) - M1/M2 | 0.325/0.309
Gate-Source Voltage (Vgs) - M1/M2 | 0.408/0.6
Rollet’s Stability Factor (K) | 1.425
Voltage Standing Wave Ratio (VSWR) | 1.137
W/L for M1 (µm) | 112/0.18
W/L for M2 (µm) | 30/0.18

Fig.9. Noise Figure

Fig.10. Gain S(2,1) in dB

Fig.11. Input Reflection Coefficient S(1,1) in dB
A comparison between the various parameters of the proposed work and various LNA designs in the reference papers is summarized in a table shown below in Table.2. This table helps us to provide the suitable way to design an efficient low noise amplifier.
REFERENCES


8. Conclusion

A CS-CS current reuse LNA is designed with high gain of 12.554 dB and minimum noise figure of 0.423. The proposed LNA achieves better trade-off between various measures like low noise, high stability and isolation compared to the other LNA designs. The power consumption is comparatively less with a voltage supply of 1.2V. The proposed LNA is used in the applications like wireless and satellite communications.

References