Upgrade for the ATLAS Tile Calorimeter Readout Electronics at the High Luminosity LHC

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ABSTRACT

This work presents an overview of the on-detector and off-detector electronics for the Phase II Upgrade of the ATLAS Tile Calorimeter at the LHC scheduled around 2022. Three options are being studied for the implementation of the new front-end readout: an improved version of the 3-in-1 card, a new version of the QIE chip and a dedicated ASIC called FATALIC. Moreover, the MainBoard will manage incoming signals from the FEBs and the DaughterBoard will send the digitized data to the off-detector electronics where the sROD will perform processing tasks on them. This work summarizes the status of the project.

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1. Introduction

ATLAS (A Toroidal LHC Apparatus) [1] is one of the four general purpose proton–proton detectors for the Large Hadron Collider (LHC) at CERN. ATLAS is composed of several subsystems including the Hadronic Tile Calorimeter detector (TileCal). The TileCal is a segmented calorimeter of steel plates and plastic scintillator tiles which covers the most central region of the ATLAS experiment. This subdetector is divided into four sections along the beam direction, each of which is segmented azimuthally into 64 modules. The light produced by a charged particle passing through a plastic scintillating tile is transmitted by wavelength shifting fibers to photomultiplier tubes (PMTs) where these signals are read out using 10,000 electronic channels which, after digitization, are transmitted through optical fibers to the Read Out Driver (ROD) modules.

The Phase II Upgrade of the LHC plans to increase the present instantaneous luminosity by a factor 10 making mandatory the redesign of the on-detector and off-detector electronics. The new requirements for the Phase II Upgrade comprise a full digital level-1 trigger, higher radiation tolerance, higher data rates and the use of highly reliable data protocols for transmission such as the GigaBit Transceiver protocol (GBT) [2]. The Demonstrator Program for Phase 0 aims to test the new readout architecture and it is planned to be installed into detector at end of 2013 shutdown. This Demonstrator will provide the read out for up to four adjacent drawers, where the hybrid electronics included in the drawers will be compatible with the present system and provide both analog and digital trigger signals.

2. On-detector electronics for the Phase II Upgrade

2.1. Modified 3-in-1 card

The Enrico Fermi Institute (University of Chicago) is developing a modified version of the present 3-in-1 card [3]. This Front-End Board (FEB) is composed of discrete components and can be divided into three stages: the fast signal processing chain, the slow signal processing chain and the calibration electronics and the control bus interface.

The fast signal processing chain includes a 7-pole passive LC shaper, bi-gain clamping amplifiers with a gain ratio of 16 and a pair of differential drivers feeding the analog signals from the low-gain channel and the high-gain channel to the digitizers which are placed in the MainBoard. The slow signal processing chain and the calibration electronics and the control bus interface.

The fast signal processing chain includes a 7-pole passive LC shaper, bi-gain clamping amplifiers with a gain ratio of 16 and a pair of differential drivers feeding the analog signals from the low-gain channel and the high-gain channel to the digitizers which are placed in the MainBoard. The slow signal processing chain includes a programmable 3-gain integrator which monitors the PMT current induced by a Cesium source and the minimum bias current induced during the collisions. Finally, the last stage includes a precise charge injection circuit, integrator gain controls and the control bus interface. This modified version presents better linearity and lower noise than the previous version. The prototype of the modified 3-in-1 card has been built using COTS components and has passed initial radiation tests.

2.2. QIE chip

The Argonne National Laboratory is working on the design of a FEB which includes a new version of the Charge (Q) Integrator and
Encoder (QIE) chip [4] developed in collaboration with Fermilab and CMS HCAL. The QIE includes a current splitter composed of 23 splitter transistors, providing four different ranges (16/23, 4/23, 2/23, 1/23), followed by a gated integrator and an on-board 6 bit flash ADC to cover a dynamic range of 17 bits. In this way only a simple digital interface is needed to communicate with the MainBoard. The QIE also includes a charge injection circuit for calibration and an integrator for source calibration. The QIE does not perform pulse shaping, therefore pile up problems are minimized and clean raw PMT pulses are measured.

At the present time two QIE prototypes have been produced and tested. The QIE version 10.4 is expected by November 2012.

2.3. FATALIC ASIC

The third option for the FEB is the Front end for ATLAS TileCal Integrated Circuit (FATALIC) ASIC [5] which is being designed at Laboratoire de Physique Corpusculaire de Clermont-Ferrand (LPC). FATALIC includes a multi-gain current conveyor (CC) with three different gains (1, 8, 64) which cover the full dynamic range of the PMT signal, followed by a shaper in order to improve the Signal-to-Noise Ratio (SNR). The readout chain is completed using an external 12 bit pipelined ADC with a sampling rate of 40 MS/s also developed at LPC and called twelve bits ADC for s-ATLAS TileCal Integrated Circuit (TACTIC). Moreover FATALIC includes an integrator and a 10 bit ADC with a low sampling rate for calibration purposes. In order to configure precisely the different time constants, passive elements are not included into the ASIC. Both chips are designed using the IBM 130 nm CMOS technology.

The first prototypes of the FATALIC, version 1 and 2, have been produced and tested. The FATALIC v3 has been delivered in March 2012 and it includes an integrator amplifier. LPC is currently designing the amplifier stage of the TACTIC which is planned to be ordered by beginning of August 2012.

2.4. MainBoard and DaughterBoard

The MainBoard [6] is responsible for the digitization of the signals coming from the FEBs, the digital control of the FEBs and sending digitized data to the DaughterBoard. The current design digitizes the signals coming from four modified 3-in-1 cards by using four 12 bit ADCs working at a sampling rate of 40 MHz. It implies the readout of 12 PMTs per MainBoard. The MainBoard maintains compatibility with the other two FEBs alternatives presented here.

The DaughterBoard is connected to the MainBoard through a 400-pin FMC connector and sends the digitized data to the super Read Out Driver (sROD) via high-speed links using the GBT protocol. In order to perform these functions the DaughterBoard includes two Xilinx Virtex 6 FPGAs, one transmitter SNAP12 format connector and two SFP+ format connectors. Future versions of the DaughterBoard will include two Xilinx Kintex 7 FPGAs, one QSFP+ and one transmitter SNAP12 format connector. Fig. 1 shows two 3-in-1 cards and one DaughterBoard connected to one MainBoard.

Both boards have been designed by the Stockholm University and the Enrico Fermi Institute (University of Chicago). First prototypes of the MainBoard and the DaughterBoard have been produced and tested. The final version of these boards is currently being designed based on the test results.

3. Off-detector electronics for the Phase II Upgrade

3.1. Super Read Out Driver

The sROD demonstrator board [7] consists of one Xilinx Virtex 7 and one Xilinx Kintex 7 FPGAs as processing core, four receiver...
Avago MiniPOD connectors, two transmitter Avago MiniPOD connectors, one QSFP+ format connector and one SFP format connector. This board is a double mid-size Advanced Mezzanine Card (AMC) and it is conceived to be plugged in a Advanced Telecommunications Computing Architecture (ATCA) carrier or in a Micro Telecommunications Computing Architecture (µTCA) system.

The sROD demonstrator board performs several functions. These include: data processing and data reception from Daughter-Boards; Timing, Trigger and Control (TTC); Detector Control System (DCS) management and transmission to MainBoards; data reconstruction and transmission to Read Out Subsystem (ROS); and data preprocessing and transmission to the Level-1 Calorimeter trigger system (L1Calo). Fig. 2 shows a block diagram of the sROD demo.

The Instituto de Física Corpuscular – Universidad de Valencia (IFIC-UV), the Laboratório de Instrumentação e Física Experimental de Partículas (LIP) and the Stockholm University are involved in the development of this project. The first prototypes of the sROD demonstrator board are expected by November 2012.

References