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Ni:Si as barrier material for a solderable PVD metallization of silicon solar cells

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Abstract

We study Ni:Si as a barrier material for the PVD metallization of silicon solar cells and investigate the long term solderability of Al/Ni:Si/Ag metal stacks in terms of peel forces and contact resistances. For this purpose, solar cell connectors are soldered on the Al/Ni:Si/Ag stacks in three different aging states: directly after metallization, after accelerated storage and after storage for six months. The thickness of the Ni:Si layer is varied in these tests. Furthermore we measure the contact resistance between cell interconnect ribbons and the test stack. To assess possible contamination of the Si by the metals we measure the effective lifetime of electron hole pairs during a regularly interrupted thermal treatment procedure. The samples with 200 nm or thicker Ni:Si layers soldered with the lead-containing solder and the flux 952S perform best and pass all tests.

Keywords: Silicon Solar Cell; PVD-Metallization; Solder connection; Long-term stability

1. Introduction

Al/Ni:V/Ag metallization stacks have been used in microelectronics as under bump metallization [1] for many years. This metallization stack was recently adapted to photovoltaics [2, 3]. The advantage of a PVD metallization compared to Al/Ag paste metallization in standard industrial type solar cells is the smaller Al layer and therewith the lower Al consumption. Intermetallic compound growth and interdiffusion of metals such as tin into the metallization and the solar cell during preparation or aging influence the long term stability of the metal stack, the solder connection and therewith the solar cell [4, 5]. Therefore in the Al/Ni:V/Ag stack the Ni:V layer protects the Al interface and the silicon wafer against Sn during thermal degradation and ensures long-time stability. The Ag layer is used as wetting layer. The purpose of additions such as V or Si to the Ni is to overcome the ferromagnetism of pure Ni and thus to allow an efficient industry sputtering process for production. The advantage of Ni:Si instead of Ni:V is a significantly lower reaction rate with the molten solder [6]. The aim of this work is to demonstrate the

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long-term solderability of an Al/Ni:Si/Ag metallization stack, and the efficiency of Ni:Si as barrier material for photovoltaic applications.

2. Experimental

We deposit the Al/Ni:Si/Ag stack on 156x156 mm² Si-wafers in our ATON500 in-line metallization system without vacuum break in between the preparation of the metal layers. The Al-layer is deposited by thermal evaporation, the Ni:Si and the Ag layers are deposited by sputtering. Here the Al layer has a thickness of about 2.5 µm, the thickness of the Ni:Si layer is 150 nm, 200 nm and 250 nm and the Ag layer is about 25 nm thick. Figure 1(a) shows the process flows for the 180° peel test and the contact resistance test.

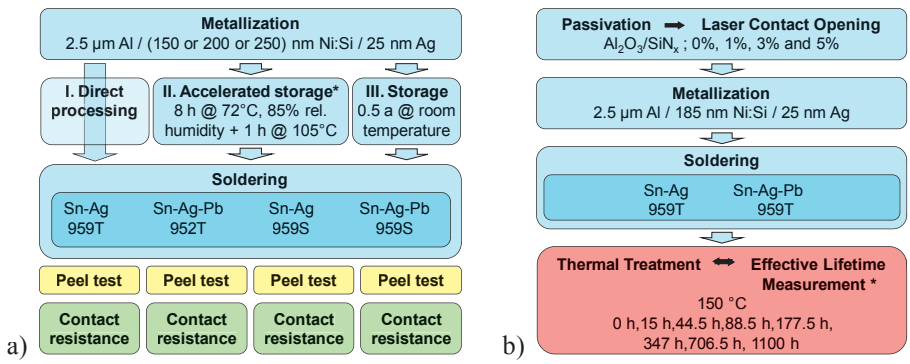

Fig. 1. (a) Process flow for peel test and contact resistance test, *accelerated storage according to ICP J-STD-003B. (b) Process flow for effective lifetime samples. Each solder / flux combination is prepared once for the peel test, once for the contact resistance measurement and once for the effective lifetime measurement.

After the metallization the samples are separated into three groups. The first is directly processed, the second undergoes an accelerated storage and the third is stored for half a year at room temperature. For soldering we use Cu-connectors plated with a lead-free solder (L1) consisting of 96.5 wt% Sn and 3.5 wt% Ag and a lead-containing solder (L2) comprising 62 wt% Sn, 36 wt% Pb and 2 wt% Ag. We apply two fluxes, one with a high (959T from Kester, F1) and one with a low solid content (952S from Kester, F2). A sample with each solder / flux combination is prepared once for the peel test and once for the contact resistance measurement. The peel test is performed in an angle of 180° in a Zwick Roell material testing machine directly after soldering. The contact resistance of the solder joints is determined with the transfer-length-method (TLM). Therefore 4 mm wide sample strips are cut and twelve to fifteen cell interconnect ribbons are soldered vertically to the sample strip. To assure the distance and the contact area between the cell interconnect ribbon we cut out a TLM pattern from an isolating foil and stick it to the sample strips.

For investigating the quality of the Ni:Si layer as diffusion barrier against lifetime killing metals we determine the effective lifetime of electron hole pairs in the silicon with the dynamic infrared lifetime mapping (dyn-ILM) method [7], see Figure 1(b). Therefore, the cleaned wafers are passivated with an Al_2O_3/SiN_x double layer and an area in between 0% and 5% is opened by laser contact opening to reproduce the laser contact opened area as it would be in a solar cell. They are then metalized with 2.5µm Al, 185 nm Ni:Si and 25 nm Ag. For soldering we apply the lead-free solder L1 and the lead-containing solder L2 and the flux F1. All these samples undergo a thermal treatment at 150 °C for up to about 1100 h, regularly interrupted for the dyn-ILM measurements.

3. Results and discussion

3.1. Mechanical stability

The minimum, mean, and maximum peel force of tin-coated Cu-connectors for the three storage groups (I., II., and III.) of the peel test is presented in Figure 2. DIN EN 50461 claims a minimum pull off force larger than 1 N/mm. In the case of 150 nm thick Ni:Si layers three of the twelve samples fall below this value. For the 200 nm thick Ni:Si layer the minimum peel force is always exceeded. For the 250 nm thick Ni:Si layer two samples of the twelve fall below the limit. The samples soldered with L2 and F2 have the smallest difference between the minimum and maximum peel force for all Ni:Si layer thicknesses and storage conditions.

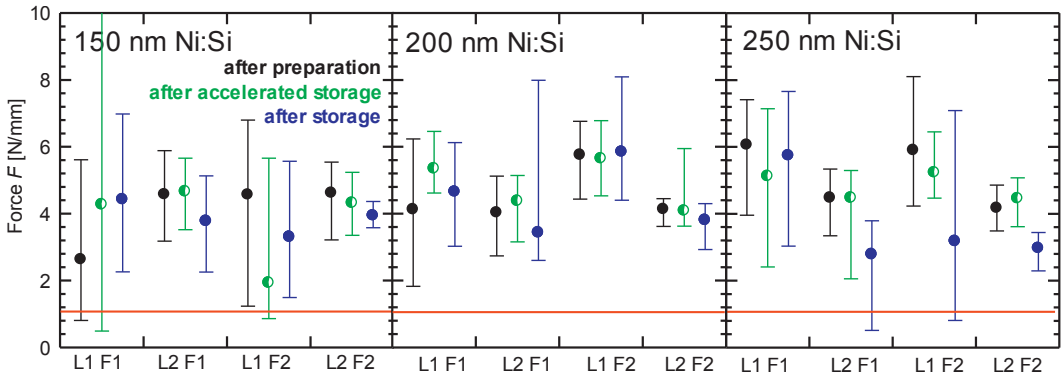

Fig. 2. Mean peel force (the error bars show the minimum and maximum value) after preparation (I.), after accelerated storage (II.) and after storage for 6 months (III.) depending on solder (L1 and L2), flux (F1 and F2) and Ni:Si layer thickness. The red line shows the required minimum adhesion force according to DIN EN 50461.

We perform a visual inspection after the peel test to determine the fracture modus. For PVD-metalized samples a fracture in the solder as shown in Figure 3(a) is the preferred fracture modus. Additionally, areas without contact presented in Figure 3(b) and fractures in the silicon as shown in Figure 3(c) appear. Only samples with 150 nm thick Ni:Si layers show the fracture mode in the Si-wafer, if they are soldered with the lead-free solder. This fracture indicates a pre-existing damage in the silicon, which may be caused by the soldering process. As this is a critical damage, these samples do not pass the test. The lead-free soldering needs a higher soldering temperature, thus the Sn-Ag soldering process introduces more stress than the Sn-Pb-Ag soldering process and leads to more damage in the silicon [4].

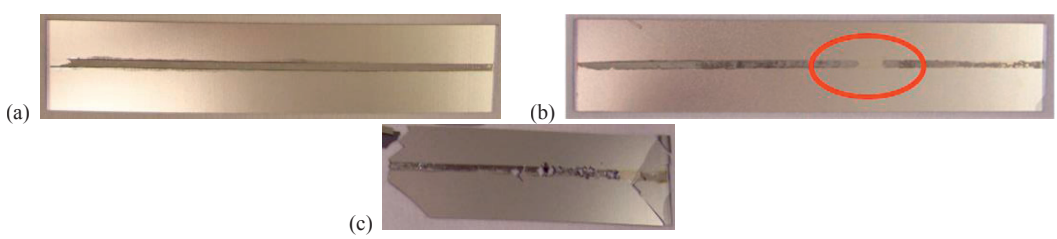

Fig. 3. Metalized Si-wafers after peel test. Figure (a) shows a fracture in the solder, in Figure (b). the red mark presents a not – contacted area, Figure (c) presents a sample with a fracture in the silicon named chipping.

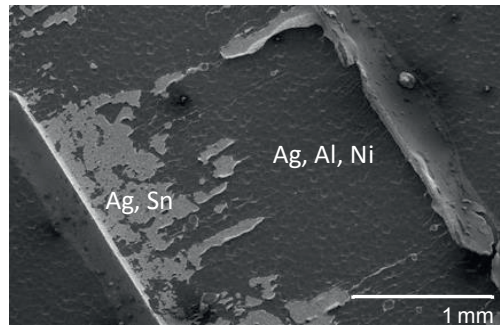

Fig. 4. REM images of solder area on metalized wafers after the peel test. The sample has a 150 nm thick Ni:Si layer and is soldered with L1 and F2 directly after processing. The image shows a mixed mode fracture of cohesive fracture in the solder and an interface fracture between solder and the Ni:Si-layer.

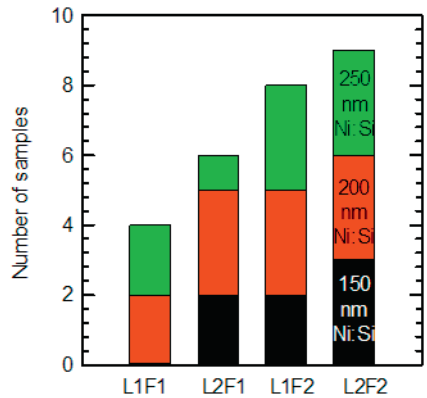

Fig. 5. The graph shows the results of the visual inspection. The number of samples with a fracture in the solder for more than 80% of the solder area plotted against the solder / flux combination.

If the fracture modus cannot be determined doubtlessly we take a REM image and execute an energy dispersive X-ray (EDX) measurement to determine the fracture mode as seen in Figure 4. Areas where Sn and Ag are found indicate a fracture in the solder. The Ag, Al and Ni containing areas exhibit the same structure as the not soldered ones and thus indicate not contacted areas.

We define the test as passed if more than 80% of the area exhibits a fracture in the solder after the peel test. The number of samples meeting this criterion is plotted against the solder / flux combination in Figure 5. Nine of nine samples prepared with L2 and F2 and eight of nine samples prepared with L1and F2 exhibit a fracture in the solder for more than 80% of the off peeled area. Hence, 952S is the favored flux and works best in combination with the Sn-Pb-Ag solder on the Al/Ni:Si/Ag stack for all Ni:Si layer thicknesses.

3.2. Contact resistance

In a second test we determine the contact resistance R_C of the solder contact. Figure 6(a) shows a plot of R_C as function of the solder - flux combination and the Ni:Si layer thickness for the three storage groups (I., II., and III.). The variance of the contact resistance R_C is largest for 150 nm thick Ni:Si layers. Two samples that are soldered directly after preparation have a contact resistance of about 0.1 mOhm cm^2.

With increasing Ni:Si layer thickness the variance of the R_C data decreases. For 200 nm Ni:Si only one sample after storage for 0.5 a has a higher contact resistance than 0.1 mOhm cm^2 and for 250 nm each contact resistance is in the desired region. 200 nm and 250 nm Ni:Si the samples soldered with the flux F2 and the solder L2 have the smallest variance for all storage conditions. By comparing the results of the visual inspection in Figure 5 with contact resistances in Figure 6 a clear correlation can be seen. All the samples soldered with the combination L2F2 exhibit a fracture in the solder for more than 80% of the area and have thus maximum 20% unconnected areas. Hence, a source for the variance of the contact resistances is the quantity of not contacted area or small cavities in the solder contacts.

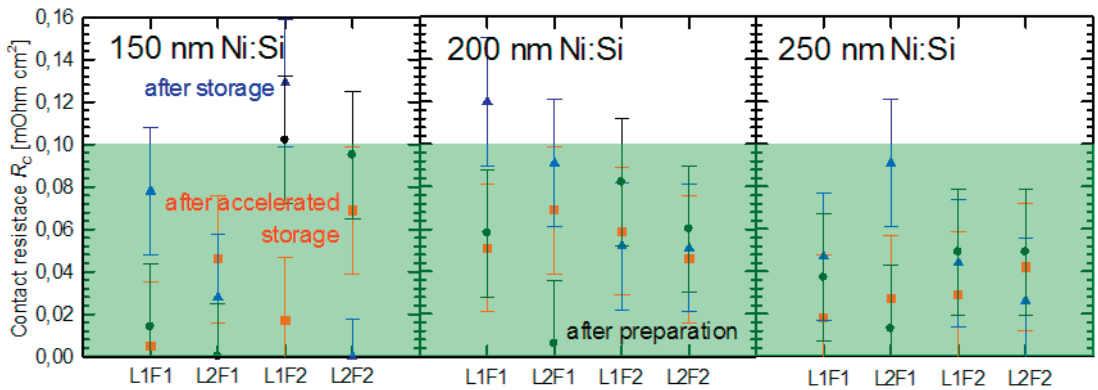

Fig. 6. Contact resistance RC as function of solder (L1 and L2) – flux (F1 and F2) combination and Ni:Si layer thickness. The error bars indicate the error of the measurement and the green area marks the desired range of values. Values smaller than 0 mOhm cm are corrected to the physically meaningful value of 0 mOhm cm^2.

3.3. Effective lifetime

We measure the lifetime of electron hole pairs by dyn-ILM measurements to investigate destructive diffusion of metal atoms into the silicon. Therefore, we interrupt the thermal treatment process of the samples at 0 h, 15 h, 44.5 h, 88.5 h, 177.5 h, 347 h, 706.5 h, and 1100 h. The measured effective lifetime τ_{eff} at a minority carrier density of $1.5 \cdot 10^{15}$ 1/cm^3 is presented in Figure 7 as a function of the thermal treatment duration at 150°C.

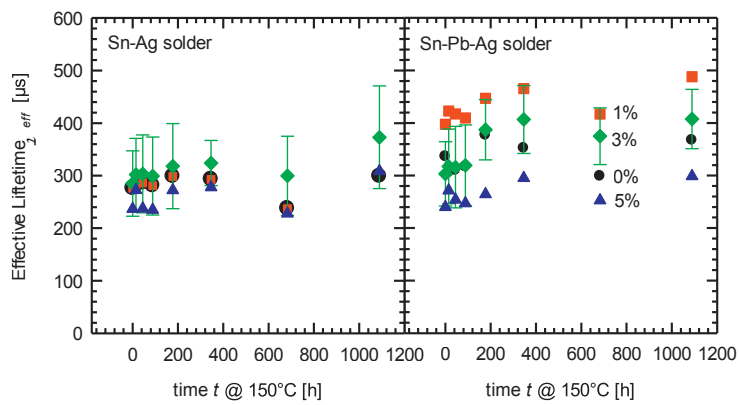

Fig. 7. Effective Lifetime of electron-hole pairs at $1.5 \cdot 10^{15}$ cm^{-3} of samples with 0%, 1%, 3% and 5% laser contact opened area as function of the thermal treatment duration at 150°C. The error of the measurement is exemplarily included for the samples with 3% laser contact opened area.

There is no decrease of the effective lifetime within the limits of error for all contact opening fractions and both kinds of solder. Therefore we conclude that no destructive metals diffused into the silicon and the Ni:Si layer works as an effective diffusion barrier.

4. Conclusion

We study Ni:Si as a barrier material in an Al/Ni:Si/Ag metal stack for the metallization of silicon solar cells. We examined the solderability of the metal stack by peeling tests and determined the solder joint contact resistance. The samples with 150 nm thick Ni:Si layers perform worst. Fractures in the silicon after the peel test reveal pre-exisiting damages in the Si presumable caused by the soldering process. They have the highest number of samples which not pass the peel test and the contact resistance measurement compared to the 200 nm and 250 nm thick Ni:Si layered samples. The origin of these problems is not really understood, yet. The samples with 200 and 250 nm thick Ni:Si layers soldered with the solder / flux combination L2F2 perform best in both tests. Here, the large area with fracture in the solder after the peel test indicates the good quality of the solder connection. That makes the spreading of the peel force and contact resistance smallest for this combination in the tests. Consequently, the lead-containing solder and the flux 952S work best on the Al/Ni:Si/Ag stack and passes all tests if the Ni:Si layer thickness is 200 nm or thicker. After 1100 h thermal treatment at 150 °C no decrease of the effective lifetime occurred for samples with up to 5 % contact opening in the PERC like rear side passivation below the tested metallization. Therefore, we proved the effectiveness of the Ni:Si layer as barrier material.

Acknowledgement

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