Full Length Article

LC-ladder filter systematic implementation by OTRA

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A R T I C L E   I N F O

Article history:
Received 14 May 2016
Revised 4 October 2016
Accepted 5 October 2016
Available online 15 October 2016

Keywords:
LC-ladder
Operational simulation
Leap frog method
OTRA

A B S T R A C T

In this paper Operational Trans Resistance Amplifier (OTRA) based LC-ladder filter implementation is presented. The proposed realization uses leap frog method which is a systematic approach for LC-ladder design. The OTRA is a current mode active block with low impedance at both input and output terminals. This active element is therefore a suitable choice for realizing voltage output filter. The proposed structure uses all grounded passive components that make it attractive from integration viewpoint. The validity of this approach is demonstrated by PSPICE simulations using CFOA (IC AD844) realization of OTRA. The simulated results are found in close agreement to proposed theory.

1. Introduction

Continuous time (CT) filter are extensively used in applications pertaining to communication, instrumentation and measurements. In some applications these filters have advantages over discrete-time counterparts as these do not produce sampling noise, consume less power and are much simpler to implement. This has led researchers to continue exploring the design and development of CT filters.

The primary filter design approach consists of (i) selection of order of the filter using design specifications for a given application (ii) determining the appropriate transfer function and (iii) circuit synthesis and implementation of the obtained transfer function. The transfer functions can be implemented either entirely out of passive components or using discrete/ integrated active circuits.

Higher order CT filters are synthesized using two dominant approaches namely cascaded biquads and lossless doubly terminated LC ladder realization. Generally losslessly doubly terminated LC ladder method is preferred as suggested in vast literature [1,2], since this method leads to component variation-tolerant filter realizations, much better dynamic range of performance and improved passband magnitude response accuracy than cascaded biquads. The only disadvantage of this method is the use of inductor as it’s realization in an integrated circuit (IC) form is not feasible in terms of space utilization, cost and tunability [1]. This shortcoming may be overcome either by using element replacement method or by leap frog method. In element replacement method inductors are replaced by gyrators. This method is suitable for grounded inductor based designs only as realizing high quality floating inductors proves to be challenging. Use of frequency dependent negative resistance (FDNR) is another method of element replacement however it is suitable for designing low pass filters. In leap frog method signal flow graph (SFG) approach is used to emulate the relationship between various passive elements. These SFGs are then physically realized using lossy and lossless active integrators [2]. The filter realizations so obtained are called active LC-ladder filters.

Few leap frog method based active LC-ladder filters [3–23] of varying order, using different approximation functions have been presented in literature. The structures use variants of second generation current conveyors (CCII) namely multiple output CCII (MCCII) [4], dual/multiple output current controlled CCII (DOCCII/MOCCCI) [5–7], differential voltage CC (DVCC) [8], differential voltage current controlled CCII (DVCCC) and differential voltage current controlled Current Feedback Operational amplifier (DVCCCFOA) [9], current feedback operational amplifier (CFOA) [10], current feedback amplifier (CFA) [11]; current differencing buffer amplifier (CCDBA) [15], current differencing transconductance amplifier (CTDA) [16–17], operational transconductance amplifier [18–20], current backward transconductance amplifier [21], CMOS based differential integrators [3], CMOS based lossy and lossless integrators [22–23]. These available structures provide voltage [9,10,15,18–20] and current [3–8,11–14,16,17,21–23]
The Operational Trans Resistance Amplifier (OTRA) \cite{24-29} is a current input voltage output active block which is neither slew limited nor does its gain bandwidth product is fixed unlike conventional voltage mode opamp. Additionally the effect of parasitic capacitances at the input can be eliminated due to internally grounded input terminals. These features make OTRA a suitable choice for realizing voltage output leapfrog filter. Therefore, the present work focuses on developing OTRA based LC-ladder filter with the systematic approach using leapfrog structure. Comparing the proposed structure with available literature on voltage mode LC-ladder filter with low output impedance except for those presented in \cite{10,15}, the proposed structure uses six OTRAs to provide 6th order response whereas \cite{10} and \cite{15} provide 5th and 3rd order responses respectively with same number of active blocks.

- The proposed topology uses six OTRAs to provide 6th order response whereas \cite{10} and \cite{15} provide 5th and 3rd order responses respectively with same number of active blocks.

Table 1
Summary of features of available LC-ladder filters based on leap frog method.

<table>
<thead>
<tr>
<th>Ref. No.</th>
<th>Active blocks</th>
<th>Output Impedance</th>
<th>Need of additional active block</th>
<th>Filter order, approximation and type</th>
<th>Inbuilt Tunability</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3]</td>
<td>CMOS based integrator</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>5th order, Butterworth, low pass filter</td>
</tr>
<tr>
<td>[4]</td>
<td>MOCC</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>3rd order, elliptic, low pass filter</td>
</tr>
<tr>
<td>[5]</td>
<td>MCCCII</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>5th order, Butterworth, low pass filter</td>
</tr>
<tr>
<td>[6]</td>
<td>DO-CCCII</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>6th order, Chebyshev, band pass filter</td>
</tr>
<tr>
<td>[7]</td>
<td>OAC + CCCII</td>
<td>Current</td>
<td>Low</td>
<td>Yes</td>
<td>3rd order, Butterworth, low-pass filter 6th order Chebyshev bandpass filter</td>
</tr>
<tr>
<td>[8]</td>
<td>DVCC</td>
<td>Current</td>
<td>Low</td>
<td>Yes</td>
<td>5th order, Butterworth, low-pass filter 6th order Chebyshev band-pass filter</td>
</tr>
<tr>
<td>[9]</td>
<td>DVCCFOA + DVCCII</td>
<td>Voltage</td>
<td>High</td>
<td>Yes</td>
<td>3rd order, Butterworth, low-pass filter</td>
</tr>
<tr>
<td>[10]</td>
<td>CFOA</td>
<td>Voltage</td>
<td>Low</td>
<td>No</td>
<td>5th order, –, low-pass filter</td>
</tr>
<tr>
<td>[12]</td>
<td>CDBA</td>
<td>Voltage</td>
<td>High</td>
<td>Yes</td>
<td>3rd order, elliptic, low-pass filter</td>
</tr>
<tr>
<td>[13]</td>
<td>CDBA</td>
<td>Current</td>
<td>Low</td>
<td>Yes</td>
<td>5th order, Butterworth, low-pass filter</td>
</tr>
<tr>
<td>[14]</td>
<td>CDBA</td>
<td>Current</td>
<td>Low</td>
<td>Yes</td>
<td>6th order, Chebyshev, band-pass filter</td>
</tr>
<tr>
<td>[15]</td>
<td>CCCDBA</td>
<td>Voltage</td>
<td>Low</td>
<td>No</td>
<td>3rd order, –, low-pass filter 3rd order, –, high-pass filter</td>
</tr>
<tr>
<td>[16]</td>
<td>CDTA</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>7th order, elliptic, low-pass filter</td>
</tr>
<tr>
<td>[17]</td>
<td>CDTA</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>6th order, Butterworth, low-pass filter</td>
</tr>
<tr>
<td>[18]</td>
<td>OTA</td>
<td>Voltage</td>
<td>High</td>
<td>Yes</td>
<td>–</td>
</tr>
<tr>
<td>[19]</td>
<td>OTA</td>
<td>Voltage</td>
<td>High</td>
<td>Yes</td>
<td>7th order, Chebyshev, low-pass filter</td>
</tr>
<tr>
<td>[20]</td>
<td>OTA</td>
<td>Voltage</td>
<td>High</td>
<td>Yes</td>
<td>3rd – order, Elliptic, low-pass filter</td>
</tr>
<tr>
<td>[21]</td>
<td>CDTA</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>5th order, Butterworth, low-pass filter</td>
</tr>
<tr>
<td>[22]</td>
<td>CMOS</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>5th order, Chebyshev, low-pass filter</td>
</tr>
<tr>
<td>[23]</td>
<td>CMOS</td>
<td>Current</td>
<td>High</td>
<td>No</td>
<td>3rd order, Chebyshev low-pass filter</td>
</tr>
</tbody>
</table>
\[ I_j = I_{j-1} - I_{j+1} \quad (j = 2, 4, 6, \ldots, n - 2) \]  
\[ V_j = V_{j-1} - V_{j+1} \quad (j = 1, 3, 5, \ldots, n - 1) \]

Since, \( I_{n+1} = 0 \) so \( I_n = I_{n-1} \).

Voltage at different nodes are given as
\[ V_j = \frac{I_j}{C_j} \quad (j = 2, 4, 6, \ldots, n - 2) \]
\[ V_n = \frac{I_n}{C_n} + G_t \]

where \( G_t = 1/R_L \).

The currents in series arm are given by
\[ I_j = \frac{V_j}{sL_j} \quad (j = 4, 6, \ldots, n) \]
\[ I_1 = \frac{V_1}{sL_1 + R_S} \]

Representing the elements in series arm as admittances and those in shunt arm as impedances Fig. 1 modifies to Fig. 2.

The series arm current is related to node voltages by
\[ I_j = Y_j (V_{j-1} - V_{j+1}) \quad (j = 1, 3, 5, \ldots, n - 1) \]

The correspondence between node voltage and series arm currents is given by
\[ V_j = Z_j (I_{j-1} - I_{j+1}) \quad (j = 2, 4, 6, \ldots, n - 2) \]
\[ V_n = Z_n I_{n-1} \]

The active realizations of the above equations will depend on terminal characteristics of the constituent active block. As this work uses OTRA as active block that processes current difference and provides voltage output, some changes are necessary for performing voltage differencing operation. The following section elaborates on it.

### 3. OTRA based implementation

The OTRA is a three terminal current mode active device shown symbolically in the Fig. 3 and is characterised by following terminal equation
\[ V_0 = R_m (I_1 - I_n) \]

where \( R_m \) is transresistance gain of OTRA. For ideal operation, \( R_m \) approaches infinity forcing the input currents to be equal and therefore this active block should be used in negative feedback configuration. The input terminals of OTRA are virtually grounded and hence are low impedance terminals. This property of OTRA leads to cancellation of parasitic effects at input thus making it a suitable for high frequency applications.

The OTRA provides voltage as output therefore direct realization of Eq. (8) is not possible. Eq. (8) is multiplied by scaling resistor \( R_{SC} \) to convert current into voltage. Eq. (6) modifies to
\[ R_{SC} I_j = R_{SC} Y_j (V_{j-1} - V_{j+1}) - V_0 = t_{ij} (V_{j-1} - V_{j+1}) \quad (j = 1, 3, 5, \ldots, n - 1) \]

where \( Y_1 = \frac{1}{sL_1 + R_S} \)
\[ Y_j = \frac{1}{sL_j + R_S} \]
\[ t_{ij} = R_{SC} Y_j \]

(\( j = 3, 5, \ldots, n - 1 \))
Using Eqs. (10), node voltages represented in Eqs. (7) and (8) are modified to Eqs. (12) and (13) respectively.

\[ j = \frac{Z_j}{R_{SC}} (R_{SC} i_j - R_{SC} i_{j-1}) \rightarrow V_j = t_j (V_{i_{j-1}} - V_{i_{j-1}}) \]

(12)

\[ V_n = Z_n \frac{R_{SC} i_{n-1}}{R_{SC}} \rightarrow v_n = t_n v_{i_{n-1}} \]

(13)

where, \[ Z_j = \frac{1}{sC_j} Z_0 = \frac{1}{sC_0 + G_j} t_j = \frac{Z_j}{R_{SC}} \]

(14)

It may be observed that active realization of Eqs. (10)–(14) is possible through differencing lossy and lossless integrator. The OTRA based differencing lossy integrator is given in Fig. 4. The output voltage \( V_{out} \) is expressed in terms of \( V_1 \) and \( V_2 \) as:

\[ V_{out} = \frac{1}{s(C + C_p)} \left( \frac{V_1}{R_1} - \frac{V_2}{R_1} \right) \]

(15)

4. Non-ideality analysis

Ideally the transresistance gain of OTRA approaches infinity and forces the two input currents to be equal. However, practically the transresistance gain \( R_m \) is finite and frequency dependent therefore its effects on the behavior of realized LC-ladder should be considered.

Considering a single pole model, the transresistance gain \( R_m \) can be expressed as

\[ R_m(s) = \left( \frac{R_0}{1 + (s/C_0)} \right) \]

(16)

For high frequencies, the transresistance gain \( R_m(s) \) reduced to:

\[ R_m(s) = \frac{1}{sC_p} \]

(17)

Here \( R_0 \) is DC open loop transresistance gain, \( \omega_0 \) is the transresistance cut-off frequency and \( C_p = 1/R_0\omega_0 \) is the parasitic capacitance. Considering finite transresistance gain the output voltage \( V_0 \) of Fig. 4 is recomputed as

\[ V_{out} = \frac{1}{s(C + C_p)} + \frac{G_2}{s} \left( \frac{V_1}{R_1} - \frac{V_2}{R_1} \right) \]

(18)

Eq. (18) clearly indicates that \( V_{out} \) modifies in presence of \( C_p \). However, the effect can be accommodated through self-compensation i.e. by pre adjusting the value of capacitor \( C \) or by connecting a capacitor of value \( C_p \) between ‘+’ and output terminal of OTRA.

5. Simulation Results

The theoretical proposition is functionally verified by taking a prototype sixth order Chebyshev low pass filter with 0.1 dB ripple in passband which may be obtained by considering \( n = 6 \) in Fig. 1. The normalized values of various passive elements [2] are \( L_1 = 1.1681, C_2 = 1.4040, L_3 = 2.0562, C_4 = 1.5171, L_5 = 1.9028, C_6 = 0.8618 \) and \( R_{load} = 0.7378 \). Considering the passband bandwidth of 340kHz, source resistor \( R_s = 1.2 \) kΩ and assuming \( C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C = 0.5 \) nF the values of the resistors for proposed OTRA based low-pass LC-ladder circuit are calculated as \( R_1 = 6.9 \) kΩ, \( R_2 = 2 \) kΩ, \( R_3 = 33 \) kΩ, \( R_4 = 3.6 \) kΩ, \( R_5 = 30 \) kΩ.
$R_S = 3.3\ \text{k}\Omega, \ R_R = 17\ \text{k}\Omega, \ R_L = 3.9\ \text{k}\Omega$. For verification purpose, CFOA based realization of OTRA [30] is used.

Fig. 6 shows the simulated and theoretical frequency responses for proposed OTRA based low-pass LC-ladder. The simulated passband bandwidth is observed to be 54 kHz which is in close agreement to the theoretical value. To study the response in time domain of the designed low pass filter an input comprising of three sinusoidal frequency components, 1 kHz, 54 kHz and 100 kHz is applied. The input time domain waveform and its corresponding frequency spectrum are depicted in Fig. 7 whereas those of output are depicted in Fig. 8. It is observed that the frequency components around $f_0$ are slightly attenuated and frequency components greater than $f_0$ are negligible.

It is well known that higher order filters based on LC ladder show very low sensitivity to component variation. To illustrate this fact the passband bandwidth is measured through Monte Carlo simulation with 10% tolerance in (i) only capacitors, (ii) only resistors and (iii) both resistors and capacitors. The histograms

![Simulated and theoretical frequency responses of the OTRA based low-pass LC-ladder.](image)

![Input Signal (a) Time domain waveform (b) Frequency spectrum.](image)

![Output signal (a) Transient Response (b) Frequency spectrum.](image)
Fig. 9. Monte Carlo analysis with 10% tolerance in capacitance values.

Fig. 10. Monte Carlo analysis with 10% tolerance in resistance values.

Fig. 11. Monte Carlo analysis with 10% tolerance in resistance and capacitance values.
obtained through simulations for cases (i)–(iii) are shown in Figs. 9–11 respectively. It is found that 75% of the samples are within ±3% of designed passband value.

6. Conclusion

A systematic development of OTRA based voltage-mode LC-ladder filter based on the leapfrog method is presented. A sixth order Chebyshev active ladder filter prototype is developed for illustration of the proposed theory which used six OTAs, six capacitors and fourteen resistors. All passive components are grounded in the realization which makes the proposition suitable from integration viewpoint. The designed structure is verified using PSPICE simulation where OTRA is emulated using two CFOAs. A close agreement is observed between the theoretical formulation and simulation results.

References