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Microarticle

Characterization of top barrier thickness from gate capacitance of high mobility III-V semiconductor MOS-HEMT devices

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ABSTRACT

We investigate the effect of varying the top barrier thickness on the gate C–V characteristics of InGaAs and InSb MOS-HEMT devices. The gate capacitance of these devices exhibits a sharp increase at certain gate voltages under both accumulation and inversion bias. The gate voltages at which some of these sharp changes occur depend on the thickness of the top barrier layer. The sharp rise in gate capacitance appears as a peak in the derivative of the capacitance with respect to the gate voltage. The positions of certain peaks of the derivative as a function of the gate voltage give information on the thickness of the top barrier layer. By exploiting this trend it is possible to extract the barrier thickness from the gate C–V characteristics.

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Introduction

As Si CMOS scaling approaches fundamental physical limits, III-V semiconductor devices appear as a potential alternative to continue the device scaling beyond the limit imposed on Si devices [1]. One major challenge to introduce III-V semiconductor devices is the high density of interface states at the semiconductor–dielectric interface [2]. This issue may be addressed by introducing the Metal-Oxide-Semiconductor-High-Electron-Mobility-Transistor (MOS-HEMT) which consists of a buried channel that is separated from the semiconductor–dielectric interface by a higher bandgap barrier [3]. Capacitance–voltage (C–V) characteristics have been widely used as a diagnostics tool for characterization of devices. We analyze the gate C–V characteristics of $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ and $InSb/Al_{0.2}In_{0.8}Sb$ MOS-HEMT devices and propose an approach to extract the barrier thickness from the gate C–V characteristics.

Results

Simulations are performed using Silvaco ATLAS TCAD tool. In order to verify our model, we simulate the low frequency (LF) C–V of an InAs MOS capacitor reported in [4]. Fig. 1 shows that our results are in reasonable agreement with the simulation results of [4]. Simulated C–V of [4] matches with experimental results.

The LF C–V curves of InGaAs/InAlAs MOS-HEMT devices, calculated by solving Poisson and Schrodinger equations self-consistently, are shown in Fig. 2. The curves exhibit staircase like behavior under both inversion and accumulation biases. Such behavior has also been observed experimentally [5]. At the first plateau for either type of bias, carriers are confined within the channel and the top barrier acts as a dielectric layer. However, at the second plateau, the top barrier region is also populated with carriers, hence the barrier does not contribute to the gate capacitance causing a rise in its value.

It is clearly seen in Fig. 2, that the gate voltages at which the transition to the second step in the C–V curves occurs under inversion or accumulation bias change with variation in the barrier thickness. To get a clearer picture, we differentiate the gate capacitance with respect to the gate voltage (dC/dV) and plot the derivative as a function of the gate voltage for different values of T_b in Fig. 3. The steps in C–V appear as derivative peaks. Thus a particular gate voltage at which the peak corresponding to the second step occurs represents a particular barrier thickness. We have plotted the barrier thickness as a function of the gate voltage at which the second peak of dC/dV occurs for both inversion and accumulation biases in Figs 4 and 5, respectively.

There is a monotonic dependence of the gate voltage at the peak of dC/dV on the barrier thickness. It is therefore possible to extract the barrier thickness from Figs 4 and 5. To investigate the generality of this trend, we have also simulated gate C–V of $InSb/Al_{0.2}In_{0.8}Sb$ strained MOS-HEMT devices. The thicknesses of the different layers are the same as those in Fig. 2. Figs 4 and 5 also show the dependence of the barrier thickness on the gate voltage at dC/dV peak of InSb devices. The same trend is observed for the both types of MOS-HEMTs. However with change in material,

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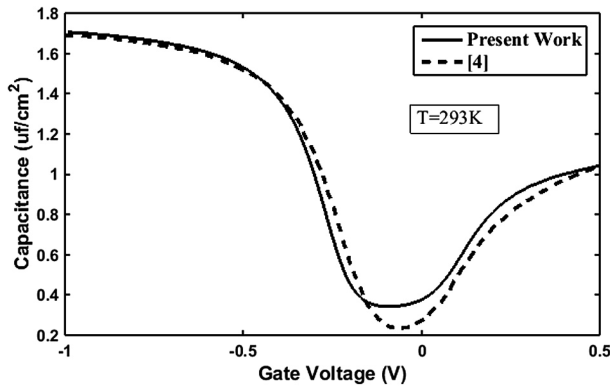

Fig. 1. Comparison of our simulated LF gate C–V curve of an InAs capacitor with that from [4].

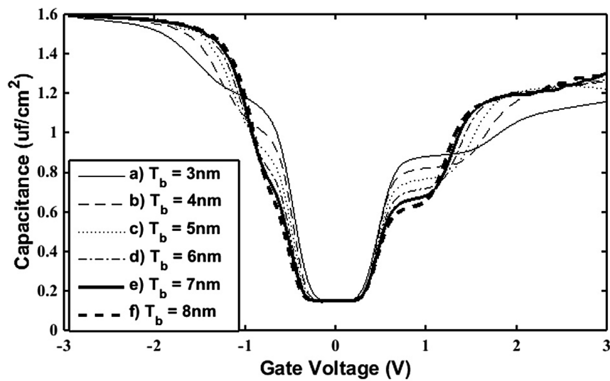

Fig. 2. LF gate C–V characteristics of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ MOS-HEMT with EOT = 1.77 nm and channel thickness T_{ch} = 4 nm for different barrier thicknesses T_b.

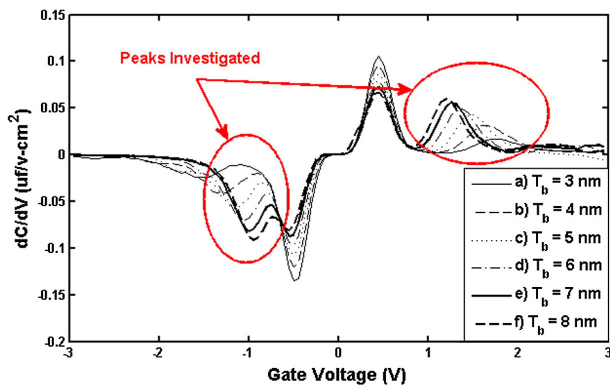

Fig. 3. *dC/dV* vs gate voltage of the InGaAs MOS-HEMT devices studied in Fig. 2.

T_{ch} or EOT, the gate voltage at which the peak of *dC/dV* occurs also changes. Effects of these parameters on *dC*/*dV* and the detailed scheme of extraction will be reported elsewhere.

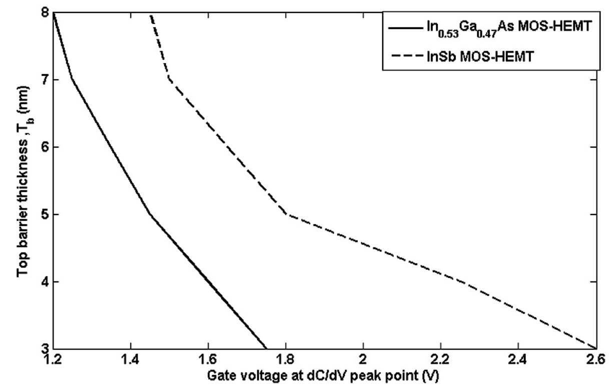

Fig. 4. Barrier thickness vs gate voltage at the second *dC/dV* peak under inversion bias for InGaAs and InSb devices.

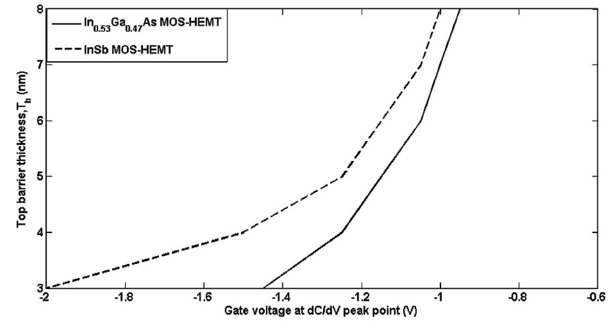

Fig. 5. Barrier thickness vs gate voltage at the second *dC/dV* peak under accumulation bias for InGaAs and InSb devices.

Conclusion

We have simulated the gate capacitance of III-V semiconductor MOS-HEMT devices. The devices demonstrate staircase like behavior of the C–V. The gate voltages at which certain stairs appear depend on the thickness of the top semiconductor barrier layer. This sharp increase in capacitance takes place when carriers begin to populate the top barrier region. By identifying the gate voltage at which the peak of *dC*/*dV* occurs, the barrier thickness can be extracted.

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