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CMOS Buffer Design Approach for Low power and Lower delay SRAM Design

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Abstract

Leakage power dissipation of on-chip SRAM constitutes a significant amount of the total chip power consumption in microprocessors and System on chips. With technology scaling, it is becoming increasingly challenging to maintain the yield while attempting to reduce the leakage power of SRAMs. The sources of SRAM power are the sum of the power consumed by decoders, memory array, write drivers, Sense amplifiers, and I/O line drivers. This paper is mainly focuses on the development of power and delay efficient SRAM structure. The paper describes the comparison of different CMOS tapper buffer topology's as word line drivers while driving large capacitive loads for minimizing power dissipation and propagation delay. The comparison has been designed and simulated using Cadence Virtuoso Spectre in 180 nm technology.

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Keywords: SRAM peripheral;CMOS tapper buffer;CMOS inverter;Tapering factor;Leakage power

1. Introduction

CMOS technology scaling has been a primary driving force to increase the processor performance. A drawback of this trend lies in a continuing increase in leakage power dissipation .Recent results have shown that leakage in SRAM peripheral circuits, such as word line drivers as well as input and output drivers are now the main sources of

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leakage[1].For instance, a word line driver drives its signal to a large number of memory cells. To drive large capacitive load, a chain of tapered inverter buffers is used, typically with two to five levels. A CMOS Tapered buffer is used to increase the driving ability of the logic circuitry; it is connected with large capacitive load. These are used between logic gate and large capacitive load to increase its drain current strength.

With advances in the VLSI technology, the use of inverting and non-inverting buffers is used to drive the large fan out by logic gate so that they can deliver large current for fast response. These circuits are required which can drive the load at high speed while not degrading the performance of previous stages in the chain of inverters [2].These buffers are used in the memory access path as word line drivers, to drive large off chip capacitances in I/O circuits and in clock trees to ensure that skew constraints are satisfied. The leakage power of standard memory cell is significantly lower than the leakage power of inverters buffers and that the inverter leakage grows exponentially with its size.

In brief, two main reasons explain this difference in leakage.

- Memory cells are designed with minimum-sized transistors mainly for area considerations. Unlike memory cells, periphery circuits use larger, faster and accordingly, more leaky transistors so as to satisfy timing requirements
- Memory cells use high threshold voltage transistors, which have a significantly lower leakage reduction compared with typical threshold voltage transistors used in peripheral circuits

The focus of this paper is, therefore, leakage-related reduction of power dissipation and propagation delay in on chip SRAM peripherals. This paper explores the comparison of different CMOS tapered buffer design for low power dissipation across load and reducing the propagation delay, highlighting the importance of leakage in on-chip SRAM peripherals. Comparisons of different CMOS buffer topology's with conventional tapered buffers are:1)Tapered buffer with optimal body biasing technique,2)Tapered buffer with feedback network,3)Tapered buffer with bypass circuitry,4)Proposed buffer design.

2. CMOS Tapered Buffer Design

The buffer consists of a chain of inverter stages where width of each MOS transistor in a stage is increased by a constant factor (called taper factor) than that of the transistors in the previous stage. The constant increase in width of transistors in each stage provides fixed ratio of output current drive to output capacitance and hence equal rise, fall, and delay times for each stage.

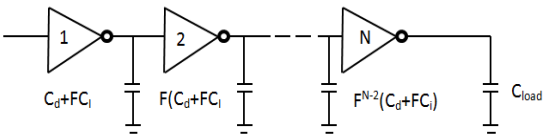

Fig.1.N stage Taper Buffer

The number of buffer stages required in each of the two design conditions depends on technology dependent tapering factor F. Here C_i denotes the input capacitance of minimum size inverter, Cd denotes the drain capacitance of minimum size inverter, C_{load} denotes the load capacitance of the last stage inverter, N denotes number of stages in the buffer chain and F denotes the scaling factor per stage in the inverter buffer chain [3]
The technology dependent tapering factor (F) is given by,

$$F^N = C_d/C_i \quad (1)$$

To achieve minimum delay, the number of stages are required are given by,

$$N_D = ln(C_L/C_I)/ln(F) \quad (2)$$

The power dissipation of the succeeding inverter increases F times compared to that of preceding inverter

$$PI = F * PI - 1 \quad (3)$$

2.1. Sources of power consumption[4]

- Dynamic power consumption:

$$P_{dyn}=f*C_L*V_{dd} \quad (4)$$

- Short circuit power consumption:

$$P_{Short} = \frac{\beta\tau}{9.6T}(V_{DD}-2V_{tn})^3 \quad (5)$$

- Static power consumption:

$$P_{static}= I_{static}*V_{dd} \quad (6)$$

- Total power:

Total power is the sum of dynamic, static and short circuit power consumption; the equation is given by-

$$P_{total}=P_{dyn}+P_{stat}+P_{short} \quad (7)$$

2.2. Circuit diagram for conventional buffer

Both four and two stage conventional buffers are shown in fig 2(a) and (b), which has capacitive load C_L=17.6fF and 295.8fF with F=5.0673 and 4.55 respectively when designed for minimum delay condition. The input is applied at IN and different buffer stages are cascaded to get output across C_L [5]

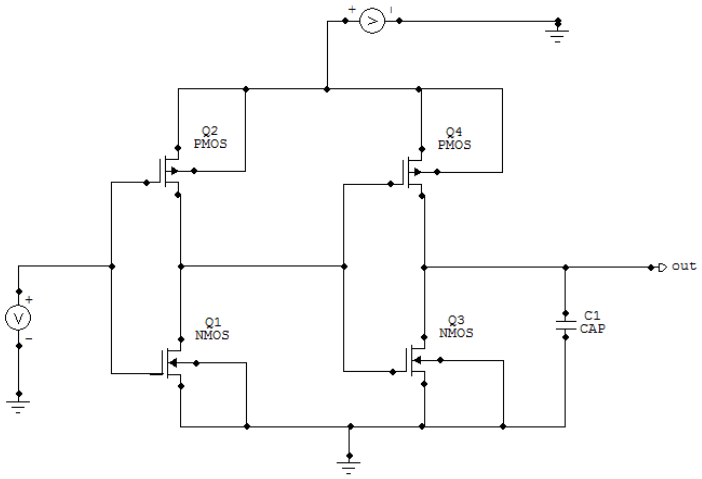

Fig.2. (a)Two stage conventional buffer

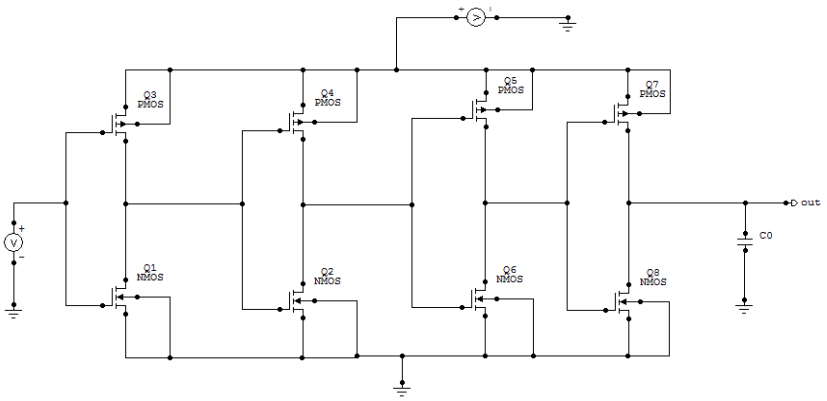

Fig.2. (b) Four stage conventional buffer

3. Comparative study on different CMOS buffer topology's

3.1. Optimal body biasing technique for CMOS tapered buffer

Body biasing of NMOS has been implemented by giving low voltage between body and the source terminals of Q1 shown in fig 3. Body biasing can vary V_{TH} of a MOS without varying the value of V_{DD} .The threshold voltage value for Q1 (0.2 V_{DD} to 0.4 V_{DD}) at which average power dissipation across load capacitor is least for the particular Reverse Bias voltage (RBB) V_{SB} and also reduced static power for the low power Tapered buffer design[6]

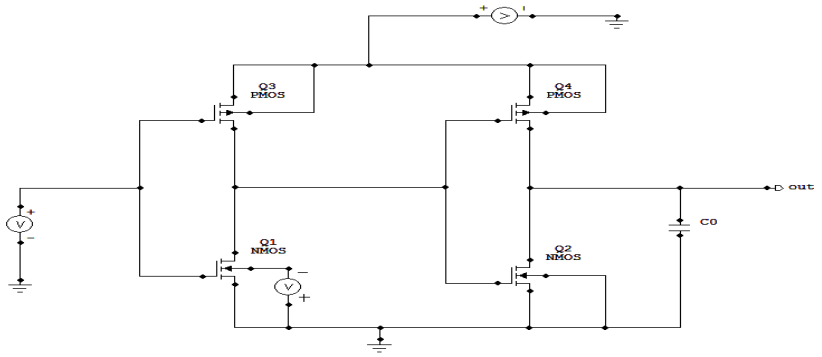

Fig. 3 Circuit diagram for two stage reverse body biasing CMOS tapered buffer

Table 1. Comparison of results for RBB and conventional Buffer

Fixed Body Biasing voltage for Q1	Static power(pW)	Average power dissipation across C_L(nW)	Propagation delay(ns)
Conventional	75.09	26.53	10.099
200mV	53.10	21.43	10.100
300mV	50.52	19.4	10.101
400mV	49.40	23.4	10.102

3.2. CMOS two stage tapered buffer feedback network

The circuit shown in fig 4 which dissipates lesser power because the short circuit component of power is eliminated in the design by tri-stating its output mode momentarily before every output signal transition. This can be obtained by giving the gate driving signal of PMOS (NMOS) transistor of the output stage via a feedback network which delays the driving signal and avoids the short circuit current [7]

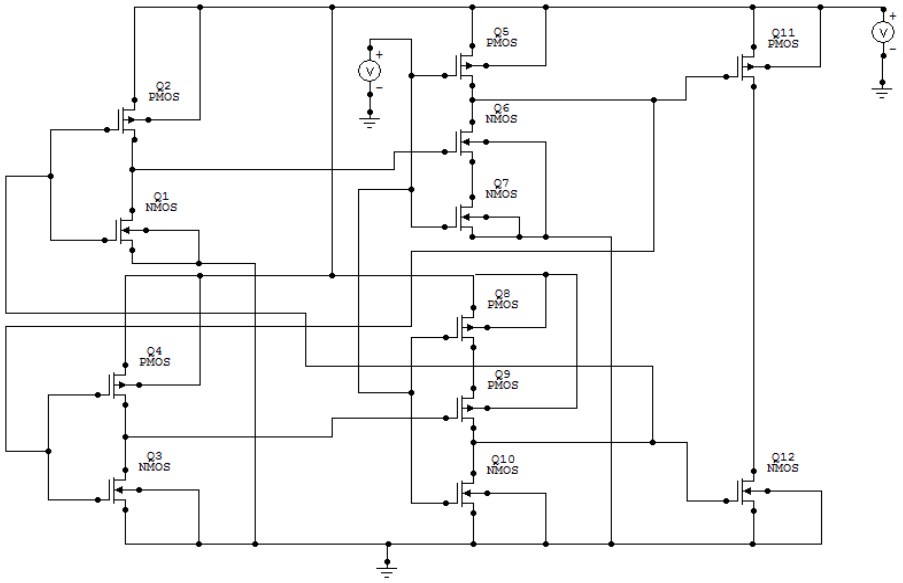

Fig. 4 Circuit diagram for two stage CMOS tapered buffer with feedback network

Table 2. Comparison of results for conventional Buffer and Taper buffer with feedback network

Topology's	C_L(fF)	N	F_D	Static Power(pW)	Average Power dissipation across C_L(nW)	Propagation Delay(ns)
Conventional	17.6	2	5.06	75.09	26.53	10.099
Taper buffer with feedback network	17.6	2	5.06	101.9	9.58	10.202

3.3. CMOS Tapered Buffer with bypass circuitry

The circuits shown in fig 5 (a) and (b), which dissipates lesser power across load and lesser propagation delay than the conventional buffer design approach because where NMOS and PMOS is used as bypass and charging /or discharges the output node in advance before input signal reached the output stage by stage. This reduces the power dissipation across load and propagation delay in a large manner because input signal need not pass all the stages; it can easily bypassed directly to last stage. So switching of circuit becomes really fast that minimizes propagation delay [8]

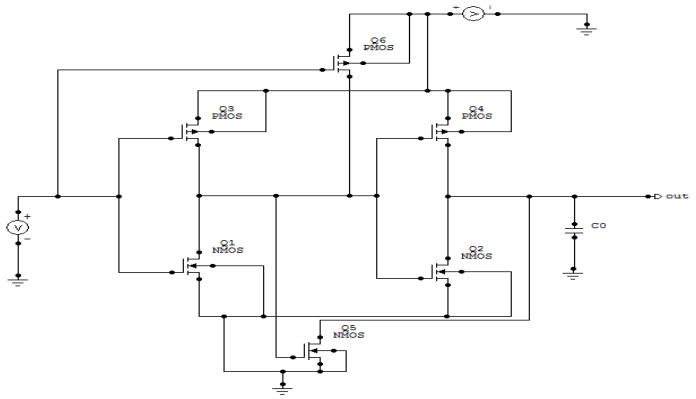

Fig.5 (a) Two stage Taper buffer with bypass circuitry

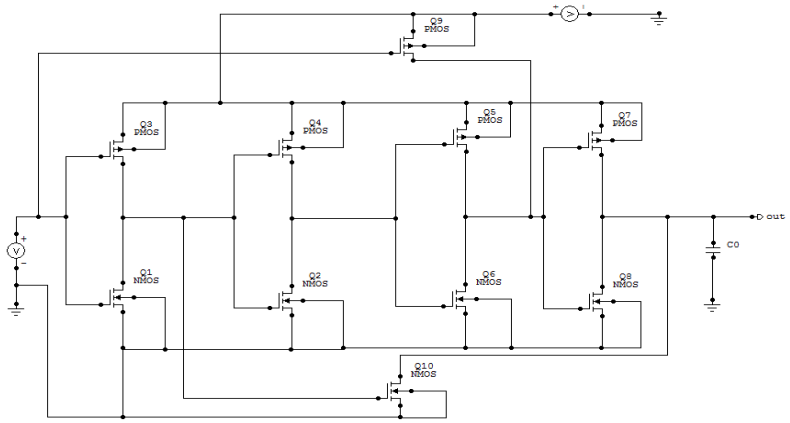

Fig.5 (b) Four stage Taper buffer with bypass circuitry

Table 3. Comparison of results for two stage conventional Buffer and Tapper buffer with bypass circuitry

Topology's	C_L(fF)	N	F_D	Static Power(pW)	Average Power dissipation across C_L(nW)	Propagation Delay(ns)
Conventional	17.6	2	5.06	75.09	26.53	10.099
Taper buffer with bypass circuitry	17.6	2	5.06	75.06	12.59	10.096

Table 4. Comparison of results for four stage conventional Buffer and Tapper buffer with bypass circuitry

Topology's	C_L(fF)	N	F_D	Static Power(nW)	Average Power dissipation across C_L(nW)	Propagation Delay(ns)
Conventional	295.8	4	4.55	1.944	493.6	10.255
Taper buffer with bypass circuitry	295.8	4	4.55	1.945	134.1	10.224

4. Proposed Buffer Design

Proposed Buffer design is the combination of both four stage tapered buffer with four stage bypass circuitry and reverse body biasing technique shown in fig 6. Optimization of propagation delay and power dissipation across load can be possible via bypass circuitry, but the unwanted static power dissipation will increases. By keeping reduction on propagation delay and power dissipation across load, we have to reduce the static power dissipation. By using the reverse body biasing technique at Q1, we can reduce the sub threshold leakage current. The basic idea of the modified circuit is to be observe the threshold value for Q1 at which average power dissipation across load capacitor is least for the 100mV

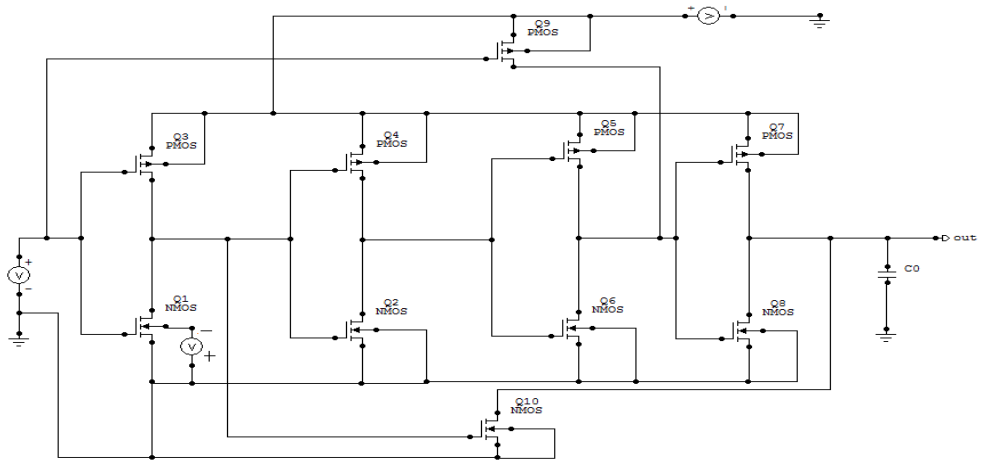

Fig. 6 Circuit diagram for four stage proposed CMOS tapered buffer with bypass circuitry and reverse body biasing

Table 5. Effect of variation of V_{th} on the output parameters of conventional Buffer and Proposed Buffer

Fixed Body Biasing voltage for NM0	Static power(nW)	Average power dissipation across C_L(nW)	Propagation delay(ns)
Conventional	1.944	493.6	10.255
100mV	1.929	178	10.225
200mV	1.923	171.8	10.266
300mV	1.920	210.3	10.227

Table 6. Effect of variation of V_{th} on the output parameters of conventional Buffer and Proposed Buffer

Topology's	C_L(fF)	N	F_D	V_{th} of NM0	Static Power(nW)	Average Power dissipation across C_L(nW)	Propagation Delay(ns)
Conventional	295.8	4	4.55	0.527V	1.944	493.6	10.255
Proposed Buffer Design	295.8	4	4.55	0.555V	1.929	178	10.225

5. Experimental Results

Table 7. Comparison for Propagation delay and power dissipation between conventional and Proposed Buffer

Topology's	F_D	N_D	C_L(fF)	Static Power(pw)	Power dissipation across load(nW)	Propagation delay(ns)
Conventional taper buffer	5.06	2	17.6	75.09	26.53	10.099
Taper buffer with RBB technique(300mv)	5.06	2	17.6	50.52	19.4	10.101
Taper buffer with feedback network	5.06	2	17.6	101.9	9.58	10.202
Taper buffer with bypass circuitry	5.06	2	17.6	75.06	12.59	10.096
Conventional taper buffer	4.55	4	295.8	1.944(nw)	493.6	10.255
Taper buffer with bypass circuitry	4.55	4	295.8	1.945(nw)	134.1	10.224
Proposed Buffer Design	4.55	4	295.8	1.929(nW)	178	10.225

6. Conclusion

In this paper power dissipation and propagation delay parameters are calculated during design of CMOS buffer driving large capacitive loads especially act as word line drivers in the SRAM design. The proposed buffer has been designed using 180 nm technology and simulated using Cadence Virtuoso environment. An improvement in both static and dynamic power dissipation has been achieved while reducing propagation delay as compared to conventional CMOS buffer design. The proposed buffer can be used to provide power efficient and minimum propagation delay SRAM design. These parameters can further be reduced by using other technologies like 135nm, 90nm, 45nm which are more predominantly used compared to 180nm technology in recent times. This is applicable to design circuits where micro watts of power dissipation becomes major factor and less amount of power and minimum propagation delay to drive the circuit like SRAM

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