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Drain Current and Noise Model of Cylindrical Surrounding Double-Gate MOSFET for RF Switch

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Abstract

In this paper, we have explored the drain current model and subthreshold model of Cylindrical Surrounding Double-Gate (CSDG) MOSFETs, for the wireless telecommunication systems to operate at the microwave frequency regime of the spectrum. This CSDG MOSFET can be used as the RF switch for selecting the data streams from antennas for both the transmitting and receiving processes. We emphasize on the basics of the drain current with DIBL and SCE, for the integrated circuit of the radio frequency sub-system. Using this device we analyzed that the drain current is higher, output conductance is lower which shows that the isolation is better in CSDG MOSFET as compared to double-gate MOSFET and single-gate MOSFET.

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1. Introduction

The Multiple-gate MOSFETs have been proposed to scale down CMOS technology more aggressively [1]. Among these non-classical structures, double-gate (DG) and surrounding-gate MOSFETs are becoming intense subjects of very large-scale integration research. Recently, continuous analytic drain current models have been developed for DG [2] and surrounding-gate [3] MOSFETs, respectively. Without charge sheet approximation, these two models are derived directly from the Pao–Sah integral [4] for DG and surrounding-gate MOSFETs with undoped (or lightly doped) silicon body. It has been validated by numerical simulations that these models can continuously cover all the three operation

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regions without the need for nonphysical fitting parameters. As the device size scales down, the total number of channel dopants decreases, resulting in a larger variation of dopant numbers, and significantly impacting threshold voltage [5]. The use of symmetric DG MOSFETs with ultrathin bodies and ultrathin gate oxides allows to suppress short-channel effects (drain-induced barrier lowering and subthreshold slope degradation), making unnecessary the conventional use of high channel doping densities and gradients [6]. This absence of dopant atoms in the channel decreases mobility reduction by scattering and eliminates random microscopic dopant fluctuations inherent to ultra-small dimensions devices which give rise to unwanted dispersion in the turn ON characteristics.

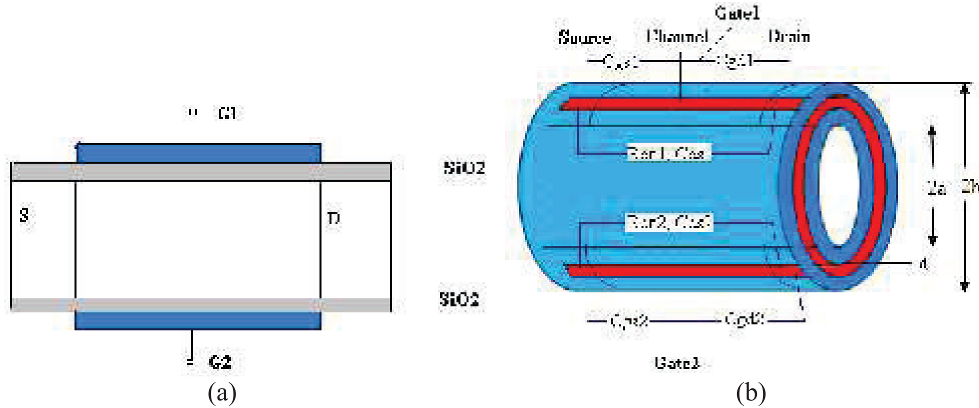
The main idea of a Cylindrical Surrounding Double-Gate (CSDG) MOSFET is to control the Si channel very efficiently with selecting the channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to suppress the SCE and leads to higher drain currents as compared with a MOSFET having only one gate. This also provides the low subthreshold slope due to large control over the channel region. Impressive compact and analytical models for the DG MOSFETs, which account for quantum, volume-inversion, short channel effect, DIBL and non-static effects have been proposed by Ge and Fossum [7]. Ge and Fossum also suggest that quantum mechanical effects have are negligible for silicon films thicker than 10 nm (i.e., radius >5 nm), so we did not considered this effect in this proposed model anyway. For films thinner than 10 nm, quantum confinement should be considered. It leads to a reduction of the channel charge density and an increase of the threshold voltage [7]. In this paper, we have presented a design of CSDG MOSFET and its details to understand the effect of device geometry as of current model. Each of the parameters is discussed separately for the operation of CSDG RF MOSFET structures by Srivastava et. al. [8]. The organization of the paper is as follows: The CSDG RF MOSFET model is presented in the Section 2. The explicit charge model of CSDG MOSFET is discussed in the Section 3. The drain current, gate leakage current noise model of the CSDG MOSFET and short channel effects are discussed in the Section 4. Finally, the Section 5 concludes the work.

2. Model of Cylindrical Surrounding Double-Gate (CSDG) MOSFET

The DG MOSFET as shown in Fig. 1(a), is a natural extension from a disparage SOI devices. This design reveals the n-type DG MOSFET, similarly we can design p-type DG MOSFET. The double-gate has increased transconductance and a lower threshold voltage. Here we design symmetrical type of device, means the thickness of back-oxide layer is identical as of front-oxide and identical gate materials are used, which allows both gates to control the operation of the device. Since with the symmetrical gate design, the channel area is raised to increase the saturation current and the Si body control is enhanced to reduce the short channel effects.

In the DG MOSFET as shown in the Fig. 1(a), when voltage is applied to the gates of device, the active Si region is so thick that the control region of the Si remains controlled by the majority carriers in the region. This causes not one but two channels to be formed. One channel is near the top boundary between Si and the Si insulator and the other one is like wise at the bottom interface. These two channels are separated by enough distance as to be independent of each other. This creates two independent transistors on the same piece of silicon. Each gate as front-gate (G_1) and back-gate (G_2) can control one half of the device and its operation is completely independent to each other. The total current through the device is equal to the sum of the currents through the separates channels under G_1 and G_2. The relative scaling advantage of the DG MOSFET is about two times. The performance of the symmetrical version of the DG MOSFET is further increased by higher channel mobility compared to a bulk MOSFET, since the average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model [9]. For the design of CSDG MOSFET, we convert the Fig. 1(a), with a circular rotation along any one gate to find a form of cylinder. Then we found the compact model of

CSDG MOSFET as shown in Fig. 1(b), which is used for the characterization of resistance, capacitance, electrostatic potentials and current of the doped device. The ultrathin CSDG MOSFET with 5 nm thick body, with $N_A = 10^{20}$ atoms/cc, internal radius, a = 10 nm and external radius, b = 15 nm. It is expected that the saturation current of a surrounding-gate MOSFET should be larger than that of a double-gate MOSFET.



(a) (b)

Figure. 1. Schematic of the a) Basic DG n-MOSFET, b) Models of a CSDG MOSFET transistor operating as a switch at ON state.

3. Accurate Explicit Model Of CSDG MOSFET

Assuming the gradual channel approximation in an undoped (lightly doped) n-type CSDG MOSFET (Fig. 1b) Poisson's equation takes the following form:

$$\frac{d^2\psi}{dr^2} + \frac{1}{r}\frac{d\psi}{dr} = \frac{qn_i}{\varepsilon_{si}} e^{q(\psi - V)/kT} \tag{1}$$

Where q is the electronic charge, ni the intrinsic carrier concentration, ε_{Si} the permittivity of silicon, V is the electrostatic potential, and ψ is the electron quasi-Fermi potential. It has been assumed that the hole density is negligible compared with the electron density. Equation (1) must satisfy the following boundary conditions:

$$\frac{d\psi}{dr}(r=0) = 0\,, \qquad \frac{d\psi}{dr}(r=a) = \psi_{\text{int}-surface}\,, \qquad \frac{d\psi}{dr}(r=b) = \psi_{ext-surface} \tag{2}$$

Where ψ is the surface potential, int-surface stands for the internal gate surface and ext-surface stands for the external gate surface. The current mainly flows along the direction of channel for both the gates. Therefore, we can assume that is constant along the direction. Equation (1) can be analytically solved as [10, 11]:

$$\psi(r) = V + \frac{kT}{q}\log\left(\frac{-8AkT\varepsilon_{Si}}{q^2 n_i (1 + Ar^2)^2}\right) \tag{3}$$

A is related to ψ_S through the second boundary condition in (2). The total mobile charge (per unit gate area) can be written as:

$$Q = C_{ox}[V_{gs} - \Delta\varphi - (\psi_{\text{int}-surface} + \psi_{ext-surface})] \tag{4}$$

where $C_{ox} = \varepsilon_{ox} / R\ln(1+\frac{t_{ox}}{R})$ and $\Delta\varphi$ is the work-function difference between the gate electrode and intrinsic silicon. From Gauss's law, the following relation holds:

$$Q = C_{ox}[V_{gs} - \Delta\varphi - (\psi_{\text{int}-surface} + \psi_{ext-surface})] = \varepsilon_{Si}\left.\frac{d\psi}{dr}\right|_{r=a} + \varepsilon_{Si}\left.\frac{d\psi}{dr}\right|_{r=b} \quad (5)$$

Substituting (3) into (5) leads to:

$$\frac{q(V_{gs} - \Delta\varphi - V)}{kT} - \log\left(\frac{8kT\varepsilon_{Si}}{q^2 n_i a^2}\right) + \log\left(\frac{(1+Aa^2)^2}{Aa^2}\right) + \frac{Aa^2}{1+Aa^2} = 0$$

$$\frac{q(V_{gs} - \Delta\varphi - V)}{kT} - \log\left(\frac{8kT\varepsilon_{Si}}{q^2 n_i b^2}\right) + \log\left(\frac{(1+Ab^2)^2}{Ab^2}\right) + \frac{Ab^2}{1+Ab^2} = 0 \quad (6)$$

For a given V_{gs}, A can be solved from (6) as a function of V. Here V varies from the source to the drain, being V = 0 at the source end, and V = V_{ds} at the drain end. From this analysis we can obtain a charge control model relating the carrier charge density with the bias. The drain current in terms of the carrier charge densities is calculated from:

$$I_{ds-\text{int}} = \mu\frac{2\pi a}{L}\int_0^{V_{ds}} Q(V)dV \quad \text{and} \quad I_{ds-ext} = \mu\frac{2\pi b}{L}\int_0^{V_{ds}} Q(V)dV\ .$$

4. Gate Leakage Current, Noise Model and Short Channel Effects for CSDG MOSFET

In the proposed CSDG MOSFET devices with ultrathin gate oxide, direct tunneling is dominant mechanism of gate-leakage current. This current can be divided into six major (three due to internal gate and three due to external gate) contributions [12]: the gate to inverted channel current (I_{gc1} and I_{gc2}), the gate to source (I_{gs1} and I_{gs2}) and the gate to drain (I_{gd1} and I_{gd2}) components due to the path through the source and drain overlap regions. The gate-leakage current noise performances of a CMOS device can be characterized in terms of the gate noise current spectrum, which can be modeled by [13]:

$$S_P^2 = S_w^2 + \frac{A_{fg}}{f^{\alpha fg}} \quad (8)$$

where S_w describes the white noise component of the spectrum and A_{fg} is a power coefficient of the 1/f noise, α_{fg} determines the slope of this low frequency noise contribution, this second term shows the Flicker noise. The term S^2_w in (8) can be expressed by means of the shot noise law $S_w^2 = 2q(I_{g1} + I_{g2})$, where I_{g1} and I_{g2} are the sum of the absolute values of each gate current contribution for a given bias condition [14]. The thermal noise associated with the substrate resistance can produce measurable effects at the main terminals of the device. The thermal noise produced by the substrate resistance R_{sub} modulates the potential of the back-gate, contributing some noisy drain current of a MOSFET is given by:

$$i^2_{nd,sub} = 4kTR_{sub}g^2_{mb}\Delta f \quad (9)$$

But for the proposed CSDG MOSFET, bulk / substrate are not present, so $R_{sub} = 0$ which provides $i^2_{nd,sub} = 0$. Hence no noise is produced by the substrate resistance. In addition to the drain current noise, the thermal agitation of the channel charge has another important consequence as gate noise. The fluctuation channel potential couples capacitive into the gate terminal, leading to a noisy gate current. The noisy gate current may also be produced by thermally noisy resistive gate material. Although this noise is negligible at low frequencies, it can be dominate at radio-frequencies (RF). The conventional scaling

rules suggest that in order to minimize the short channel effects, the doping concentration of channel must be increased. However, a high doping level degrades the mobility and therefore lowers the drive current. Another possible alternative necessitates the reduction of gate oxide thickness. However, the extent to which gate oxide thickness can be scaled down is limited by direct tunneling [15, 16]. The CSDG MOSFET, which has greater control over the channel, was proposed in order to overcome these drawbacks as well as to offer high packing density and steep subthreshold characteristics. By reducing the thickness of silicon film of CSDG MOSFET, greater short channel immunity can be achieved. However, as the thickness of the silicon pillar is reduced, the current drive decreases thus presenting a serious limiting factor to the device performance.

5. Conclusion

We have presented an analytical model for undoped CSDG MOSFETs and provide the explicit solutions for the intermediate parameters that were used in previous DG MOSFETs models, which can be verified by numerical simulations. The model is based on a unified charge control model from which we derived a channel current expression in terms of the channel charge densities at the source and drain ends of the channel. The model becomes explicit by using appropriate expressions for the channel charge densities in terms of the applied voltages. The channel charge distribution in the silicon film is adequately accounted for in the charge control model. Besides, the channel current expression presents an infinite order of continuity over all operating regimes, which makes the model very promising for circuit simulation. In this proposed model, drain current, terminal charges, drain conductance, transconductance, and trans-capacitances can be expressed as explicit functions of applied voltages and structural parameters.

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