Designing a Future Value Stream Mapping to Reduce Lead Time using SMED-A Case Study

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Abstract

Many manufacturers struggle with improving productivity, producing the right products or services at the right place and meeting on-time delivery. To survive in today`s era competitive world, manufacturers need to find new ways to reduce the manufacturing lead times in order to improve productivity and operating principle. Nowadays, it is targeted to improve the productivity performance by reducing the production lead time and production waste that are the most important goals for almost all manufacturing companies. The main objective of this study is to design an efficient Value Stream Mapping (VSM) to improve the productivity in Small Medium Enterprise (SME) by eliminating non-value added activities. The methodology of the study is to firstly analyze the production waste in current state map, secondly to use the Kaizen activity with Single Minute Exchange of Die (SMED) to effectively support future state for process improvement of the action plan. As a conclusion, this paper presents that the designed Future Value Stream Map (FVSM) helps to effectively identify wasteful activities and production processes. VSM and Kaizen serve as an input for continuous improvement by reducing the manufacturing lead time using SMED in SME.

1. Introduction

The demand for smart tag is constantly increasing among the people in Malaysia. Smart tag is an Onboard Unit (OBU) vehicle-based device used as an Electronic Toll Collection (ETC) system over long distance to complement Touch n' Go. The central part of a smart tag product, which is a Printed Circuit Board (PCB) is manufactured in an

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automated assembly line. It includes several stations such as Surface Mounting Technology (SMT), reflow oven, Automatic Optical Inspection (AOI), and insertion process to place necessary electronic components onto the board. Smart tag manufacturing companies struggle to remain competitive in the global market and continuously finding a better way to cut down the production costs and increase the production volume. A cases study was conducted in domestic appliances production industry and trade incorporated Company to reduce the total lead time (LT) through eliminating non-value added activities [1]. Lean Manufacturing (LM) is an arrangement of technique and activities for running a production industries or service operation [2]. The first step to implement lean manufacturing tool in any organization is to apply Value Stream Mapping (VSM). A value stream is a combination of value added and non-value added activities that are required to bring a product through the essential flows; starting with raw material and ending with the customer for reducing the production wastes [3].

The objective of this study is to examine how VSM and Single Minute Exchange of Die (SMED) improves the quality of PCB production line in smart tag and reduce production cost and manufacturing LT. A future value stream map is then established to highlight the improved area and applied lean tools.

2. Literature Review

Lean Production System (LPS) is the systematic approach of identifying and eliminating all wastages through continuous improvement to pursuit customer satisfaction [4]. The primary goal of LPS is to reduce cost and improving productivity by eliminating major manufacturing waste in all work elements [5,13]. Application of the LPS was guided by five principles starting by 1-specifying value, 2-identifying the value stream, 3-making the value flow,4- configuring of pull system by customer, and 5-pursuing towards perfection [6,14]. LPS consists of a set of powerful "tools" that assisted in the identification and steady elimination of waste (Muda) such as VSM, 5S, SMED and standardized work [8.13]. These tools focused on certain aspect of a manufacturing process to eliminate waste and improve the quality while production time and cost were reduced [9]. VSM provides a tool to start the process improvement through a systematic approach [2]. The system approach to create VSM was divided into five basic steps [10]; 1- Create a current VSM, 2- Evaluate the current map, 3- identify problem areas, 4- Create a future state VSM, 5- Implement the final plan. VSM was created by William [11] to reduce waste in bread manufacturing in Zimbabwe. Samad [10] deployed VSM approach to reduce manufacturing LT by 50% from the current LT in a semi-automated factory in Texas. Venkatraman [12] applied VSM for reduction of cycle time from 135 seconds to 70 seconds in a crankshaft manufacturing system at an automotive plant located in south India.

3. Methodology

A case study as SME is considered, producing smart tag. PCB is focused, which is one of the major parts in smart tag where electronic components such as resistors, capacitors, transistors and others are inserted. The average monthly production of the company is 20016 units and the monthly working day is 24. Once order was delivered to the shop floor, operator unpacks the cartons of components and starts loading the components to the printing and solder paste machine. Then the PCB will move through SMT machines followed by the reflow oven. Operators will perform setup operations for the Screen Printing, SMT and Reflow oven machines prior to the loading of PCB.

The completed PCB will be inspected in AOI for any missing and faulty components by using a template. This inspection is monitored by an operator for the manual loading and unloading of PCB to the machine. The inspected PCB will then move to the next station which was a LED and buzzer mounting process followed by the Integrated Circuit Test (ICT) and Functional Test (FCT). Work in progress (WIP) of PCB was transported to different departments for testing and packaging. Before the packaging, the PCB will be assembled into the smart tag casing and proceed to the FCT. The packed smart tag units will then be shipped to the customer.

The methodology of implementing VSM in PCB assembly line is presented in Fig. 1.
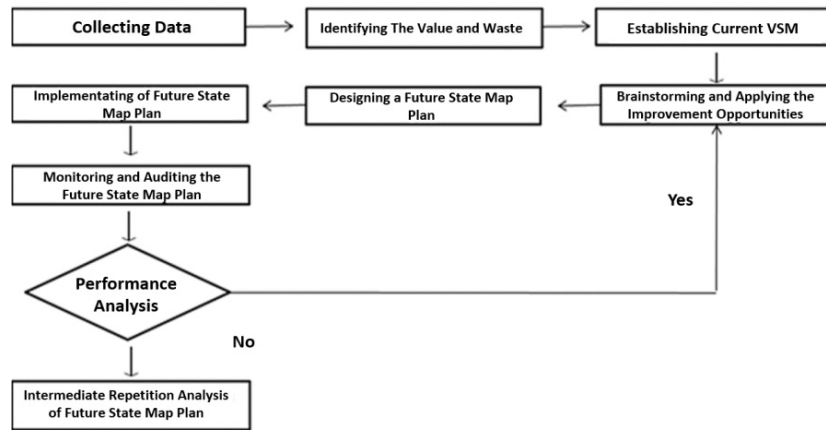
Fig.1 Methodology of implementing VSM in PCB assembly line

The 3G's (Gemba, Gembutsu, and Genjitsu) are used in this study to gather the data and information at the PCB assembly line for three months. Gemba conducted to study the production process flow and standard operation procedure of smart tag, which was selected before setting up the data collection. It then followed by conducting time study to collect and measure the relevant value stream data (Gembutsu). The measurements include the cycle time, processing time, changeover time, transportation time, queuing, handling time to establish the baseline for data analysis. Line observation (Genjitsu) is captured and quantified to identify the current value stream. The construction of Current VSM (CVSM) is based on Identifying the flow of materials and information in the actual PCB assembly line, and Transferring the collected data; (LT, cycle time, and changeover time), inventory, WIP materials, customer demand, and supplier information into current state map using the specific graphic symbols. The bottleneck of PCB assembly line is identified. CVSM is analyzed to identify the improvement opportunities. Future VSM (FVSM) is designed to provide guides for improvement activities. The FVSM plan includes essential actions to continuously improve the PCB assembly line by designing the lean flow including kaizen activities. All actions focused on improving the entire process by reducing waste. The monitoring of the PCB assembly line is examined before and after the implementation of the improvement process. The performance analysis is conducted to ensure that the effectiveness of future state map plan and line production is stable.

4. Results

Table 1 presents the summary of measurements at the PCB assembly line for three months.

Table 1. Time measurement at the PCB assembly line

Process Name	Printing and Solder Paste	SMT	Reflow oven	AOI	Insertion	ICT
Manual Cycle time (secs)	55.8	0	0	62.5	0	0
Machine Cycle time (secs)	5	47.3	20	7.5	87	3.9
Average Changeover/day	1	1	1	1	1	1
Changeover time (secs)	65	0	105	0	145	0
Batch Size	300	300	300	300	300	300
[1]Effective Cycle Time (secs)	61.0	473	20.4	70	89.5	3.9
WIP Inventory	0	0	0	0	144	0
Available time (secs)	72000	72000	72000	72000	72000	72000
[2]Uptime	99.91%	100%	99.85%	100%	99.80%	100%

[1]Effective Cycle Time = manual cycle time + machine cycle time+ (changeover time/ batch size)
[2]Uptime = (available time- changeover time of each process/day) / available time × 100%
    Where available time for each process = net operation time- break time – setup time = 2 shifts × (12-1.5-0.5) × 3600 = 72000 sec
Takt time = time available (per shift) divided by the customer demand = Takt time = 72000 secs/834 = 86.33 secs.

4.1 Current VSM

Fig. 2 shows CVSM by adding timeline at the bottom of the map to calculate the LT and the value added time.
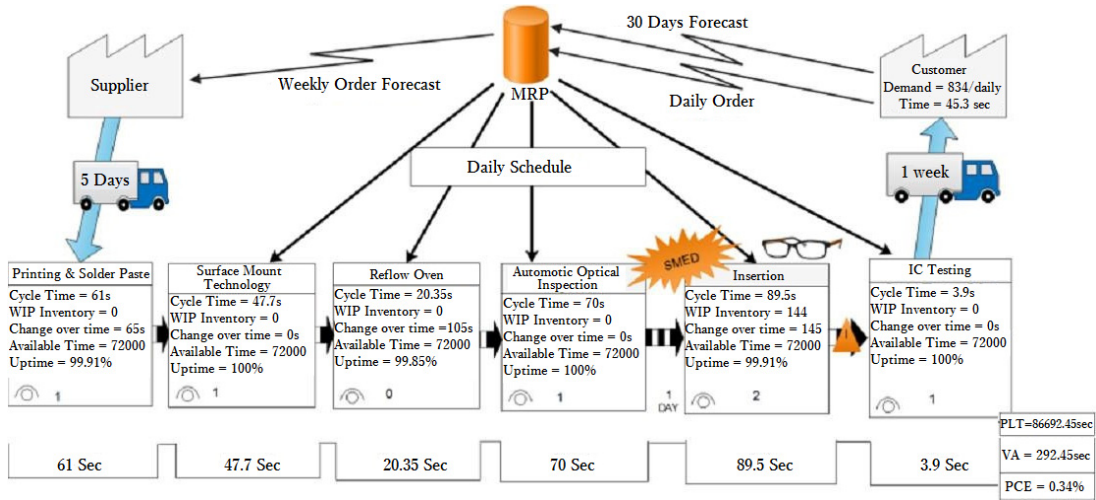

Fig.2. Current value state map

The insertion process has the highest changeover time. It is the bottleneck at the PCB assembly line as it's cycle time is 89.5sec (exceed the takt time=86.33sec). In current practice, all 13 internal activities during the setup for SMT at the insertion process are performed while the machine is not running. SMED and quick changeover are performed on SMT at the insertion line by separating the internal from external setup operations, converting internal to external setup, and adopting parallel operation. After the implementation of SMED, number of setup tasks with respect to cast on strap were reduced from 13 to 7 tasks (see Table 2), which results 63% reduction in changeover.

Table 2 Tasks after SMED implementation

N0.	Task	Before SMED(secs)	After SMED (secs)		
		Time taken	Internal	External	Parallel
1	Peel off tape[I]	10	10		
2	Tape used to hold PCB width using settling belt[P]	4			4
3	Machine power is switched off[I]	10	10		
4	Machine power switched back on[E]	10		10	
5	rewind tape leader signal cable[P]	8			8
6	rewind PG tape[E]	26		26	
7	set PCB on loader[I]	10	10		
8	turn machine power on[E]	10		10	
9	check contact of No1 device on coating head side[I]	2	2		
10	use satellite operation panel to adjust position[E]	30		30	
11	check contact of No 1 device on mount head side[I]	5	5		
12	use satellite operation panel to adjust position[P]	15			15
13	check for slippage after first contact[I]	5	5		
	Total	145	42	76	27

I=Internal setup, E= External setup, P = Parallel operation

4.2 Future VSM after the Implementation of Kaizen Activity

Fig. 3 shows the future VSM after the implementation of FVSM plan and Kaizen activity.
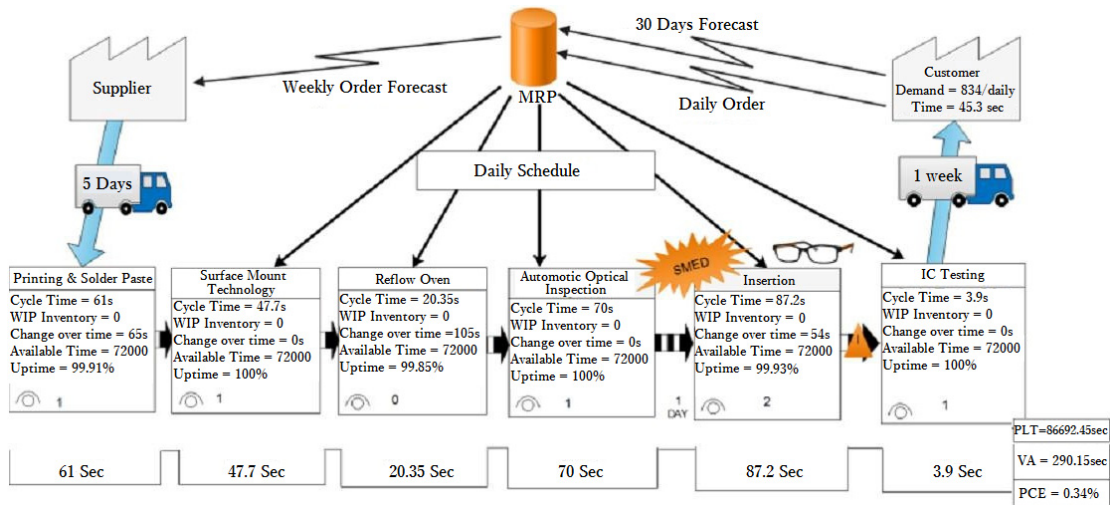
Fig.3. Future Value Stream Mapping

Table 3 shows the comparison between before and after the implementation of SMED at insertion process.

Table 3. Before and after the implementation of SMED

	Before SMED	After SMED
Cycle time (secs)	89.5	87.2
WIP Inventory	144	0
Changeover time (secs)	145	54
Available time (secs)	72000	72000
Uptime	99.83%	99.93%

5. Conclusion

This study has shown the implementation of VSM in PCB assembly line to reveal obvious and hidden waste that affected the productivity of smart tag production. This hidden waste was related to the high changeover time at the insertion process of PCB assembly line and induced high WIP. Improvement process is designed to reduce the WIP and lead time using SMED and Kaizen techniques. The SMED technique was implemented at the insertion process that was bottleneck. SMED technique was successfully implemented because the machine setup time in the insertion process was reduced from 145 seconds to 54 seconds. This study recommends that the insertion process might be converted from batch operation to continuous flow operation to reduce more wastes.

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