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Observation of geometry induced doping in thin Si nano-grating layers

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Abstract

We fabricate Si nano-grating layers and measure their electrical characteristics to monitor geometry induced doping. SOI device layer was thinned down by thermal oxidizing and subsequent wet etching of the oxide. Grating was fabricated using laser interference lithography (375 nm laser) followed by reactive ion etching of Si. Next, large square island (0.5x0.5 mm) was shaped in the device layer and four Si\Ti\Ag ohmic contacts were formed to measure electrical characteristics. The I-V characteristics were recorded using both 4 wire and 2 wire methods. Resistance-temperature dependences (T= 4-300 K) were recorded as well. For all 12 samples, nano-grating layers show 2-3 order reduction of resistivity. Resistivity anisotropy was in the range 0.2-1 at 300 K. Obtained geometry induced doping level corresponds to “effective impurity” concentration of $3x10^{18}$ cm^{-3}. The dependence is in agreement with G-doping theory only below T=150K.

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Keywords: nanostructuring; nano-grating; electronic structure; doping

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1. Introduction

Developments in nanotechnology have enabled the fabrication of densely packed periodic structures [1-3]. At the same time, nano-grating (NG) has been shown to dramatically change electronic [4], thermoelectric [5] and electron emission properties [6] when the grating pitch becomes comparable with the electron's de Broglie wavelength. This is due to the special boundary conditions imposed by NG on the electron wave function. Supplementary boundary conditions forbid some quantum states, and the density of quantum states (DOS) is reduced (in all bands). Electrons rejected from NG-forbidden quantum states have to occupy empty states with a higher energy. Fermi energy increases, and the electronic properties of the NG layer change. In the case of semiconductor materials, electrons rejected from the valence band (VB) occupy empty quantum states in the conduction band (CB). Electron concentration n in the CB increases, which can be termed as geometry-induced electron doping or G-doping. G-doping is equivalent to donor doping from the point of view of the increase in n and Fermi energy. However, there are no ionized impurities. This maintains charge carrier scattering to the intrinsic semiconductor level and increases carrier mobility with respect to the donor-doped layer of the same electron concentration. G-doping is temperature independent because it originates from layer geometry and no ionized impurities are involved.

Other methods of doping without impurities include the well-known modulation doping and the recently introduced polarization doping [7]. Both are 2D in nature. However, a 3D approach to modulation doping was introduced in [8] to improve the thermoelelectric characteristics of nanocomposites [9, 10].

Related quantum systems, such as the narrow-wide-narrow geometry quantum wire [11], periodic curved surfaces [12, 13], electron waveguides [14], and strain-driven nanostructures [15], have also been investigated.

Fig. 1 shows a typical cross-section of a Si nano-grating layer. The grating on the surface has depth a and pitch $2w$. For comparison, we choose as a reference layer a planar layer with thickness H, such that it has the same cross-sectional area. The NG layer is a quasi-1D system in the range $0<a<2H$. The NG layer is a 2D quantum well for $a=0$ and a system of 1D quantum wires for $a=2H$ [16].

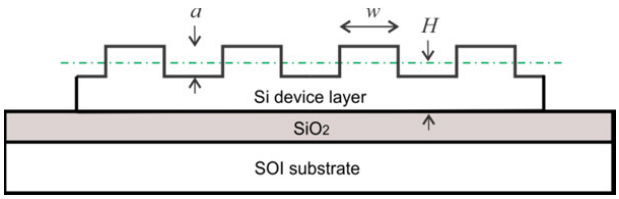

Fig. 1 shows a typical cross-section of a Si nano-grating layer.

The objective of this work is to experimentally investigate electronic properties of Si nano-grating layers and find out how they are dependent on layer dimensions and temperature. First, we describe sample preparation and experimental methods (Sec. 2). Next, we present experimental results in Sec. 3. Finally, we discuss obtained results in Sec. 4. In Sec. 5, our conclusions are summarized briefly.

2. Sample preparation and characterization

Both buried oxide (BOX) and transferred layer SOI substrates were used for sample preparation. BOX layer SOI substrate (Soitech) device layer thickness was 70 nm. Layer was slightly p-type doped (Boron) with resistivity 8.5-11.5 Ohm cm. BOX thickness was 150 nm. BOX layer SOI substrate (supplied by company "University wafer") device layer initial thickness was 250 nm. Layer was slightly p-type doped (Boron) with resistivity 14-22 Ohm cm. BOX thickness was 3000 nm. Transferred layer SOI substrate (Ultrasil Corp.) device layer initial thickness was 1500 nm. Layer was very slightly p-doped (Boron) with resistivity >5000 Ohm cm. Oxide thickness was 500 nm.

Transferred layer SOI device layer was thinned down to 70-100 nm by thermal oxidizing and subsequent wet etching of the oxide. Device layer was oxidized in wet oxygen and dry oxygen. When oxidized in wet oxygen they were heated up to 1150 C for 40 minutes resulting in removal of 230 nm of Si from device layer after wet etching.

When thinned down in dry oxygen they were heated up to 1000 C for 40 minutes to remove 50 nm of Si from device layer after wet etching. Wet etching of the oxide was done in HF+H_2O (1:20) during 20-30 seconds. From 2 to 10 iterations were needed to thin device layer down to 70-110 nm. Surface roughness was monitored using AFM during the thinning process. RMS of maximum 0.7 nm was measured on thinned layer surface. Initial RMS was in the range 0.3-0.5 nm.

Fig.2 shows simplified process for sample preparation:

A) NG was fabricated in the center of 8x10 mm chip using laser interference lithography [17, 18] and subsequent reactive ion etching of Si. To prepare samples for interference lithography, SOI substrates were processed in the solution H_2SO_4 + H_2O_2 + H_2O (1:1:3) for 5-10 minutes. Next, they were cleaned in deionized water for 10 minutes and dehydrated on the centrifuge. Next, they were passivated in HF + H_2O (1: 20), washed in demonized water during 10 minutes, dehydrated on the centrifuge and hotplate at 180 C during 20 min. Next, negative photo resist ma-N 2401 was applied at 4000-4200 rpm during 30 seconds, resulting in resist thickness of 70-90 nm. Finally, Resist was dried at 90-115 C during 10 minutes.

Laser interference lithography setup is shown in Fig. 3. Blue-Violet (375 nm) semiconductor laser DL375-010-SO was used as coherent (coherence length >20 meters) light source. Laser beam with diameter 1.2 mm was focused by the lens and aimed at 50 micron diameter pinhole. Obtained beam was directed to Lloyd interfetometer which consisted of mirror and substrate aligned at 90 degrees and mounted on rotating table. Light coming directly from the pinhole interfered with light reflected from the mirror and formed interference fringes at the substrate. Fringe width varied from 120 nm to 1000 nm depending on angle set by the rotating table. Resist exposition time was 10-25 seconds. After exposition, resist was developed in alkaline solution AZ-400K + H_2O (1:3) during 2-35 seconds.

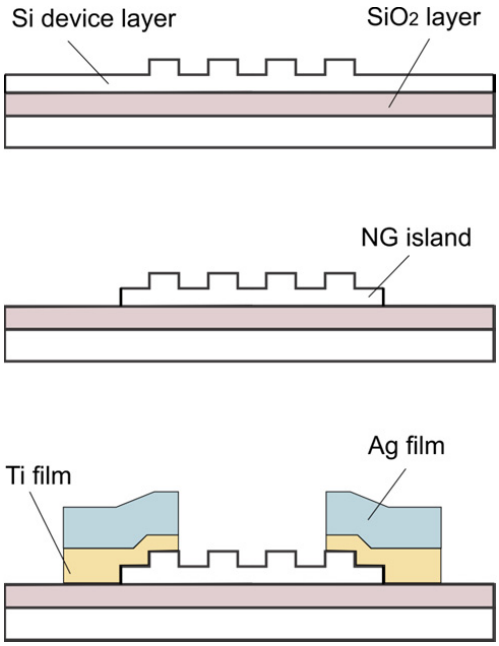

Fig. 2. Sample preparation process flow (simplified). a) NG fabrication using laser interference lithography; b) Shaping of 0.5x0.5 mm island in the device layer; c) Deposition of Ti and Ag film for ohmic contacts.

Reactive ion etching was done in CF_4 at P=6-7x10^{-2} Pa, V=3.8-4.2 kV and I =200 mA. Etching time varied from 6 minute to 20 minutes depending on etching depth. Surface roughness measured after etching did not exceed RMS=1 nm.

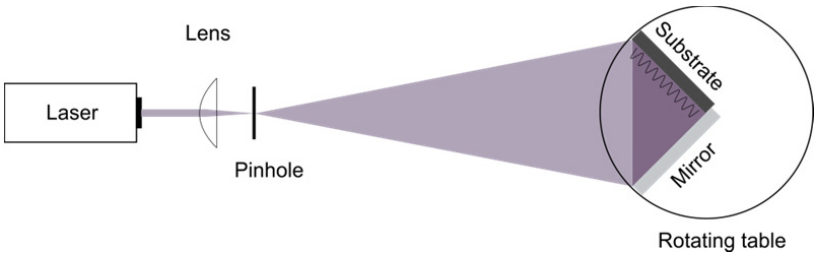

Fig. 3. Laser interference lithography setup.

B) Square island 0.5x0.5 mm was formed in the NG device layer using photo lithography. Positive photo resist AZ-5412? was applied at 3200-3500 rpm during 30 seconds. Resist thickness was 0.8 micron. It was backed at 90 C during 60 seconds. After exposure during 35-40 seconds, resist was developed in AZ-400K + H_2O (1:4) during 25-40 seconds. Next Si was etched by reactive ion etching until SiO_2 layer was reached (20 minutes).

C) Ohmic contacts were made by Ti\Ag deposition through Mo mask. Films were grown using DC magnetron sputtering in the same vacuum process at substrate temperature 250 C. The Ag gas pressure was $1\text{-}3x10^{-1}$ Pa. The Ti film 30-40 nm was grown at V = 400-450V, I=1±0.1A during 15-20 seconds. The Ag film 1000 nm was grown at V = 450-500V, I = 0.6±0.1A during 60 seconds.

Current-Voltage characteristics were recorded using both 4-wire Van der Pauw method (4W) and 2-wire method (2W) along (=) and across (+) the grating. Using of 2-wire method was necessary as 4-wire method do not gives sufficient information for anisotropic (grating) layers.

Resistance temperature dependences were recorded using Physical Property Measurement System PPMS (Quantum Design). Both resistance along the grating $R_=$ and resistance across the grating R_+ temperature dependences were recorded in the range T=4-300 K.

Carrier type was determined from straightforward thermoelectric measurements. For this, one of the Ti\Ag contacts were heated up to 150 C using temperature controlled soldering machine and the sign of voltage generated between hot and cold contacts was monitored using high input impedance multimeter. Measured voltages were in millivolt range.

3. Result and discussion

Nano-grating reduces resistivity in all samples. Table 1 shows measured values for resistance along the grating , $R_=$ resistance across the grating R_+, resistance anisotropy $R_= / R_+$ and resistivity (calculated based from $R_=$ 4W) for 12 nano-grating samples. In addition, 2 reference samples with plain layers (S32 ref. and S ref.) are included in Table 1 for comparison.

Nanograting reduces resistivity to approximately 10^{-2} Ohm cm, almost independent of initial resistivity (>5000 Ohm cm, 8.5-11.5 Ohm cm, 12-14 Ohm cm) and SOI wafer type (BOX or transferred layer). Most samples show resistance anisotropy which varies in the range of 0.2–1. Resistance along the grating is always less than across the grating. Increased pitch sample (S114) shows more resistance anisotropy. Both 4W and 2W I-V characteristics (Fig. 4) of NG layers are linear indicating good quality of ohmic contacts. 4W resistances of NG layers are 5-10 times lower than 2W resistances. This is common for square shape of measured area. I-V characteristics of plain layers (S32 ref. and S fer.) were nonlinear. This was expected as plain layer resistivity is too high (>5000 Ohm cm and 8.5-11.5 Ohm cm) to form good ohmic contacts.

Table 1. Experimental data for SOI nano-grating samples

#	*H* [nm]	*a* [nm]	*w* [nm]	$R_=$ 4W [kOhm]	$R_=/R_+$ 4W	$R_=$ 2W [kOhm]	$R_=/R_+$ 2W	Initial resistivity [Ohm cm]	G doping resistivity [Ohm cm]
S32	100	30	150	4.3	1.0	31	0.7	>5000	$4.3x10^{-2}$
S88	58	24	150	9.5	0.9	50	0.89	8.5-11.5	$5.5\ x10^{-2}$
S89	55	30	150	3.26	0.83	20	0.82	8.5-11.5	$1.8\ x10^{-2}$
S100	63.8	12.5	150	1.55	0.62	15.3	0.98	8.5-11.5	$1.0\ x10^{-2}$
S101	60	20	150	1.43	0.90	15	0.83	8.5-11.5	$0.8\ x10^{-2}$
S104	60	20	150	1.28	0.83	9.7	0.78	8.5-11.5	$0.8\ x10^{-2}$
S105	60	20	150	5.4	1.0	36.5	0.90	8.5-11.5	$3.2\ x10^{-2}$
S106	60	20	150	3.5	1.0	23.7	0.87	8.5-11.5	$2.1\ x10^{-2}$
S107	51	38	150	1.6	0.86	8.5	0.89	8.5-11.5	$1.0\ x10^{-2}$
S108	58.5	23	150	2.3	0.54	26	0.97	8.5-11.5	$1.3\ x10^{-2}$
S114	60	20	250	2.43	0.2	24.5	0.7	8.5-11.5	$1.0\ x10^{-2}$
S124	96.5	21.5	150	4.5	0.76	25.3	0.84	14-22	$4.15\ x10^{-2}$
S32 ref.	110-120	0	-	2.500 -3500*	-	10000--15000*	-	>5000	-
S ref.	70	0	-	540--3900*	-	10000--19000*	-	8.5-11.5	-

*I-V is diode type

Our explanation of such a dramatic reduction in resistivity is based on G-doping [4]. Nano-grating on the surface of the thin layer imposes additional boundary conditions on the electron wave function and reduces Density of Quantum States (DOS) which induces G-doping or geometry doping. G-doping is equivalent to donor doping from the point of view of the increase in electron concentration. However, there are no ionized impurities. G-doping resistivity value 10^{-2} Ohm cm corresponds to conventional n-type doping "impurity" concentration of $3x10^{18}$ cm^{-3} (example of phosphorus in Si) [19]. This indicates that G-doping effect is quite strong even in the gratings having relatively large pitch (300 nm).

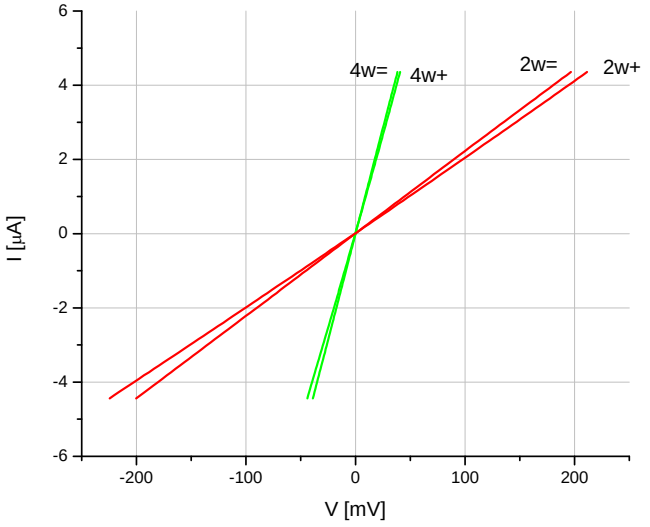

Fig. 4. The I-V characteristics of sample S88 recorded at T=300 K. = depicts resistance along the grating and + depicts resistance across the grating.

To verify G-doping type we determined the type of charge carriers. For this, the sign of thermoelectric voltage generated by G-doped layers were compared to the sigh of thermoelectric voltage generated by conventionally (Boron) doped SOI device layers of same thickness. Thermoelectric measurements show that electrons are charge carriers in the case of G-doping. This is in agreement with prediction of G-doping theory.

Resistivity of n-type semiconductor is determined from well known expression

$$\rho = 1/e\,\mu\,n, \tag{1}$$

where e is the electron charge, μ is the electron mobility and *n* is the electron concentration. Observed decrease of NG layer resistivity (Table I) can be caused by increase in both μ_e and *n*. G-doping increases μ_e depending on geometry factor. Last is caused by reduction of DOS in nano-grating geometry. Calculation of DOS predicts that it reduces 1-5 fold [20]. Such reduction of DOS results in a proportional decrease of electron scattering rates (Fermi Golden Rule) and corresponding increase of electron mobility [21]. Consequently, we expect 1-5 fold increase in μ. The rest of increase 200-1000 fold can be attributed to increase of *n*.

Both *n* and μ_e are temperature dependent. G-doping $n(T)$ differs from corresponding dependence for donor doped Si. G-doping results in $n = \text{const}$ [4]. Donor doping results in well known dependence $n \sim (T)^{3/4} \exp[-(E_C - E_D)/2K_BT]$ [19]. Regarding μ it is $\mu_l \sim T^{-3/2}$ for acoustic phonons and $\mu_i \sim T^{3/2}$ for impurity scattering [19]. G-doping $\mu(T)$ do not differs from acoustic phonon $\mu(T)$ as soon as geometry factor is temperature independent [21]. Inserting above formulas in Eq. (1) we get:

$$\rho_G(T) \sim T^{3/2}, \tag{2.1}$$

$$\rho_D(T) \sim T^{-2.25} \exp[(E_C - E_D)/2K_BT]. \tag{2.2}$$

where ρ_G is G-doping resistivity and ρ_D is donor doping resistivity. Obviously, G-doping and donor doping result in a very different resistivity temperature dependences. We compare measured data to Eq. (2) and Eq. (3) to get more information from our samples.

Resistance-temperature dependence in the range T=4-300 K were recorded for S32. Corresponding resistivity $\rho_=(T)$ and $\rho_+(T)$ are shown in Fig. 5. For comparison, we plot theoretical curves according to Eq. (2.1) and Eq. (2.2). In Eq. (2.2), $E_C - E_D = 0.046$ eV was inserted which corresponds to phosphorus donor impurities in Si.

Resistivity-T dependences $\rho_=(T)$ and $\rho_+(T)$ are close to each other and $\rho_=(T)$ is a little bit lower as expected (Table I). Below 150 K both $\rho_=(T)$ and $\rho_+(T)$ approximately follow $\sim T^{3/2}$. This is in a good agreement with G-doping theory. However, in the range 300-150 K both $\rho_=(T)$ and $\rho_+(T)$ are far from $\sim T^{3/2}$. This can be explained by transport electron scattering on the nanograting. For high temperatures electron mean free path $\lambda_m \approx 40$ nm (at T=300) is less than half pitch and electron scatters on nano-grating. When T is reduced to 100 K mean free path increases to $\lambda_m \approx 300$ nm [22]. When λ_m exceeds half pitch (150 nm) of the nanograting, transport electron begins to interact with nanograting as coherent wave and ignores it by diffraction. This mechanism can lead to increase of electron mobility and corresponding reduction in resistivity below 100 K. Experimental dependences are very far from impurity doping case $\sim T^{-2.25} \exp[(E_C - E_D)/2K_BT]$. This is natural as we use very lightly doped device layers $\rho_0 \approx 10$ Ohm cm.

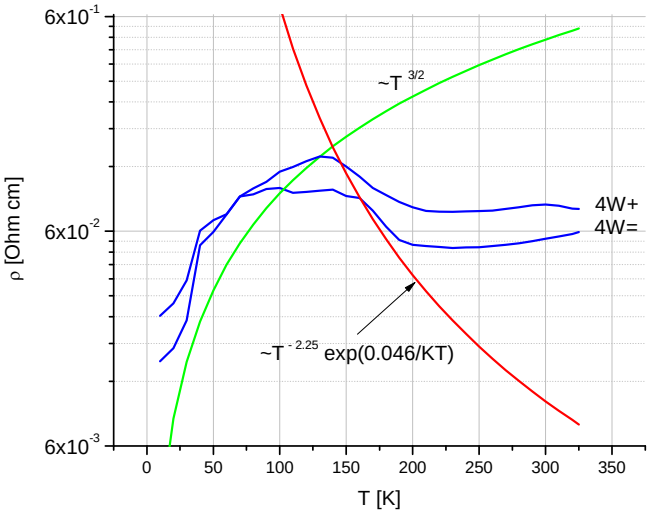

Fig. 5. The 4W Resistivity of S88 along (=) and across (+) the grating. Green curve corresponds to G doping Eq. (2) and red curve corresponds to donor doping (phosphorus impurities in Si).

4. Conclusions

It was observed (data from 12 samples) that nano-grating reduces resistivity of Si layer from 10 Ohm cm (plain layer) to $5x10^{-2}$ - $8x10^{-3}$ Ohm cm. This reduction is in agreement with theoretical prediction of G-doping in nano-grating layers. Value 10^{-2} Ohm cm corresponds to "impurity" concentration of $3x10^{18}$ cm^{-3} (phosphorus in Si). Both 4W and 2W I-V characteristics were linear indicating good quality of ohmic contacts. 4W resistances of NG layers were 6-10 times lower than 2W resistances, which is common for square area. Most samples show resistivity anisotropy which varied in the range of 0.2–1. Resistivity was always less along the grating. Increased pitch sample (S114) shows more resistance anisotropy. Resistivity temperature dependence matches G-doping theory only below 150 K. G-doping do not requires ionized impurities. This allows high carrier mobility and temperature independent carrier concentration. Such layer fabrication does not require sophisticated technology and can be used for solar cells and other photovoltaic devices, ultra high frequency electronics, and power electronics.

Acknowledgments

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References

[1] Wang L., Terhalle B., Guzenko VA., Farhan A., Hojeij M., and Ekinci Y. "Generation of high-resolution kagome lattice structures using extreme ultraviolet interference lithography," Appl. Phys. Lett. 101 (2012) 093104.

[2] Sreekanth KV, Chua JK, Murukeshan VM (2010) Interferometric lithography for nanoscale feature patterning: a comparative analysis between laser interference, evanescent wave interference, and surface plasmon interference. Appl Optics 49:6710–6717

[3] Liu Q., Duan X., Peng C., Novel Optical Technologies for Nanofabrication, Nanostructure Science and Technology, Ed. D. J. Lockwood, Springer-Verlag Berlin Heidelberg 2014
[4] Tavkhelidze A., Geometry-induced electron doping in periodic semiconductor nanostructures, Physica E 60 (2014) 4.
[5] Tavkhelidze A., Large enhancement of the thermoelectric figure of merit in a ridged quantum well, Nanotechnology 20 (2009) 405401.
[6] Tavkhelidze A., Nanostructured electrodes for thermionic and thermo-tunnel devices, J. Appl. Phys. 108 (2010) 044313.
[7] Simon J., Protasenko V., Lian C., Xing H. and Jena D., , Science 327 (2010) 60-64.
[8] Zebarjadi B, Wang H., Lukas K., Wang D., Opeil C., Dresselhaus M., Chen G., and Ren Z., , Nano Lett. 12 (2012) 2077.
[9] Goldsmid HJ., Introduction to Thermoelectricity, Springer, 2010.
[10] Birkel CS., Claudio T., Panthoefer M., Birkel A., Koll D., Kieslich G., Schmidt J., Hermann R., and Tremel W.. Phys. Stat. Solidi A 208 (2011) 1913.
[11] Nonoyama S., Honma Y., Nakamura A., Phys. Lett. A 379 (2015) 979.
[12] Ono S., Shima H., Physica E 42 (2010)1224–1227.
[13] Kartashov YV., Szameit A., Keil R., Vysloukh VA., Torner L., Opt. Lett. 36 (2011) 3470.
[14] Ban Yue, YaSherman E., J. Appl. Phys. 113 (2013) 043716.
[15] Ortix C., Kiravittaya S., Schmidt OG., Vanden Brink J., Phys. Rev. B 84 (2011) 045438.
[16] Kakulia D. , Tavkhelidze A., Gogoberidze V., Mebonia M., Density of quantum states in quasi-1D layers, Physica E: Low-dimensional Systems and Nanostructures, 78, (2016) 49-55.
[17] Henk van Wolferen, Leon Abelmann, Laser Interference Lithography, In “Lithography: Principles, Processes and Materials” Ed. Theodore C. Hennessy, Nova Science Publishers 2011.
[18] Corey P. Fucetola, Hasan Korre, and Karl K. Berggren, Low-cost interference lithography, J. Vac. Sci. Technol. B 27, (2009) 2958.
[19] Sze SM. and Ng K.K., Physics of Semiconductor Devices, New Jersey: Wiley-Interscience, 2007.
[20] Kakulia D. , Tavkhelidze A., Gogoberidze V., Mebonia M., Density of quantum states in quasi-1D layers, Physica E: Low-dimensional Systems and Nanostructures, 78, Pages (2016) 49-55.
[21] Tavkhelidze A. and Svanidze V., Quantum state depression in a semiconductor quantum well, International Journal of Nanoscience, Vol. 7, No. 6, (2008) 333-338.
[22] Weber L.and Gmelin E., Appl. Phys. A 53, (1991) 136-140.