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Sub-micron SNIS Josephson junctions for metrological application

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Abstract

The overdamped Nb/Al-AlOx/Nb superconductor-normal metal-insulator-superconductor SNIS Josephson junctions recently developed at INRIM exhibit high values of critical current density and characteristic voltage, making these devices appealing both for metrology and digital electronics. High current densities could allow reduction of junction size, increasing the integration level.

In this work authors present first results concerning the realization of sub-μm SNIS including a nanolithographic technique (Electron Beam Lithography, EBL) into the conventional process, to reduce junction dimensions. Fabrication and electrical parameters have been evaluated considering the scaling of the areas of junctions, furthermore RF and temperature behaviour have been studied.

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1. Introduction

The demand of reducing Josephson junction dimensions down to sub-micron scale occurs in several application fields. In superconducting digital electronics the rising of clock frequency, a reduction of capacitance values and a higher integration density for electronic circuits are some of the main requirements strictly linked to lower dimensions.

In voltage standard metrology, the characteristic voltage $V_c$ ($V_c = I_c R_n$, being $I_c$ the critical current and $R_n$ the normal resistance of the junction) determines the microwave optimal drive frequency thus the step voltage and the number of junctions needed to define the maximum output voltage. In this context an increase of critical current density could entail a gain in term of size reduction. Sub-micron Josephson junctions are especially required in pulse driven arrays employed in the Josephson arbitrary waveform synthesizer, where a train of pulses is used to generate AC voltages with fundamental accuracy. The most reliable solution to guarantee pulse operation is to reduce array dimensions below a length shorter than $\lambda/8$, where $\lambda$ is the wavelength of the microwave signal [1, 2].

The overdamped Nb/Al-AlO$_x$/Nb SNIS Josephson junctions recently developed at INRIM exhibit high values of critical current density and characteristic voltage. In this technology a thick aluminum metal layer and a thin insulating oxide layer represent the tunneling barrier.

Recently, 1 V binary-divided arrays based on SNIS Josephson junctions have been realized for programmable Josephson voltage standards [3]. These arrays, consisting of 8192 overdamped Nb/Al–AlO$_x$/Nb SNIS junctions, were successfully operated at microwave frequencies around 70 GHz and operation at temperatures up to 6 – 7 K has also been verified, measuring quantized voltages up to 1.25 V on the $n = 1$ step.

The realization of sub-micron junctions according to the INRIM fabrication process, added to the peculiar features mentioned above, could represent a interesting challenge making these devices appealing both for metrological applications and digital electronics.

2. SNIS fabrication process

Overdamped Nb/Al–AlO$_x$/Nb SNIS Josephson junctions are fabricated starting from a revisited SIS trilayer process [4] by properly oxidizing, in-situ and without breaking the vacuum, the aluminum barrier in pure oxygen ambient. The aluminum thickness and the oxidation time determine the proper internal shunt of a SNIS junction and a transition from a hysteretic to a non-hysteretic current-voltage I-V characteristic. This transition has been also observed increasing the operating temperature [5, 6].

SNIS junctions can be fabricated trimming a wide range of electrical parameters, showing critical current density values $J_c$ from less than 1 kA·cm$^{-2}$ up to $10^5$ A·cm$^{-2}$, and $V_c$ easily tuned from 0.1 to 0.7 mV at 4.2 K, and referring to a typical SNIS junction size of 5x5 $\mu$m$^2$ realized by optical lithography.

For this work the aluminum thickness of the barrier was about 50 nm, being subject to an oxidation exposure dose ranging from 160 to 200 Pa·s. The effective area of SNIS has been defined exploiting a nanolithographic technique (Electron Beam Lithography, EBL) by using a FEI Quanta 3D ESEM FEG equipped with a J. C. Nabity NPGS pattern generator. The process has been carried out with a very thin negative e-beam resist (ma-N2400 series by Microresist Technology), and optimizing the e-beam exposure dose with the scaling of dimensions.

The first aim was to validate the standard INRIM process at sub-micron level, using the same techniques exploited at the micrometric scale. In particular, since the e-beam resist is considerably thinner than the optical one and less stable during etching processes, the Reactive Ion Etching (RIE) and
anodization steps have been adapted and calibrated as a function of patterned dimensions by EBL, in order to preserve the resist.

Starting from a 5x5 μm² area down to 0.7x0.7 μm² both the RIE, used to remove the niobium top electrode in excess, and the anodization have been properly optimized. During the sputtering deposition, the thickness of the top layer was reduced from the usual 120 nm value to 50 nm, in order to drastically lower the etching time during reactive ion etching, from 10 to 3 minutes at 100 W. Figure 1 shows the SEM images of two SNIS junctions fabricated by electron-beam lithography, with the wiring layer on top.

The standard anodization, performed to avoid short circuits between the two superconducting junction electrodes, has been carried out paying attention to the current density ($8 \times 10^4 \text{ A cm}^{-2}$), so limiting under etching and/or under anodization effects.

A traditional optical lithography has been lastly exploited to define the trilayer layout, the wiring and the contact pads.

![SEM images of SNIS junctions](image)

Fig. 1. Scanning electron microscope (SEM) photographs of (a) 1 μm² and (b) 3 μm² SNIS junctions fabricated by electron-beam lithography, with Nb wiring on top.

### 3. Electrical characterisation

Electrical parameters of Josephson junctions fabricated by EBL have been measured and analyzing the DC I-V characteristics a proper scaling of current densities has been observed. In figure 2 the IV curve of a 1 μm² and a 3 μm² SNIS are shown, with critical current values of about 2.1 mA and 5.25 mA, respectively.

Moreover, magnetic field patterns were carried out for several junctions to validate techniques employed in the framework of the usual process. They were performed on 0.7x0.7 μm² and on 1 μm² junctions. As shown in the inset in the figure 2 (a), the experimental data show a zero value of critical current at 185 Gauss. This confirms the absence of short circuits into the barrier and in the anodic oxide, assessing the high quality of the junctions, and it is well related to junction dimensions and current density.
Fig. 2. Current – voltage characteristic referred to (a) $1 \mu m^2$ and (b) $3 \mu m^2$ SNIS junctions defined by EBL. The inset in the figure (a) represents the magnetic pattern of the junction.

The RF and temperature behaviours have been also analyzed. Due to the peculiar high characteristic voltages, high order steps are enhanced. Irradiating a $1 \mu m^2$ SNIS with a $V_c = 670 \mu V$, Shapiro steps have been measured up to $n = 7$ at 4.2 K (Fig. 3 (a)). This feature allows operating near the niobium critical temperature. The $n = \pm 1$ Shapiro steps have been optimized at about 7 K (Fig. 3 (b)), confirming the interest to use the SNIS junctions at higher operating temperatures.

Fig. 3. Quantized voltage steps for a $1 \mu m^2$ single junction with a $V_c = 670 \mu V$, measured with a frequency of 69.78 GHz at (a) 4.2 K and (b) at 6.7 K. The inset in the figure (a) shows the $n = 7$ step at 4.2 K, due to the high $V_c$ value.
4. Conclusion

We have scaled the typical SNIS junction size (5x5 $\mu m^2$) down to the submicron level and the magnetic pattern confirmed the absence of short circuits into the barrier and in the anodic oxide, so validating the fabrication process.

A proper scaling of junction current densities has been observed and quantized Shapiro steps have been measured also at the temperatures of about 7 K. Therefore this class of junctions could be used at temperature above 4.2 K in a cryocooler set up for AC voltage standards.

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