
Optimization of Underlap Length for DGMOSFET and FinFET

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Abstract

From the commencement of CMOS scaling, the simple MOSFETs are not up to the performance due to the increased SCEs and leakage current. To slacken the SCEs and leakage currents, different types of structures i.e. Multi-Gate MOSFETs like DG, TG, FinFETs are introduced. Currently the Integrated Device Manufacturer (IDM), foundries and electronic design automation (EDA) companies grant more investments and emphasis on most promising Multi-Gate technology. In this, sensitivity of underlap length on DC and AC parameters like drain current, SS, transition frequency, delay, EDP etc. is studied for both the chosen devices i.e. DG MOSFET and FinFET. From our reported results, DG MOSFET is a good candidate for high current drivability whereas FinFET provides better immunity to leakage currents and hence improved delay, EDP over DG MOSFET. Furthermore, FinFET provides high value of transition frequency which indicates that it is faster than DG MOSFET.

Keywords: underlap length; DG; FinFET; EDP; delay; transition frequency.

1. Main text

Scaling of planar FET's has sustained to provide performance, power, and circuit density improvements up to the 22nm process node. Although deedful pioneering on FinFET devices has been ongoing for more than a decade, their use by a production fab has only recently gained adoption.

As scaling into submicron region, Short Channel effects inhibit further scaling like DIBL, threshold voltage roll off etc. occurs in single gate MOSFET. FinFET is the prime candidate which have excellent control over channel in submicron region and making transistors still scalable. In order to overcome SCEs and leakage
current, different device Multigate MOSFETs (Mug-FET) structures like Double gate, Tri gate, FinFET were proposed [1][2].

The transistor channel width of one FinFET is outlined by the fin width $W_{\text{Fin}}$ and fin height $H_{\text{Fin}}$. In many cases, especially when $H_{\text{Fin}}$ is at least twice $W_{\text{Fin}}$, the FinFET can be considered a DG transistor where the channel width can be considered $H_{\text{Fin}} + W_{\text{Fin}}/2$, and for this reason, the rise of FinFET models is related to the evolution of DG models. The fabrication process of these bulk FinFETs is reported to be compatible with standard CMOS technology [3].

The advantages of Mug-FET technology are higher drain current and switching speed, less than half the dynamic power requirement with 90% less static leakage current. Double Gate (DG) MOSFET fabricated on SOI wafers is one of the most promising candidate due to its attractive features of high current drivability ($I_{\text{on}}$), transconductance ($g_{\text{m}}$), reduced short channel effects (SCEs) [4]. Similarly, FinFETs also acquired attentions because of their low cost process steps and compatibility with CMOS technology [5][6]. The transistor performance depends on the process induced variations categorized under systematic values of gate length $L_g$, underlap gate length $L_{\text{un}}$, gate oxide thickness $t_{\text{ox}}$, etc. [7].

The main purpose of this work is to study the sensitivity of $L_{\text{un}}$ on various performance metrics of both DG MOSFET and FinFET for further scalability of the device. A systematic analysis is carried out among DG and FinFET.

2. Device design and simulation setup

The DG MOSFET and 3-D SOI-FinFET architecture simulated in this work are shown in Fig. 1(a) and (b) respectively. An n-channel MOSFET having SiO2 as interfacial oxide with high-k material (Si3N4) as spacer in the underlap regions is modeled. The spacer is used to reduce the parasitic source resistance, $R_s$ and drain resistance, $R_d$. The channel length ($L_g$) is considered as 30 nm for both devices. The Source/Drain length ($L_s/L_d$) are taken to be 40 nm, and doping, $N_D$ is uniform with a density of $5 \times 10^{19}$ cm$^{-3}$. The Equivalent Oxide Thickness (EOT) is 0.9 nm [8] and supply voltage $V_{\text{DD}}=0.7$ V. The work function for the gate electrode is tuned between 4.5 eV to 4.7 eV to achieve a constant threshold voltage for both device cases. The channel is lightly doped ($10^{15}$ cm$^{-3}$) i.e. undoped channel which maximizes the effective mobility and hence on current density from the source. The underlap length, $L_{\text{un}}$ is varied from 0 nm to 15 nm to analyse the parameter dependency. The technology parameters and the supply voltages used for the device simulations are according to the ITRS roadmap [9] for below 50 nm gate length devices. The validity of the simulator has been investigated by comparing its results with previous literature data [10]. The drift-diffusion model is the default carrier transport model in Sentaurus device simulator, which is actuated during the simulation. The mobility model with definition of band gap is included [11].

![Fig. 1. Cross sectional view of (a) DG; (b) FinFET](image-url)
3. Results and discussions

In this work, we have considered a symmetrical underlap region, Lun for both DG MOSFET and FinFET. With an increase in Lun, the source to drain coupling significantly reduces, which further reduces the subthreshold leakage current. The $I_D-V_{GS}$ characteristic with different Lun for DG and FinFET are plotted in Fig. 2 (a) and (b) respectively. The $I_{off}$ is significantly reduced with increase in Lun, which can be observed from the inset values of Fig. 2. If we make a comparison between Fig. 2(a) and (b) i.e. among DG and FinFET, then the first one shows a high drive current while the later predicts very low leakage.

Fig. 2 Drain current ($I_D$) as a function of gate to source voltage ($V_{GS}$) for $V_{DS}=V_{DD}$ with variation of Lun (a) DG; (b) FinFET.

Fig. 3 Dependency of Intrinsic Gain ($A_V$) on cutoff frequency ($f_T$) for $V_{DS}=V_{DD}$ with variation of Lun (a) DG; (b) FinFET.

Fig. 3 describes the dependency of intrinsic gain ($A_V$) on cutoff frequency ($f_T$) with a variation of Lun for DG and FinFET. From the figure it can be observed that $A_V$ increases with the increase in Lun. The $f_T$ dependency on $I_D$ with variation of Lun ranging from 0 to 15 nm for DG and FinFET is given in Fig. 4. We can observe that $f_T$ ($f_T=g_m/2\pi C_{gs}$) increases rapidly with increase in $I_D$ because higher $I_D$ generates a larger transconductance, $g_m$. From the inset of Fig. 4, FinFET predicts a higher $f_T$ value as compared to DG. Fig. 5 discussed various important performance metrics like energy delay product ($EDP=C\sqrt{2\pi CVII}$), $I_{on}/I_{off}$,
subthreshold swing (SS) and energy ($E=CV^2$) for different $L_u$ of DG and FinFET devices. The $I_{on}/I_{off}$ and SS are improved sufficiently with increase in $L_u$. This is due to the reduction in source drain coupling as $L_u$ increases which in results decrease the off state current and SS. However, there is a degradation which is observed in case of $EDP$ and $E$ with the increase in $L_u$. So, it is very important to choose $L_u$ to fit the energy requirements.

From the same analysis, DG MOSFET gives a higher $I_{on}/I_{off}$ ratio and lower SS, while FinFET demonstrates an improvement in $EDP$ and $E$. Similarly, Fig. 6 describes about intrinsic source drain inductance ($L_{SD}$), power dissipation ($P.D=V_{DD}*I_{off}$) and intrinsic delay ($I_{off}/(C_{gs}*V_{DD})/I_{eff}$) with a variation of $L_u$ ranging from 0 to 15 nm. An improvement in P.D. but degradation in intrinsic delay can be observed for higher $L_u$. Thus, it is needed to be careful while choosing $L_u$ for both device cases. FinFET demonstrates better results in case of $L_{SD}$, P.D. and intrinsic delay over DG MOSFET. This is because FinFET design has an optimum control on the channel which shows better immunization capability towards short channel effects (SCEs).

The extracted values for all above said parameters are tabulated and compared for different $L_u$ values for DG and FinFET in Table 1. There is an improvement in $I_{on}/I_{off}$, SS, $L_{SD}$ and P.D. can be observed with increase in $L_u$. However, degradation occurred in case of intrinsic delay, $EDP$, $Q$-factor and $g_m$ for higher $L_u$. Among
DG and FinFET, the prior one gives higher current drivability, while the later one shows an improvement in EDP and delay.

![Graph showing dependencies of various performance parameters on underlap length (Lun) of DG MOSFET and FinFET at VDS=VDD.](image)

**Fig. 6** Dependency of various performance parameters on underlap length (Lun) of DG MOSFET and FinFET at VDS=VDD. (a) Intrinsic source drain inductance (LSD); (b) Power Dissipation (P.D); (c) Intrinsic Delay.

<table>
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<tr>
<th>Lun (nm)</th>
<th>Delay (CV/I) (ps)</th>
<th>Energy (CV^2) (J) x10^-16</th>
<th>EDP (JS) (J) x10^-21</th>
<th>Inductance, LSD (H) (Delay/ghs) x10^-8</th>
<th>Ion/Ioff x10^7</th>
<th>PD (Ioff*VDD) (pW)</th>
<th>SS (mV/decade)</th>
<th>Vth (V)</th>
<th>g_m,max (mS)</th>
<th>Q-factor (g_m,max/SS)</th>
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4. Conclusion

Various performances of DG MOSFET and FinFET are systemically examined and compared using extensively 3-D device simulator Sentaurus™. We have optimized the gate underlap length (Lun) of both DG and FinFET, to demonstrate that Lun can be suitably chosen for high performance (HP) or low operating power (LOP) applications. Analog/RF performance of nanoscale DG MOSFET and FinFET is collated by means of 3-D numerical TCAD simulations. When underlap length increases, an improvement in P.D. occurs but with the compensation of high delay. Thus, it is needed to be careful while choosing Lun. There is an improvement in Ion/Ioff, SS, LSD and P.D. can be observed with increase in Lun. FinFET demonstrates better results in case of LSD, P.D. and intrinsic delay over DG MOSFET. This is because FinFET design has a bonzer control on the channel which shows better immunization capability towards short channel effects (SCEs). Among DG and FinFET, the former one gives higher current drivability, while the successive one shows the betterment in EDP and delay.
References


