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Optimization and Numerical Simulation of Multi-layer Microchannel Heat Sink

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Abstract

The configuration sizes of multi-layer microchannel heat sink is optimized in order to enhance the performance of the high flux chip, which is 556W/cm^2. Taking the thermal resistance and the pressure drop as goal functions, a double-objective optimization model was proposed based on the thermal resistance network model. The opimized microchannel heat sink is numerically simulated by computational fluid dynamics (CFD) software. The number of microchannel in width n_1 and that in height n_2 are 24 and 2, the width of optimized optimized microchannel and fin are 196 and 50 μm, respectively, and the corresponding total thermal resistance of the whole microchannel heat sink is 0.4025 ℃/W. The highest temperature is less than 98℃, which can satisfy the requirement of chip to temperature. The maximum temperature difference is 77.8673℃, and the transferred power of heat flux is 200W, so the total thermal resistance R_{total} is 0.3893 ℃/W, which agrees well with the analysis result of thermal resistance network model.

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Keywords: Microchannel Heat Sink, Optimization Design, Numerical Simulation;

1. Introduction

With the developments of international international aerospace technology, micro-electromechanical system and micro-machining technology, to transfer more heat generated by the high flux chip to keep the stable and reliable operation of the devices presents problems to be solved in microelectronic industry[1].

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When the heat flux of micro-electronic devices exceeds 100 W/cm^2, traditioanl cooling method is unlikely to meet the cooling needs[2], and microchannel heat sink has been an effective kind of substitute method. The configuration sizes of microchannel can significantly affect the heat transfer performance of microchannel heat sink, and the optimization microchannel heat sink can enhance its heat transfer performance. Chong et al.[3] modeled a single layer counter flow and a double layer counter flow microchannel heat sink with rectangular channels by employing the thermal resistance network, and the accuracy of the prediction was verified by comparing the results obtained with those from the more comprehensive three dimensional CFD conjugate heat transfer model, and good agreements were obtained. The results showed that the overal thermal resistance was related with configuartion sizes of microchannel heat sink. Shao et al.[4] optimized the cross-section sizes of microchannels, the heat flux of chip is 278 W/cm^2, and through the optimization microchannel heat sink, the highest temperature in the chip could be kept below 42℃. They[5] also optimized the configuration sizes of microchannel cooling heat sink using the thermal resistance network model, for the heat sink to cool a chip with the sizes of L×W=2.5mm×2.5mm and the power of 8W, the optimized width and height of the microchannel are 154 and 1000 μm, repectively, and its corresponding total thermal resistance is 8.255K/W.

Though the opitimized single-layer microchannel cooling heat sink can keep the temperature of chip below its working temperature, the power of the chip is low. In this paper, the configuration sizes of multi-layer microchannel cooling heat sink is optimized, and which cooling performance is simulated by CFD software, and the total thermal resistance is calculated to compare with that of thermal resistance network model.

2. Problem description

2.1. Microchannel heat sink

A double-layer microchannel cooling heat sink is shown in Figure1, which is used to cool a chip with the sizes of L×W=6mm×6mm, and the power is 200W, and the corresponding heat flux is 556W/cm^2. The working fluid is deionized water. In Figure 1, W_c and H_c are the width and depth of microchannel, W_f and H_f is the width and depth of fin, and H_{sub} is the thickness of substrate. For the symmetry of the structure of model and load, the computational zone can be half microchannel and fin and the schematic diagram of computational zone cross-section is shown in Figure2.

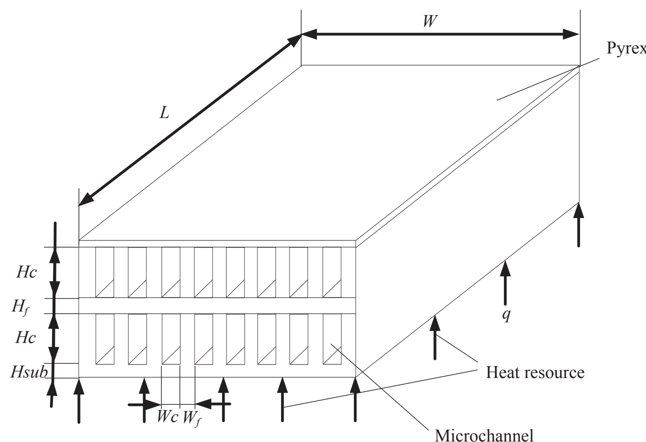

Fig. 1. schematic diagram of three-dimension rectangle double-layer microchannel cooling heat sink

Fig. 2. schematic diagram of computational zone cross-section

2.2. Thermal resistance network model

In microchannel cooling heat sink, the total resistance R'_{total} includes the substrate conduction thermal resistance R_{base}, the wall conduction thermal resistance R_{wall}, the fin conduction thermal resistance R_{fin}, the substrate convection thermal resistance $R_{base,conv}$, the wall convection thermal resistance $R_{wall,conv}$, the fin convection thermal resistance $R_{fin,conv}$ and the liquid flow thermal resistance R_{fluid}.

The thermal resistance network model of Figure2 is shown in Figure 3.

Fig. 3. The thermal resistance network model

Thus, the total thermal resistanc R'_{total} of half microchannel and fin can be expressed as:

$$R'_{total} = \frac{\{R_{base} + [R_{base,conv} \| (R_{wall} + (R_{wall,conv} + R_{base,conv}))] + R_{fluid}\} R_{fluid}}{\{R_{base} + [R_{base,conv} \| (R_{wall} + (R_{wall,conv} + R_{base,conv}))] + R_{fluid}\} + R_{fin} + R_{fin,conv} + R_{fluid}} \quad (1)$$

where the fin conduction thermal resistance R_{fin} is:

$$R_{fin} = \frac{2H_f}{k_s W_c L} \quad (2)$$

The fin convection thermal resistance $R_{fin,conv}$ is:

$$R_{fin,conv} = \frac{2}{h_{conv} W_c L} \quad (3)$$

and other thermal resistancs are the same as those of reference [5].

In equation (1), the parallel symbol "$\|$" is defined as:

$$x \| y = \frac{x \cdot y}{x + y} \quad (4)$$

According to equation (1), the total thermal resistance of the whole microchannel heat sin can be expressed as:

$$R_{total} = \frac{R'_{total}}{2n_1} \quad (5)$$

where n_1 is the number of single-layer microchannels or the number of microchannels in wide.

Besides thermal resistance, pressure drop affects the heat transfer performance of microchannel cooling heat sink[6]:

$$\Delta P = 2 f \rho_l u_{ave}^2 L / D_h \quad (6)$$

The means of symbols above equations can be seen in reference [5].

3. Optimization design and results

Select the number of microchannel in width n_1 and that in height n_2, the width of microchannel W_c and fin W_f, and the height of microchannel H_c and fin H_f as design variable, expressed as x_1, x_2, x_3, x_4, x_5 and x_6, respectively, and written in vector $\mathbf{x}$=[x_1, x_2, x_3, x_4, x_5, x_6]. The formula (1) and (6) are goal functions, and can be written in fuction of $\mathbf{x}$, as $f_1(\mathbf{x})$ and $f_2(\mathbf{x})$. The width of heat sink is constraint, and the boundary of variables are construct, the multi-objective optimization problem is:

$$\begin{cases} Find & \mathbf{x} \\ \min & F(\mathbf{x}) = \min\{f_1(\mathbf{x}), f_2(\mathbf{x})\} \\ s.t. & x_1 x_3 + (x_1+1)x_4 - 0.006 = 0 \\ & x_2 x_5 + (x_2+1)x_6 - 0.0025 = 0 \\ & 2 \le x_1 \le 100 \\ & 1 \le x_2 \le 20 \\ & 2\times10^{-5} \le x_3, x_4 \le 10^{-3} \\ & 5\times10^{-5} \le x_5, x_6 \le 10^{-3} \end{cases} \quad (7)$$

The above multi-objective optimization problem is solved by Adaptive Genetic algorithms, which can be seen in reference [7]. The optimized results of configuration sizes of microchannel cooling heat sink are shown in Table 1, and the total and component thermal resistance are listed in Table 2.

Table 1. Configuration sizes of microchannel cooling heat sink

n_1	n_2	W_c (μm)	W_f (μm)	H_c (μm)	H_f (μm)
24	2	196	50	1000	100

Table 1. Total and component thermal resistance of microchannel cooling heat sink

R_{total} ℃/W	R_{base} ℃/W	R_{wall} ℃/W	R_{fin} ℃/W	$R_{base,conv}$ ℃/W	$R_{wall,conv}$ ℃/W	$R_{fin,conv}$ ℃/W	R_{fluid} ℃/W
0.4025	0.0124	0.4328	0.2504	0.5120	0.0326	0.0218	0.1204

4. Numerical simulation and discussion

The numerical simulation is used to verify the cooling performance of optimal microchannel cooling heat sink by using electronics cooling software that has been previously used in analyzing the heat transfer character in electronics and chip cooling applications, which uses finite volume method to solve CFD problem. The inlet velocity and density of deionized water is 0.02m/s and 997kg/m^3, the specific heat is 4179 J/kg℃, and the thermal conductivity of the substrate and deionized water is 148 and 0.613 W/m℃, respectively. The Reynolds number estimated by the above conditions is about 350, therefore the flow is laminar.

Figure 4 shows the temperature distribution of the whole mirochannel cooling heat sink. The highest temperature is less than 98℃, which can satisfy the requirement of chip to temperature. The maximum temperature difference is 77.8673℃, and the transferred power of heat flux is 200W, so the total thermal resistance R_{total} is 0.3893 ℃/W. Compared with the analysis results by thermal resistance model in Table 2, the relative error is 3.2795 percent, which shows the results of numerical simulation agree well with the analysis results. Figure 5 shows the temperature distibution of deionized water in microchannel. The highest temperature is less than 80 ℃, so the deionized water is still at fluid state.

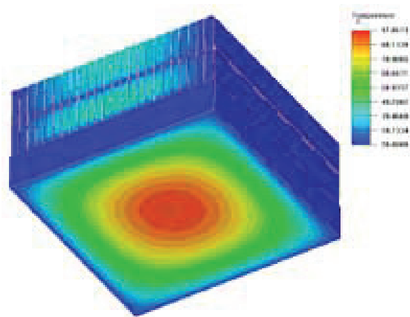

Fig. 4. The temperature distribution of whole microchannel cooling heat sink

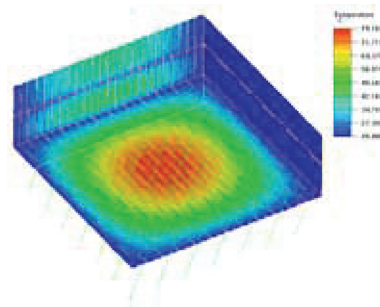

Fig. 5. The temperature distribution of deionized water in microchannel

5. Conclusions

A multi-layer microchannel cooling heat sink is optimized using adaptive GA considering the couple solution of the flow and heat transfer, and numerical simulation is used to verify the cooling performance of optimal microchannel cooling heat sink.

The number of microchannel in width n_1 and that in height n_2 are 24 and 2, the width of optimized optimized microchannel and fin are 196 and 50 μm, respectively, and the corresponding total thermal resistance of the whole microchannel heat sink is 0.4025 ℃/W.

The results of numerical simulatin agree well with the analysis result, which shows that the theory analysis of thermal resistance network model is reasonable.

The simulation results also show that the optimized microchannel cooling heat sink has favorable heat transfer performance, which can satisfy the requirement for removal of high heat flux in new-generation chips.

Acknowledgements

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